Title (en)

DOUBLE-GATE FOUR-TERMINAL SEMICONDUCTOR COMPONENT WITH FIN-TYPE CHANNEL REGION

Title (de)

DOPPELGATE-VIERPOL-HALBLEITERBAUELEMENT MIT FINNENFÖRMIGEM KANALGEBIET

Title (fr)

DISPOSITIF SEMI-CONDUCTEUR QUADRIPOLAIRE À DOUBLE GRILLE AYANT UNE RÉGION DE CANAL EN FORME D'AILERON

Publication

EP 4315428 A2 20240207 (DE)

Application

EP 22716902 A 20220318

Priority

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- EP 2022057201 W 20220318

Abstract (en)

[origin: WO2022207369A2] A double-gate four-terminal semiconductor component (100), comprising a substrate (102), an electrically insulating cover layer (104) on the substrate (102), a fin-type channel region (110) situated above the substrate and composed of a doped semiconductor material of a first conductivity type having two mutually opposite longitudinal sides (110.1, 110.2) extending along a longitudinal direction of the channel region (110), the channel region (110) having a first end (118) and a second end (119) in the longitudinal direction, a first and a second gate electrode (112, 113), which are situated on the cover layer (104) and are arranged opposite one another each on one of the longitudinal sides (110.1, 110.2) of the channel region (110) and are each electrically insulated from the longitudinal sides (110.1, 110.2) by an insulation layer (114, 115), a first and a second contact region (106, 107) situated on the cover layer and composed of a semiconductor material of a second conductivity type, which are each arranged next to one of the gate electrodes (112, 113) toward the first end (118) in the longitudinal direction of the channel region (110), each of the two contact regions (106, 107) being electrically conductively connected to the channel region (110) and being electrically insulated from the adjacent gate electrode (112, 113) by an insulation layer, a third and a fourth contact region (108, 109) situated on the cover layer (104) and composed of a semiconductor material of the second conductivity type, which are each arranged next to one of the gate electrodes (112, 113) toward the second end (119) in the longitudinal direction of the channel region (110), each of the two contact regions (108, 109) being electrically conductively connected to the channel region (110) and being electrically insulated from the adjacent gate electrode (112, 113) by an insulation layer, a transverse extent ("D") of the channel region (110) in a transverse direction being dimensioned such that in a first operating state, in which a first and a second operating voltage are respectively applied to the gate electrodes (112, 113), two conductivity channels (120, 121) of the second conductivity type separated by a barrier region (122) in the transverse direction of the channel region (110) are formed.

IPC 8 full level

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CPC (source: EP US)

H01L 27/1211 (2013.01 - EP US); **H01L 29/0847** (2013.01 - US); **H01L 29/7606** (2013.01 - EP); **H01L 29/7855** (2013.01 - EP US)

Citation (search report)

See references of WO 2022207369A2

Designated contracting state (EPC)

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KH MA MD TN

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