

Title (en)

PIPELINED OPERATIONS IN NEURAL NETWORKS

Title (de)

PIPELINEOPERATIONEN IN NEURONALEN NETZWERKEN

Title (fr)

OPÉRATIONS EN PIPELINE DANS DES RÉSEAUX NEURONAUX

Publication

EP 4323864 A1 20240221 (EN)

Application

EP 22788657 A 20220405

Priority

- US 202117231711 A 20210415
- US 2022023434 W 20220405

Abstract (en)

[origin: WO2022221092A1] An integrated circuit (IC) implements an M by N aperture function over an R by C source array. The IC has an input port receiving an ordered stream of independent input values, an output port producing an output stream, a mass multiplier circuit multiplying inputs by weights, producing streams of products on pathways on the IC, an M by N array of compositor circuits on the IC, single dedicated pathways between compositors, delay circuits, a finalization circuit, and a control circuit operating counters and producing control signals. The compositors combine the values received from product pathways, further combine that result to an initial value or to a value from an adjacent compositor upstream, or to a value from a delay circuit. Upon a last downstream compositor producing a complete composition of values, that value is passed to the finalization circuit, which posts a result to the output port.

IPC 8 full level

G06F 9/38 (2018.01)

CPC (source: EP IL KR)

G06F 7/53 (2013.01 - KR); **G06F 9/3875** (2013.01 - EP IL KR); **G06F 17/153** (2013.01 - KR); **G06N 3/0464** (2023.01 - KR);
G06N 3/063 (2013.01 - KR); **Y02D 10/00** (2017.12 - KR)

Citation (search report)

See references of WO 2022221092A1

Designated contracting state (EPC)

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

Designated extension state (EPC)

BA ME

Designated validation state (EPC)

KH MA MD TN

DOCDB simple family (publication)

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DOCDB simple family (application)

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