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(54) **APPARATUS FOR PACKAGING SEMICONDUCTOR DEVICES**

VORRICHTUNG ZUM KAPSELN VON HALBLEITERBAUELEMENTEN

APPAREIL POUR EMBALLER DES DISPOSITIFS À SEMI-CONDUCTEURS

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Description

TECHNICAL FIELD

[0001] The present invention is related to packaging semiconductor devices. More specifically, the invention provides apparatus for packaging semiconductor devices, and packaged semiconductor components.

BACKGROUND

[0002] Semiconductor devices are typically manufactured on semiconductor wafers or other types of work pieces using sophisticated equipment and processes that enable reliable, high-quality manufacturing. The individual dies (e.g., devices) generally include integrated circuits and a plurality of bond-pads coupled to the integrated circuits. The bond-pads provide an array of external contacts through which supply voltage, electrical signals, and other input/output parameters are transmitted to/from the integrated circuits. The bond-pads are usually very small, and they are typically arranged in dense arrays having fine pitches between bond-pads. The dies are quite delicate and need to be protected from the environment and for handling. As a result, the dies are packaged to protect them and to connect the bond-pads to an array of larger terminals that are easier to connect to a printed circuit board. The packaged semiconductor components can then be electrically connected to other microelectronic devices or circuits in many types of products.

[0003] Ceramic packages are one type of packaging for semiconductor dies. Ceramic packages typically have individual ceramic units that have a cavity, die contacts within the cavity, and external terminals electrically coupled to the die contacts. The external terminals are generally on the exterior sidewall or backside of the ceramic unit. A die is positioned in the cavity, and the bond-pads on the dies are electrically coupled to the die contacts within the cavity. An encapsulant is then deposited into the cavity to cover the die.

[0004] Ceramic packages are useful in many applications, but they also have several drawbacks. One drawback of ceramic packages is that the ceramic units are generally handled individually instead of being in the form of a wafer that can be handled in wafer processing equipment. As a result, each of the individual ceramic units must be loaded into trays for the packaging process, and then unloaded for subsequent processing. This type of handling is costly and impacts the throughput of packaging processes. Ceramic packages are also relatively expensive to a manufacturer compared to other types of packages. Therefore, ceramic packages have several drawbacks.

[0005] Another cavity-type semiconductor package has a polymer riser laminated to a circuit board. For example, Kinsus Company of Korea makes a non-stacking cavity package that includes a printed circuit board having a plurality of die contacts on one side and a plurality of backside contacts on the other side. The package further includes an upper board without circuitry laminated to the printed circuit board. The upper board has openings that define cavities over the printed circuit board, but the upper board does not include any circuitry or vias. A die is mounted to the printed circuit board within the cavity formed by the opening in the upper board, and the bond-pads on the die are connected to the die contacts on the printed circuit board. The cavity is then filled with a polymer or other type of encapsulant to encapsulate the die.

[0006] US5043794 describes an integrated circuit package comprising a thermally conductive plate and an open rectangular structure of conductor and insulator for surrounding the sides of the circuit and presenting one or more linear arrays of conductive connectors extending laterally through the rectangular structure.

[0007] US2001/0023980A describes a stacked semiconductor device including a plurality of stacked wiring substrates with a semiconductor device mounted on each of the wiring substrates and electrically connected to the wires thereof.

[0008] US6469374B describes a semiconductor device including a superposed structure formed by superposing a plurality of superposed substrates each comprised of a wiring printed substrate loaded with a semiconductor element and an inner conductive-via provided insulating substrate.

[0009] EP1617714A describes an electronic circuit assembly comprises a casing having two opposite outer faces and an inner space separate from each of said outer faces by a respective closing portion, and a die incorporating an integrated circuit. The casing includes integrated electrically conducting elements connecting terminals of the die to pads of the casing. The electrically conducting elements also connect sets of pads respectively located on each one of the opposite outer faces of the casing. Such electronic circuit assemblies are suitable for being stacked with bonding means arranged between respective sets of pads of two successive electronic circuit assemblies in a stack.

[0010] Although such laminated packages are useful and relatively inexpensive to manufacture, they are not well suited for stacking packages in high-density applications. For example, such laminated packages cannot be used in stacked assemblies because these packages do not provide an electrical connection that routes power and signals to/from the upper package(s). Therefore, it would be desirable to develop a cavity-type package using laminated circuit board material for manufacturing high-density stacks with fully tested packages.

[0011] To this end, the invention provides the apparatus according to claim 1. Advantageous additional aspects follow from the dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012]

Figure 1 is a cross-sectional view illustrating a packaged semiconductor component in accordance with an embodiment of the invention.

Figures 2A-G are cross-sectional views illustrating stages of a method for manufacturing packaged semiconductor components in accordance with an embodiment of the invention.

Figure 2H is a top plan view of a plurality of packaged semiconductor components in accordance with an embodiment of the invention.

Figures 3A and 3B are flow charts illustrating methods in accordance with embodiments of the invention.

Figure 4 is a schematic, cross-sectional view illustrating a stacked assembly of packaged semiconductor components in accordance with an embodiment of the invention.

Figure 5 is a schematic, cross-sectional view illustrating a stacked assembly of packaged semiconductor components in accordance with an alternative example which is not part of the claimed invention.

Figure 6 is a schematic cross-sectional view illustrating a stacked assembly of packaged semiconductor components in accordance with still alternative example which is not part of the claimed invention.

Figure 7 is a schematic view of a system that incorporates packaged semiconductor components in accordance with embodiments of the invention.

DETAILED DESCRIPTION

[0013] Specific details of several embodiments of the disclosure are described below with reference to packaged semiconductor components, and apparatus for packaging semiconductor devices. The devices are manufactured on semiconductor wafers that can include substrates upon which and/or in which microelectronic devices, micromechanical devices, data storage elements, optics, read/write components, and other features are fabricated. For example, SRAM, DRAM (e.g., DDR/SDRAM), flash memory (e.g., NAND/memory), processors, imagers, and other types of devices can be constructed on semiconductor wafers.

[0014] Figure 1 is a cross-sectional view that schematically illustrates a packaged semiconductor component 100 in accordance with one embodiment of the invention. In this embodiment, the semiconductor component 100 includes a base 110 having a first substrate 112, a riser 120 having a second substrate 122, and a semiconductor die 130 attached to the base 110. The first and second substrates 112 and 122 can be composed of polymeric materials (resins, silicones, etc.), organic materials other than polymeric materials, or other suitable non-ceramic dielectric materials. For example, the first substrate 112 and the second substrate 122 can be composed of laminated circuit board materials. Several embodiments of the packaged semiconductor component 100 provide a cost-effective cavity-type package composed of a polymeric material that is suitable for stacking. In specific embodiments, for example, a stacked assembly can have identical or other types of packaged semiconductor components 100 attached to the top of the riser 120 to provide high-density stacks of fully tested packaged devices.

[0015] In the illustrated embodiment of the base 110, the first substrate 112 has a front side 114 and a backside 115. The illustrated embodiment of the base 110 further includes a plurality of die contacts 116, a first array of first backside terminals 117 at the backside 115, and a second array of second backside terminals 118 at the backside 115. The die contacts 116 in the embodiment shown in Figure 1 are located at, or at least proximate to, the front side 114 of the first substrate 112. The die contacts 116, however, can be located at the backside 115 in other embodiments for board-on-chip configurations as described in more detail below. The base 110 further includes first interconnects 119 electrically coupling the die contacts 116 to corresponding first backside terminals 117. The packaged semiconductor component 100 can also have wire-bonds 132 electrically connecting bond-pads (not shown) on the die 130 to the die contacts 116. The first interconnects 119 and the wire-bonds 132 can accordingly carry the signals and power between the die 130 and the first backside terminals 117.

[0016] In the specific embodiment of the riser 120 shown in Figure 1, the second substrate 122 includes a first side 124 and a second side 125. The first side 124 of the second substrate 122 is attached to the front side 114 of the first substrate 112 by an adhesive (not shown in Figure 1) at the interface between the first and second substrates 112 and 122. The illustrated embodiment of the riser 120 further includes an opening 126 that defines a die cavity 127 in which the die 130 is positioned. The riser 120 can further include a plurality of front contacts 128 at the second side 125 of the second substrate 122. The front contacts 128 provide electrical terminals for contacting solder balls or other types of electrical connectors on a packaged component that is stacked on top of the packaged semiconductor component 100.

[0017] The packaged semiconductor component 100 further includes a plurality of second interconnects 140 that extend through the base 110 and the riser 120. For example, the packaged semiconductor component 100 can have a through package via 141 that extends through the thickness of the first substrate 112 and the thickness of the second substrate 122. The via 141 can then be at least partially filled with a conductive material to form the second interconnects 140 (e.g., through package interconnects). The second interconnects 140 electrically couple the front contacts 128 at the second side 125 of the second substrate 122 to corresponding second back-

side terminals 118 at the backside 115 of the first substrate 112. The second interconnects 140 provide a package stack route to transmit power and electrical signals to/from another packaged semiconductor component (not shown) stacked on top of the packaged semiconductor component 100 illustrated in Figure 1. The second interconnects 140 can also carry power and/or electrical signals for the die 130 shown in the packaged semiconductor component 100 of Figure 1.

[0018] The packaged semiconductor component 100 can further include a protective material 150 in the cavity 127 to cover the die 130 and the wire-bonds 132. The protective material 150 can be deposited using a needle-like dispenser, stenciling, molding, or other suitable technique. The protective material 150 is generally a polymer or other suitable material that covers the die 130 and the wire-bonds 132. The upper surface of the protective material 150 is generally co-planar or below the second side 125 of the second substrate 122. The upper surface of the protective material 150, however, can project above the second side 125 so long as the protective material 150 does not interfere with any packages that may be stacked on top of the packaged semiconductor component 100.

[0019] Figures 2A-2G illustrate stages of a specific embodiment of a method for packaging semiconductor devices. Figure 2A illustrates a stage of the method at which a first board 210 (e.g., base panel) has a dielectric core 212, a front side 213, a first conductive layer 214 at the front side 213, a backside 215, and a second conductive layer 216 at the backside 215. The dielectric core 212 can be a polymer, non-polymeric organic material, or another suitable non-ceramic dielectric material. The first and second conductive layers 214 and 216 can be copper or other suitably conductive materials. Figure 2B illustrates the first board 210 at a subsequent stage in which first openings 218 are formed through the first conductive layer 214, the dielectric core 212, and the second conductive layer 216. The first openings 218 can be formed by drilling, etching, laser cutting, water jetting, or other suitable techniques. For example, the openings 218 can be formed using mechanical drills or laser drills known in the art.

[0020] Figure 2C illustrates the first board 210 at a stage of the method in which first interconnects 220 are formed in the first openings 218 to electrically couple the first conductive layer 214 to the second conductive layer 216. The first interconnects 220 can be formed by plating material onto the sidewall of the first openings 218 as known in the art. For example, the first interconnects 220 can comprise copper plated onto the sidewalls of the first openings 218. Figure 2D illustrates another stage of the method in which the first conductive layer 214 has been patterned and etched to form conductive traces 217 on the front side 213 of the first board 210, and the second layer 216 has been patterned and etched to form conductive traces 219 on the backside 215 of the first board 210. A solder mask 230 or other type of dielectric element can also be formed in the region between the openings 218. As described in more detail below, the solder mask 230 provides a die-attach site at which a die is positioned, and the solder mask can fill the open volume in the first openings 218.

[0021] Figure 2E illustrates a subsequent stage of the method in which a second board 250 is attached to the first board 210. The second board 250 can include a second substrate 252, a first side 254, a second side 256, and an opening 258. The opening 258 can be formed in a previous process by punching larger holes through the second board 250. The opening 258 is aligned with the die-attach site over the solder mask 230 to form a cavity 260 in which a die (not shown in Figure 2E) can be positioned. The second board 250 can accordingly be a riser panel or riser board that forms the riser projecting above the die. The second board 250 can further include patterned conductive traces 262 on the second side 256.

[0022] The second board 250 is attached to the first board 210 by an adhesive 270. In the embodiment illustrated in Figure 2E, the first side 254 of the second board 250 is attached to the front side 213 of the first board 210 by the adhesive 270. The adhesive 270 can be pre-attached to the first side 254 of the second board 250 or the front side 213 of the first board 210. In many applications, the first board 210 includes a plurality of package regions that each include a die-attach site, and the second board 250 includes a plurality of openings 258. As such, the second board 250 is positioned over the first board 210 such that the openings 258 are aligned with corresponding die-attach sites. Aligning the openings 258 with the die-attach sites may be difficult because the openings 258 will cause the second board to have significantly different contraction/expansion properties than the first board 210. To overcome this, the first and second boards 210 and 250 can have alignment holes through which a jig with alignment pins is connected. The first board 210 and the second board 250 are then moved toward each other along the alignment pins until the adhesive 270 secures the first and second boards 210 and 250 together. The adhesive 270 can have a low flow characteristic such that it does not flow into the cavity 260 and cover the traces 217 at the front side 213 of the first board 210.

[0023] Figure 2F illustrates a portion of an assembled apparatus 200 for packaging semiconductor devices at another stage in which openings 270 (e.g., through package vias) have been formed through the first board 210 and the second board 250. The openings 270 can be drilled through the first and second boards 210 and 250. The openings 270 have sidewalls 272 that extend through the first substrate 212, the adhesive 270, and the second substrate 252. The openings 270 are at least partially filled with a conductive material to form second interconnects 274 (e.g., through package interconnects). The second interconnects 274 can be formed by plating a material, such as copper, to the sidewalls 272 of the openings 270. The second interconnects 274 electrically

couple the conductive traces 262 at the second side 256 of the second board 250 to the traces 219 on the backside 215 of the first board 210.

[0024] Figure 2G illustrates the apparatus 200 with a packaged die at a subsequent stage of the method. The apparatus 200 has a first solder mask 281 at the second side 256 of the second board 250. The first solder mask 281 can fill the open space within the openings 270 (Figure 2F), and the first solder mask 281 has openings 282 over portions of the conductive traces 262 in which front contacts can be formed. In an alternative embodiment, the openings 270 can be filled by a via fill material before applying the first solder mask 281. The apparatus 200 also has a second solder mask 283 at the backside 215 of the first board 210. The second solder mask 283 has openings 284 in which backside terminals can be formed. The apparatus 200 can then be plated to form first backside terminals 291 at the backside 215 of the first board 210, second backside terminals 292 at the backside 215 of the first board 210, and front contacts 294 at the second side 256 of the second board 250. The plating process can also form die contacts 296 at the die-attach site within the cavity 260. The backside terminals and the contacts can be formed by plating a nickel layer 297 onto the traces, and then plating a gold layer 298 onto the nickel layer 297. The first and second backside terminals 291 and 292 can be arranged in conventional JEDEC pinning configurations for bottom or outboard stacking.

[0025] After forming the apparatus 200, a die 130 is mounted to the solder mask 230, and bond-pads 131 on the die 130 are connected to the die contacts 296. In the embodiment illustrated in Figure 2G, the bond-pads 131 are connected to the die contacts 296 by wire-bonds 132. After the die 130 is electrically connected to the apparatus 200, the cavity 260 can be at least partially filled with the protective material 150 as described above with reference to Figure 1.

[0026] Figure 2H is a top view illustrating the apparatus 200 with a plurality of packaged dies 130. Referring to Figures 2G and 2H together, the first board 210 (shown in Figure 2G) and the second board 250 can be configured into a strip having an array of individual package areas 299 (Figure 2H). The apparatus 200 is cut along lines S-S to separate individual packaged components from each other. In several embodiments, the individual packaged semiconductor components can be tested while the apparatus 200 is in a contiguous strip before cutting the apparatus 200 to avoid handling individual packages for testing. In an alternative embodiment, the apparatus 200 is cut along lines S-S before testing the individual packaged semiconductor components, and then the individual packaged components are loaded into a tray for testing. In either situation, only known-good-packages can be identified before they are stacked or otherwise mounted to a circuit board.

[0027] Many embodiments of the apparatus 200 may be significantly less expensive to implement compared to ceramic cavity-type packages. First, a plurality of dies can be mounted to the apparatus 200 in a strip format to eliminate the need to transfer individual cavity-type units to/from handling trays. This significantly reduces the time and manufacturing costs associated with cavity-type packaging. Many embodiments of the apparatus 200 may also be relatively inexpensive because the package can be made from polymeric materials or other suitable non-ceramic dielectric materials. Many embodiments of the apparatus 200 and the packaged semiconductor component 100 can accordingly provide a cost-effective cavity-type package suitable for stacking.

[0028] Several embodiments of the apparatus 200 and the packaged semiconductor component 100 can also have JEDEC contact configurations on the bottom package for testing and stacking the individual packaged semiconductor component 100 using existing equipment. This further enhances the efficiency of several embodiments of the apparatus 200 and the packaged semiconductor component 100 for manufacturing semiconductor devices.

[0029] Several embodiments of the apparatus 200 also enable cost-effective testing of the packaged semiconductor components because the packaged dies can be tested while the apparatus 200 is in a strip format. More specifically, the strip can be arranged in the pattern of a test tray to avoid having to transfer individual packages to/from the test trays. As such, the packaged devices can be tested more efficiently.

[0030] Figure 3A is a flow chart of an embodiment of a method 300 for manufacturing an apparatus for packaging semiconductor devices. The method 300 can include attaching a first side of a riser board to a front side of a base board (block 310). The riser board is attached to the base board so that individual openings in the riser board form die cavities aligned with corresponding individual package areas of the base board. The base board can have die contacts, first backside terminals at a backside of the base board, and second backside terminals at the backside of the base board. The die contacts can be electrically coupled to the first backside terminals. The method 300 can further include forming a plurality of through package vias extending through the riser board and the base board (block 320). Additionally, the method 300 can further include depositing a conductive material in the through package vias (block 330). The conductive material can form through package interconnects that electrically couple front side contacts at a second side of the riser board to corresponding second backside terminals at the backside of the base board.

[0031] Figure 3B is a flow chart illustrating an embodiment of a method 340 for manufacturing semiconductor components. In one embodiment, the method 340 can include providing an apparatus in which a plurality of dies are to be packaged (block 350). The apparatus can comprise a first board having a front side, a backside, arrays of die contacts, arrays of first backside terminals electrically coupled to the die contacts, arrays of second backside terminals, and a plurality of individual package are-

as. The individual package areas can have an array of the die contacts, an array of the first backside terminals, and an array of the second backside terminals. The apparatus can further include a second board having a first side laminated to the front side of the first board, a second side, openings through the second board aligned with individual package areas, and arrays of front contacts at the second side. The openings form die cavities over the first board, and the front contacts are electrically coupled to the second backside terminals by through package interconnects extending through the first board and the second board. The method 340 can further include positioning semiconductor dies in the cavities (block 360), and electrically coupling the dies to corresponding die contacts of the first board (block 370). The method can also include depositing a protective material into the die cavities (block 380) to cover the dies within the cavities. The apparatus with the first and second boards can then be cut to separate individual packaged semiconductor components from each other.

[0032] Figure 4 is a cross-sectional view that schematically illustrates a stacked assembly 400 having a first packaged component 100a and a second packaged component 100b stacked on the first packaged component 100a. The first and second packaged components 100a and 100b can be similar or identical to the packaged semiconductor component 100 described above with reference to Figure 1. Therefore, like reference numbers can refer to like components in Figures 1 and 4. The first packaged component 100a can have a plurality of first connectors 402, such as solder balls, coupled to the first backside terminals 117. The first packaged component 100a can also include additional first connectors 404 coupled to the second backside terminals 118. The connectors 404, however, are optional and may not be included in many embodiments. The second packaged component 100b can include a plurality of second connectors 406, such as solder balls, attached to the second backside terminals 118 on the backside of the second packaged component 100b. The second connectors 406 of the second packaged component 100b are connected to the front contacts 128 of the first packaged component 100a. An underfill or other type of protective material may be inserted between the first and second packaged components 100a and 100b. In operation, the die-to-package routing in the stacked assembly 400 can proceed as shown by arrows 410. Additionally, the routing from the second component 100b to the first packaged component 100a can occur as shown by arrows 420.

[0033] Figure 5 schematically illustrates a stacked assembly 500 in accordance with another arrangement which is not part of the claimed invention. This arrangement is for flip-chip applications. The stacked assembly 500 includes a first packaged component 510a and a second packaged component 510b. The first and second packaged semiconductor components 510a and 510b can be similar to the packaged semiconductor components 100 described above. However, the dies 130 are flip-chip dies that are connected to the die contacts using flip-chip connections instead of wire-bonds. As such, the die contacts 116 are positioned at the die-attach site to be covered by the die 130.

[0034] Figure 6 schematically illustrates a stacked assembly in accordance with still another arrangement which is not part of the claimed invention. This arrangement is for board-on-chip applications. In this embodiment, the stacked assembly 600 includes a first packaged component 610a having a board-on-chip design and a second packaged component 610b also having a board-on-chip design. More specifically, the dies 130 are inverted compared to the dies 130 illustrated in Figure 1 such that the bond-pads 131 on the dies are wire-bonded to the die contacts 116 on the backside of base boards 612a and 612b of each of the first and second packaged components 610a and 610b, respectively. Referring to the first packaged semiconductor component 610a, the base board 612a has an opening 614a or slot through which the wire-bonds 132 extend from the bond-pads 131 to the die contacts 116. Similarly, the base board 612b can have a slot 614b. The first interconnects from the die contacts 116 can accordingly be traces that extend along the backside of the base board 612a instead of through the base board as shown in the packaged semiconductor component 100 of Figure 1. The board-on-chip packaged components may accordingly eliminate the metallization of the front side of the base board.

[0035] Figure 7 illustrates a system 700 that includes any one of the packaged semiconductor components described above with reference to Figures 1-6. More specifically, any one of the semiconductor components described above with reference to Figures 1-6 can be incorporated into any of a myriad of larger and/or more complex systems, and the system 700 is merely a representative sample of such a system. The system 700 can include a processor 701, a memory 702 (e.g., SRAM, DRAM, flash, or other memory devices), input/output devices 703, and/or subsystems and other components 704. The packaged semiconductor components may be included in any of the components shown in Figure 7. The resulting system 700 can perform any of a wide variety of computing, processing, storage, sensing, imaging, and/or other functions. Accordingly, the system 700 can be, without limitation, a computer and/or other data processor, for example, a desktop computer, laptop computer, Internet appliance, hand-held device, multi-processor system, processor-based or programmable consumer electronic, network computer, and/or mini-computer. Suitable hand-held devices for these systems can include palm-type computers, wearable computers, cellular or mobile phones, personal digital assistants, etc. The system 700 can further be a camera, light or other radiation sensor, server and associated server subsystems, and/or any display device. In such systems, individual dies can include imager arrays, such as CMOS imagers. Components of the system 700 may be housed in a single unit or distributed over multiple, interconnected

units (e.g., through a communications network). The components of the system 700 can accordingly include local and/or remote memory storage devices and any of a wide variety of computer-readable media.

[0036] From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that the invention is not limited except as by the appended claims.

Claims

1. An apparatus for packaging semiconductor devices, comprising:

a first board (210) including a first substrate (112; 212) having a front side (114; 213) and a backside (115; 215), arrays of die contacts (116; 296) located at the front side of the first substrate, arrays of first backside terminals (117; 291) electrically coupled to the die contacts, arrays of second backside terminals (118; 292), and a plurality of individual package areas (299) that have a die attach site, an array of the first backside terminals, and an array of the second backside terminals, wherein the first board further comprises first interconnects (119; 220) electrically coupling the die contacts with corresponding first backside terminals;
a second board (250) having a first side (254) laminated to the front side of the first substrate, a second side (256), openings (258) through the second board aligned with individual package areas that define die cavities (260), and arrays of front contacts (294) at the second side electrically coupled to the second backside terminals by second interconnects (140; 274) extending through the first board and the second board;
a semiconductor die (130) attached to the front side of the first substrate, wherein an array of the die contacts are positioned at the die attach site so as not to be covered by the semiconductor die; and
wherein the second interconnects extending through the first board and the second board provide a package stack route that can transmit power and electrical signals to/from another packaged semiconductor component when such another packaged semiconductor component is stacked on top of the second board.

2. The apparatus of claim 1 wherein the first and second boards have a polymeric core.

3. The apparatus of claim 1 wherein the interconnects extending through the first and second boards are continuous through package interconnects.

4. The apparatus of claim 1 wherein the first board comprises a first printed circuit board and the second board comprises a second printed circuit board.

5. The apparatus of claim 1 wherein the individual package areas and the die cavities are arranged in a strip, and wherein individual die cavities are separated by cutting lanes on the strip.

6. The apparatus of claim 1, wherein:

the first substrate comprises a polymeric material;
the second board comprises a riser (120) having the first side attached to the front side of the first substrate, the second side, and the plurality of openings that define die cavities, wherein the riser comprises a polymeric material;
the arrays of first backside terminals are at the backside of the first substrate;
the arrays of front contacts are at the second side of the riser;
the arrays of second backside terminals are at the backside of the first substrate; and
the second interconnects extending through the first substrate and the riser.

7. The apparatus of claim 6 wherein the first substrate comprises a first printed circuit board, the riser comprises a second printed circuit board, and the openings comprise punched holes in the second printed circuit board.

8. The apparatus of claim 7 wherein the second terminals comprise continuous through package terminals extending from the second side of the riser to the backside of the first substrate.

9. The apparatus of claim 1, wherein:

the first substrate is a first polymeric substrate;
the second board comprises a riser having a second polymeric substrate with the first side and the second side, and the openings;
the second interconnects extend through the first polymeric substrate and the second polymeric substrate; and
the semiconductor die is in the die cavity and has an integrated circuit electrically coupled to the die contacts.

10. The apparatus of claim 9, further comprising a second packaged semiconductor component (100a, 100b) stacked on the second side of the riser, wherein the second packaged semiconductor component has electrical connectors attached to the front contacts.

11. The apparatus of claim 9 wherein die contacts are at the front side of the first substrate and the die has bond-pads wired-bonded to die contacts.

12. The apparatus of any one of claims 1 to 8, further comprising a die in the die cavity.

13. The apparatus of claim 1, wherein a portion of each of the die contacts (116; 296) is exposed within the openings (126; 258).

Patentansprüche

1. Einrichtung zum Kapseln von Halbleitervorrichtung, umfassend:

eine erste Platine (210) einschließlich eines ersten Substrats (112; 212) mit einer Vorderseite (114; 213) und einer Rückseite (115; 215), Arrays von Die-Kontakten (116; 296), die sich an der Vorderseite des ersten Substrats befinden, Arrays von ersten Rückseitenanschlüssen (117; 291), die elektrisch mit den Die-Kontakten gekoppelt sind, Arrays von zweiten Rückseitenanschlüssen (118, 292) und mehrere einzelne Kapselungsbereiche (299), die eine Die-Befestigungsstelle, ein Array der ersten Rückseitenanschlüsse und ein Array der zweiten Rückseitenanschlüsse aufweisen, wobei die erste Platine ferner erste Zwischenverbindungen (119; 220) umfasst, die die Die-Kontakte elektrisch mit entsprechenden ersten Rückseitenanschlüssen koppeln;
eine zweite Platine (250) mit einer ersten Seite (254), die an die Vorderseite des ersten Substrats laminiert ist, einer zweiten Seite (256), Öffnungen (258) durch die zweite Platine, die mit einzelnen Kapselungsbereichen ausgerichtet sind und Die-Hohlräume (260) definieren, und Arrays von vorderen Kontakten (294) an der zweiten Seite, die durch zweite Zwischenverbindungen (140; 274), die sich durch die erste Platine und die zweite Platine erstrecken, elektrisch mit den zweiten Rückseitenanschlüssen gekoppelt werden;
ein Halbleiter-Die (130), der an der Vorderseite des ersten Substrats befestigt ist, wobei ein Array der Die-Kontakte so an der Die-Befestigungsstelle positioniert sind, dass sie nicht durch den Halbleiter-Die bedeckt werden;
und wobei die zweiten Zwischenverbindungen, die sich durch die erste Platine und die zweite Platine erstrecken, eine
Kapselungsstapelroute bereitstellen, die Leistung und elektrische Signale zu/von einer anderen gekapselten Halbleiterkomponente übertragen kann, wenn eine derartige andere gekapselte Halbleiterkomponente auf der zweiten Platine gestapelt ist.

2. Einrichtung nach Anspruch 1, wobei die erste und zweite Platine einen Polymerkern aufweisen.

3. Einrichtung nach Anspruch 1, wobei die Zwischenverbindungen, die sich durch die erste und zweite Platine erstrecken, kontinuierliche Durch-Kapselung-Zwischenverbindungen sind.

4. Einrichtung nach Anspruch 1, wobei die erste Platine eine erste Leiterplatte umfasst und die zweite Platine eine zweite Leiterplatte umfasst.

5. Einrichtung nach Anspruch 1, wobei die einzelnen Kapselungsbereiche und die Die-Hohlräume in einem Streifen angeordnet sind und wobei einzelne Die-Hohlräume durch Schneidespuren auf dem Streifen getrennt sind.

6. Einrichtung nach Anspruch 1, wobei:

das erste Substrat ein Polymermaterial umfasst;
die zweite Platine einen Riser (120) umfasst, der die an der Vorderseite des ersten Substrats befestigte erste Seite, die zweite Seite und die mehreren Öffnungen, die Die-Hohlräume definieren, aufweist, wobei der Riser ein Polymermaterial umfasst;
sich die Arrays von ersten Rückseitenanschlüssen an der Rückseite des ersten Substrats befinden;
sich die Arrays von vorderen Kontakten an der zweiten Seite des Risers befinden;
sich die Arrays von zweiten Rückseitenanschlüssen an der Rückseite des ersten Substrats befinden; und
sich die zweiten Zwischenverbindungen durch das erste Substrat und den Riser erstrecken.

7. Einrichtung nach Anspruch 6, wobei das erste Substrat eine erste Leiterplatte umfasst, der Riser eine zweite Leiterplatte umfasst und die Öffnungen gestanzte Löcher in der zweiten Leiterplatte umfassen.

8. Einrichtung nach Anspruch 7, wobei die zweiten Anschlüsse kontinuierliche Durch-Kapselung-Anschlüsse umfassen, die sich von der zweiten Seite des Risers zu der Rückseite des ersten Substrats erstrecken.

9. Einrichtung nach Anspruch 1, wobei:

das erste Substrat ein erstes Polymersubstrat ist; die zweite Platine einen Riser umfasst, der ein zweites Polymersubstrat mit der ersten Seite und der zweiten Seite und die Öffnungen auf-

weist;
sich die zweiten Zwischenverbindungen durch das erste Polymersubstrat und das zweite Polymersubstrat erstrecken; und
sich der Halbleiter-Die im Die-Hohlraum befindet und eine integrierte Schaltung aufweist, die elektrisch mit den Die-Kontakten gekoppelt ist.

10. Einrichtung nach Anspruch 9, ferner umfassend eine zweite gekapselte Halbleiterkomponente (100a, 100b), die auf der zweiten Seite des Risers gestapelt ist, wobei die zweite gekapselte Halbleiterkomponente elektrische Verbinder aufweist, die an den vorderen Kontakten befestigt sind.

11. Einrichtung nach Anspruch 9, wobei sich Die-Kontakte an der Vorderseite des ersten Substrats befinden und der Die Bondpads aufweist, die mit Die-Kontakten drahtgebondet sind.

12. Einrichtung nach einem der Ansprüche 1 bis 8, ferner umfassend einen Die im Die-Hohlraum.

13. Einrichtung nach Anspruch 1, wobei ein Teil von jedem der Die-Kontakte (116; 296) in den Öffnungen (126; 258) freigelegt ist.

Revendications

1. Appareil permettant d'encapsuler des dispositifs semi-conducteurs, comprenant :

une première carte (210) comprenant un premier substrat (112 ; 212) possédant un côté avant (114 ; 213) et un côté arrière (115 ; 215), des réseaux de contacts (116 ; 296) de puces situés au niveau du côté avant du premier substrat, des réseaux de premières bornes (117 ; 291) de côté arrière couplés électriquement aux contacts de puces, des réseaux de secondes bornes (118 ; 292) de côté arrière, et une pluralité de zones de boîtier individuelles (299) qui possèdent un site de fixation de puce, un réseau des premières bornes de côté arrière et un réseau des secondes bornes de côté arrière, la première carte comprenant en outre des premières interconnexions (119 ; 220) couplant électriquement les contacts de puces avec des premières bornes de côté arrière correspondantes ;
une seconde carte (250) possédant un premier côté (254) stratifié sur le côté avant du premier substrat, un second côté (256), des ouvertures (258) à travers la seconde carte alignées sur des zones de boîtier individuelles qui définissent des cavités (260) pour puces, et des réseaux de contacts avant (294) au niveau du second côté électriquement couplés aux secondes bornes de côté arrière par des secondes interconnexions (140 ; 274) s'étendant à travers la première carte et la seconde carte ;
une puce à semi-conducteur (130) fixée au côté avant du premier substrat, dans lequel un réseau des contacts est positionné au niveau du site de fixation de puce de façon à ne pas être couvert par la puce à semi-conducteur ; et
dans lequel les secondes interconnexions s'étendant à travers la première carte et la seconde carte forment un itinéraire d'empilement de boîtiers qui peut transmettre une puissance et des signaux électriques de/vers un autre composant semi-conducteur encapsulé lorsqu'un tel autre composant semi-conducteur encapsulé est empilé en haut de la seconde carte.

2. Appareil selon la revendication 1 dans lequel les première et seconde cartes ont un coeur polymère.

3. Appareil selon la revendication 1 dans lequel les interconnexions s'étendant à travers les première et seconde cartes sont des interconnexions de boîtier traversantes continues.

4. Appareil selon la revendication 1 dans lequel la première carte comprend une première carte de circuits imprimés et la seconde carte comprend une seconde carte de circuits imprimés.

5. Appareil selon la revendication 1 dans lequel les zones de boîtier individuelles et les cavités pour puces sont agencées dans une bande, et dans lequel les cavités pour puces individuelles sont séparées par des lignes de coupe sur la bande.

6. Appareil selon la revendication 1, dans lequel :

le premier substrat comprend un matériau polymère ;
la seconde carte comprend une tige (120) possédant le premier côté fixé au côté avant du premier substrat, au second côté, et à la pluralité d'ouvertures qui délimitent les cavités pour puces, la tige comprenant un matériau polymère ;
les réseaux des bornes de côté arrière sont au niveau du côté arrière du premier substrat ;
les réseaux des contacts avant sont au niveau du second côté de la tige ;
les réseaux des secondes bornes de côté arrière sont au niveau du côté arrière du premier substrat ; et
les secondes interconnexions s'étendant à travers le premier substrat et la tige.

7. Appareil selon la revendication 6 dans lequel le premier substrat comprend une première carte de cir-

cuits imprimés, la tige comprend une seconde carte de circuits imprimés, et les ouvertures comprennent des trous perforés dans la seconde carte de circuits imprimés.

8. Appareil selon la revendication 7 dans lequel les secondes bornes comprennent des bornes de boîtier traversantes continues s'étendant depuis le second côté de la tige vers le côté arrière du premier substrat.

9. Appareil selon la revendication 1, dans lequel :

le premier substrat est un premier substrat polymère ;
la seconde carte comprend une tige possédant un second substrat polymère avec le premier côté et le second côté, et les ouvertures ;
les secondes interconnexions s'étendent à travers le premier substrat polymère et le second substrat polymère ; et
la puce à semi-conducteur se situe dans la cavité pour puce et possède un circuit intégré électriquement couplé aux contacts de puces.

10. Appareil selon la revendication 9, comprenant en outre un second composant semi-conducteur encapsulé (100a ; 100b) empilé sur le second côté de la tige, dans lequel le second composant semi-conducteur encapsulé possède des connecteurs électriques fixés aux contacts avant.

11. Appareil selon la revendication 9 dans lequel les contacts de puces sont au niveau du côté avant du premier substrat et la puce possède des pastilles liées par fil aux contacts de puces.

12. Appareil selon l'une quelconque des revendications 1 à 8, comprenant en outre une puce dans la cavité pour puce.

13. Appareil selon la revendication 1, dans lequel une partie de chacun des contacts (116 ; 296) de puces est apparente dans les ouvertures (126 ; 258).

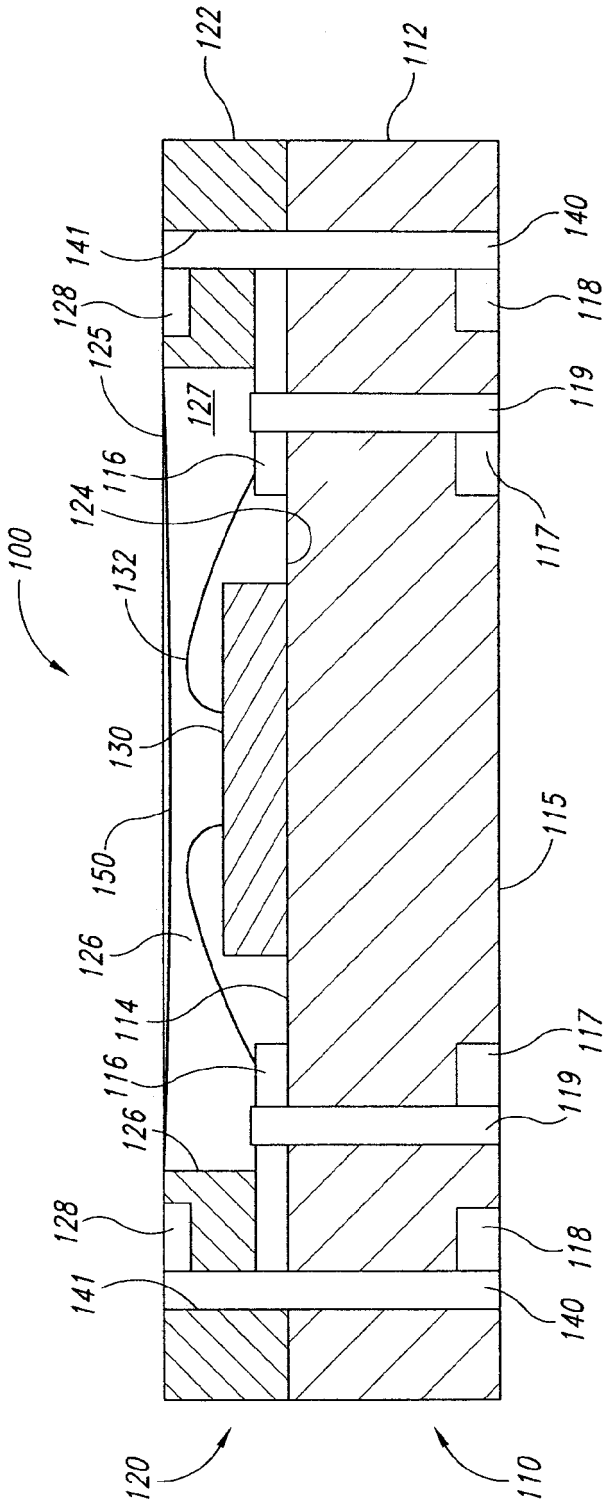
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Fig. 1

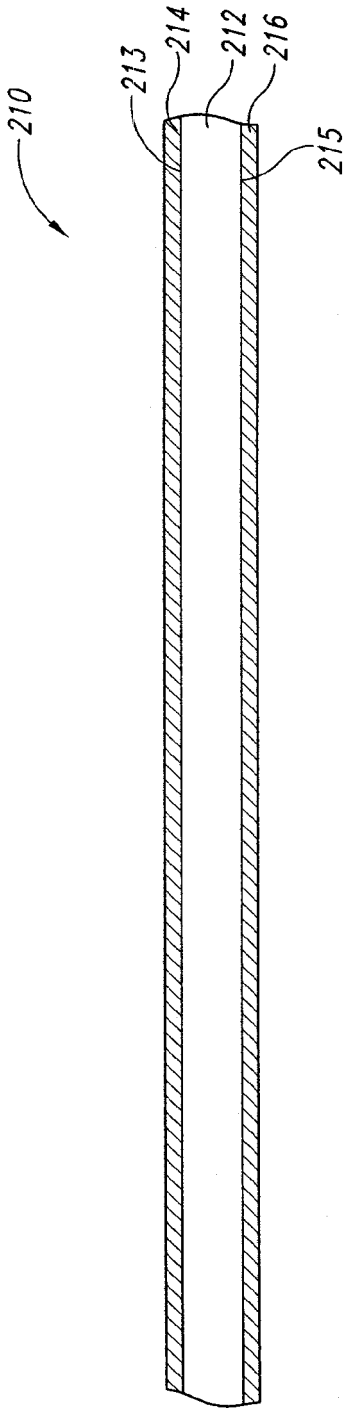
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Fig. 2A

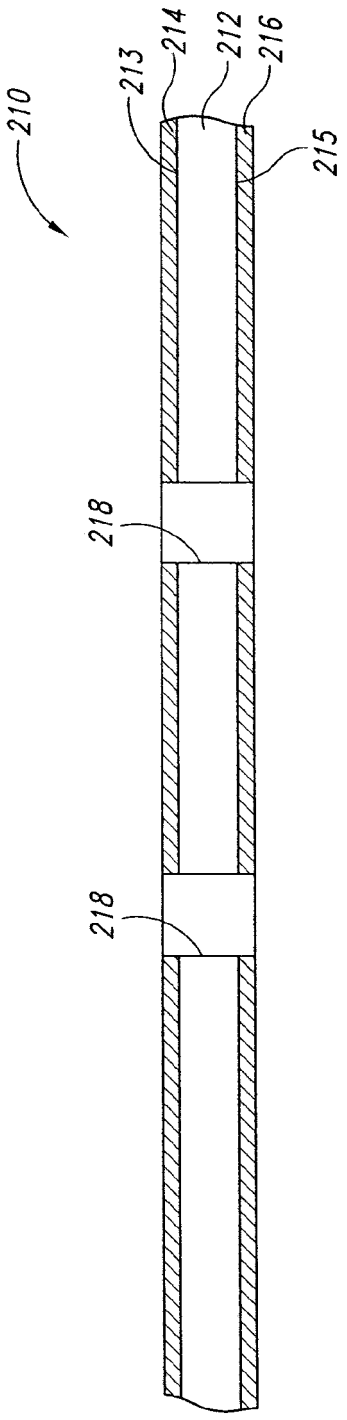
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Fig. 2B

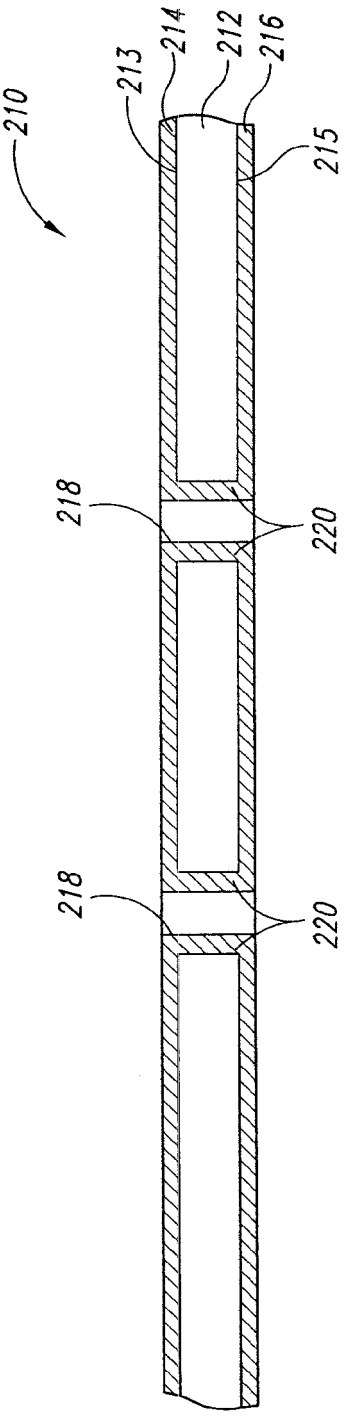
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Fig. 2C

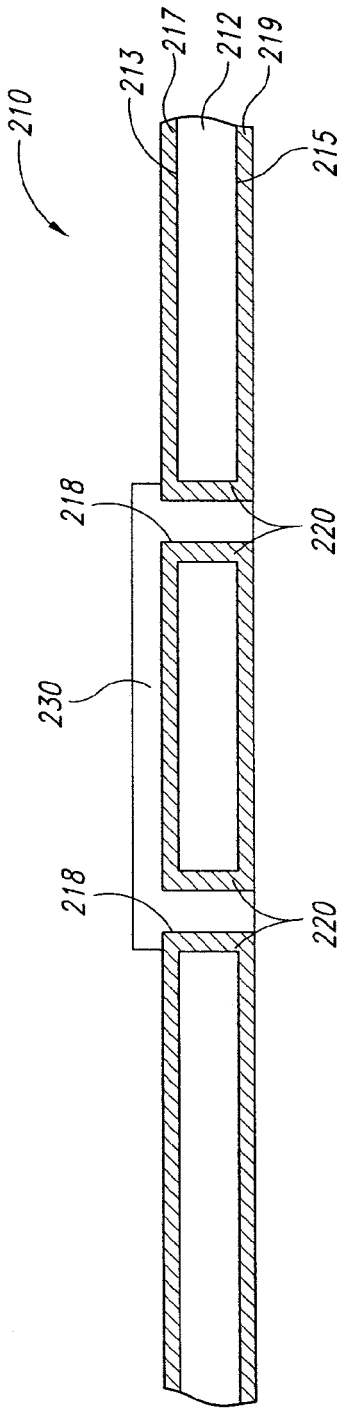
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Fig. 2D

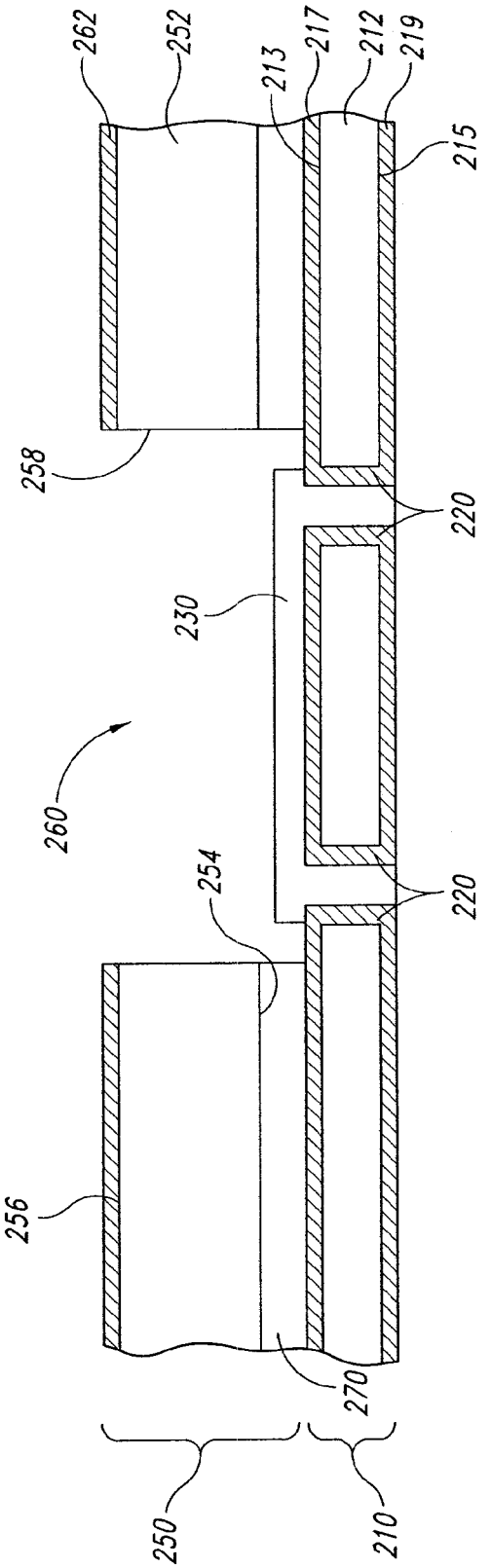
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Fig. 2E

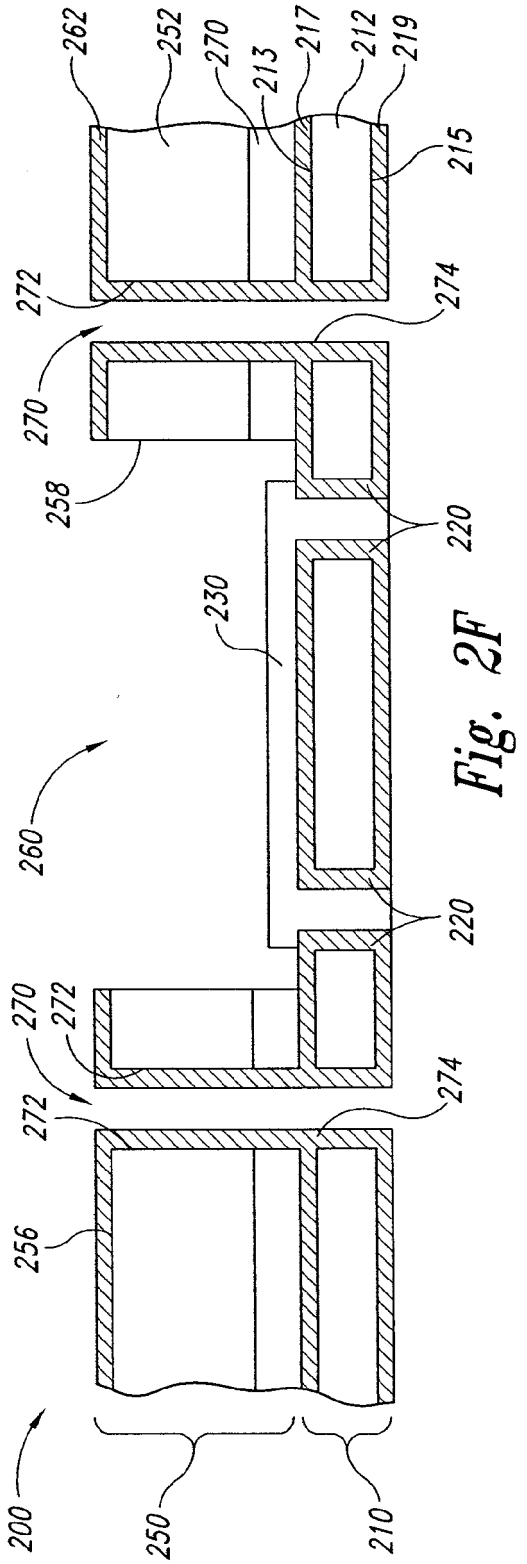
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Fig. 2F

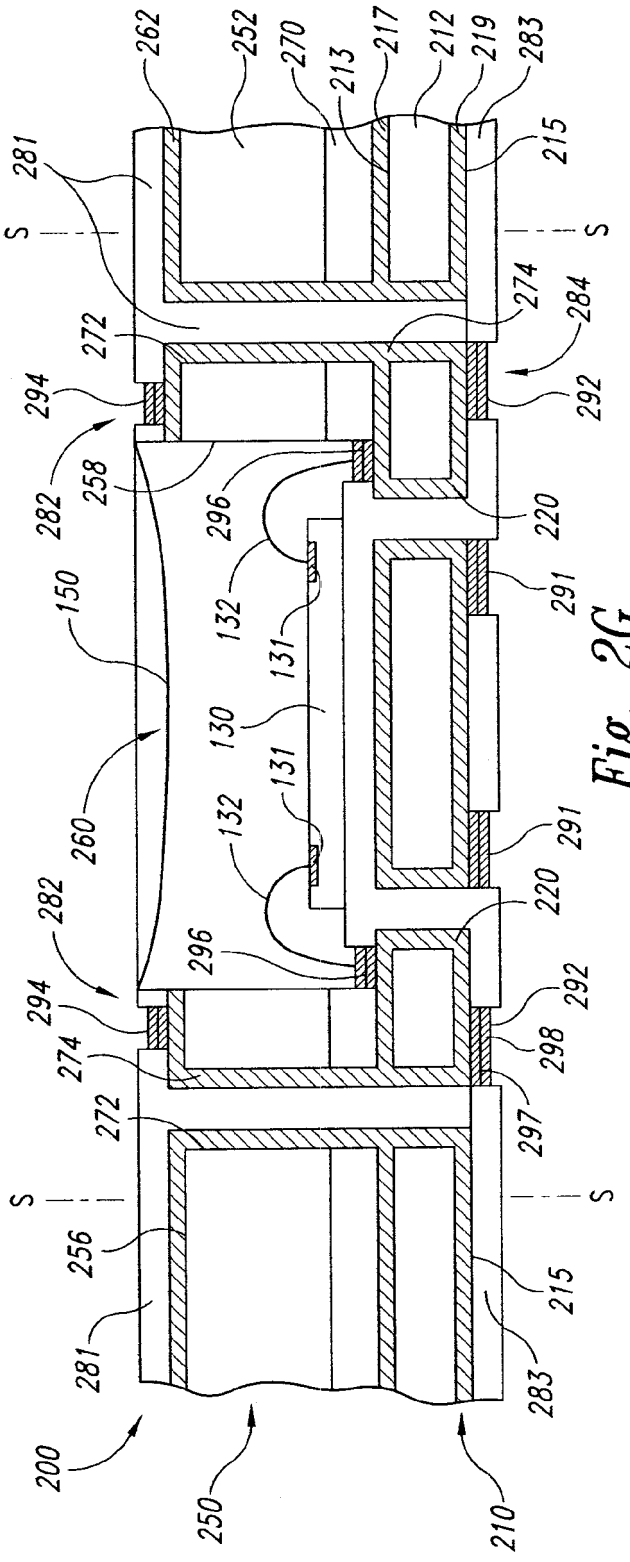
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Fig. 2G

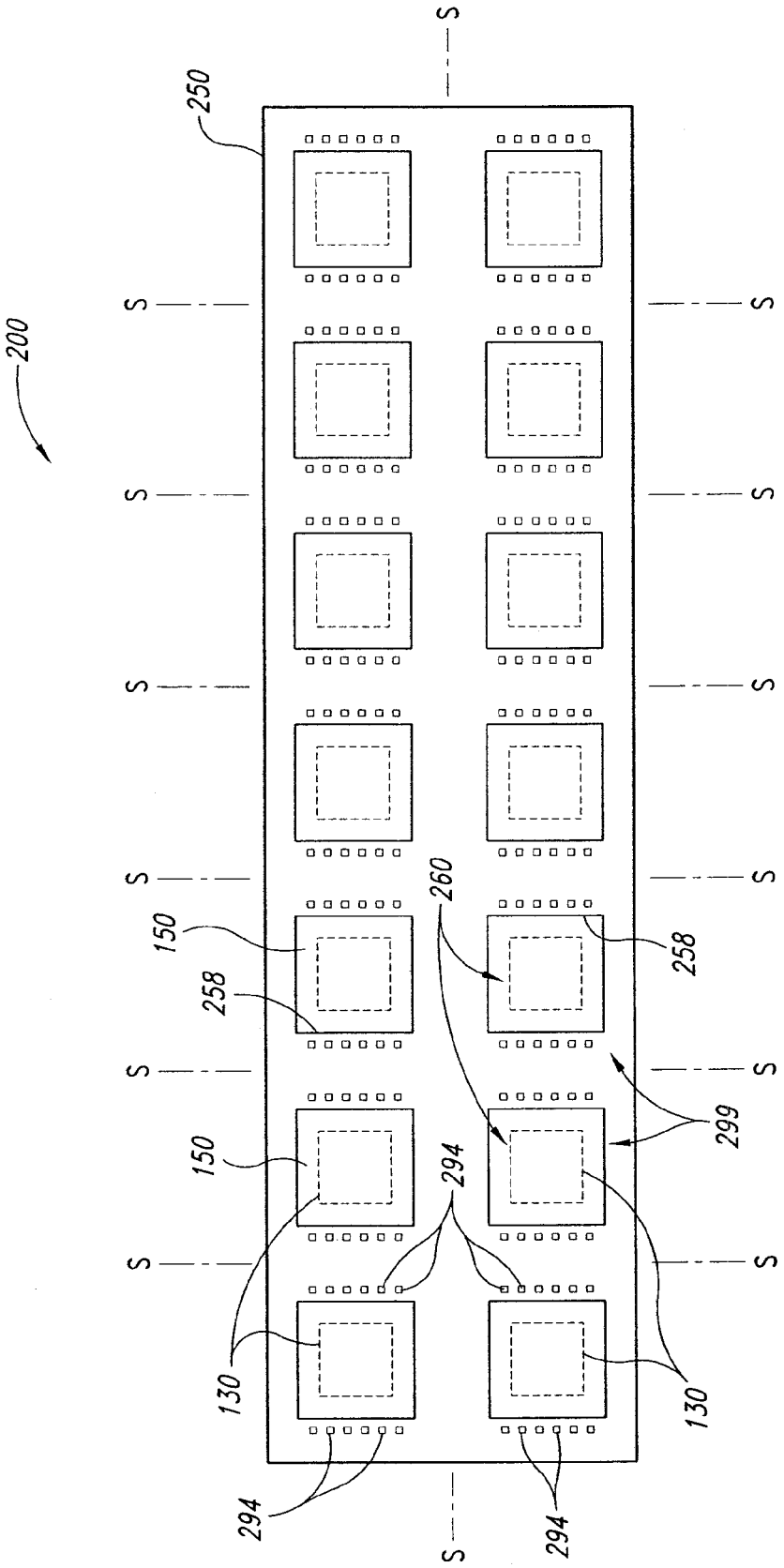

Fig. 2H

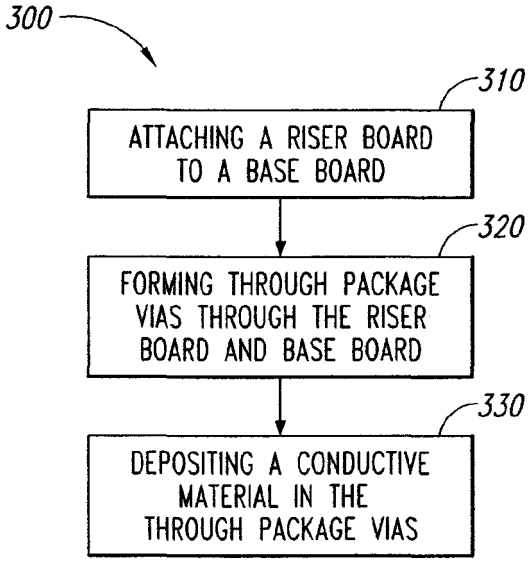
300
310
ATTACHING A RISER BOARD TO A BASE BOARD
320
FORMING THROUGH PACKAGE VIAS THROUGH THE RISER BOARD AND BASE BOARD
330
DEPOSITING A CONDUCTIVE MATERIAL IN THE THROUGH PACKAGE VIAS

Fig. 3A

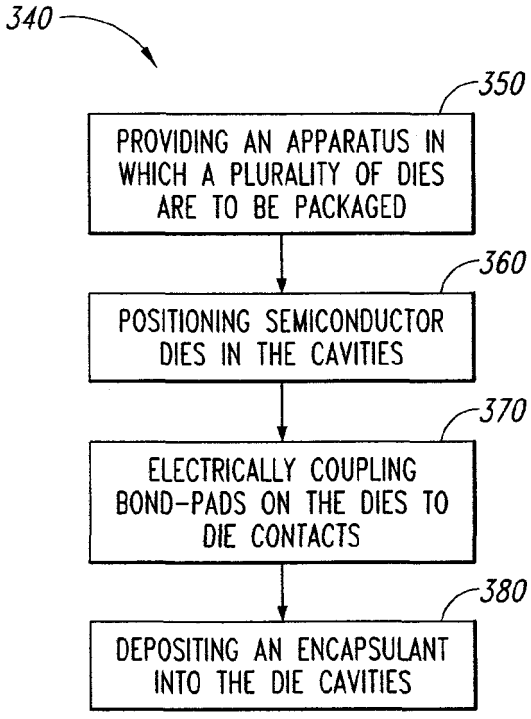
340
350
PROVIDING AN APPARATUS IN WHICH A PLURALITY OF DIES ARE TO BE PACKAGED
360
POSITIONING SEMICONDUCTOR DIES IN THE CAVITIES
370
ELECTRICALLY COUPLING BOND-PADS ON THE DIES TO DIE CONTACTS
380
DEPOSITING AN ENCAPSULANT INTO THE DIE CAVITIES

Fig. 3B

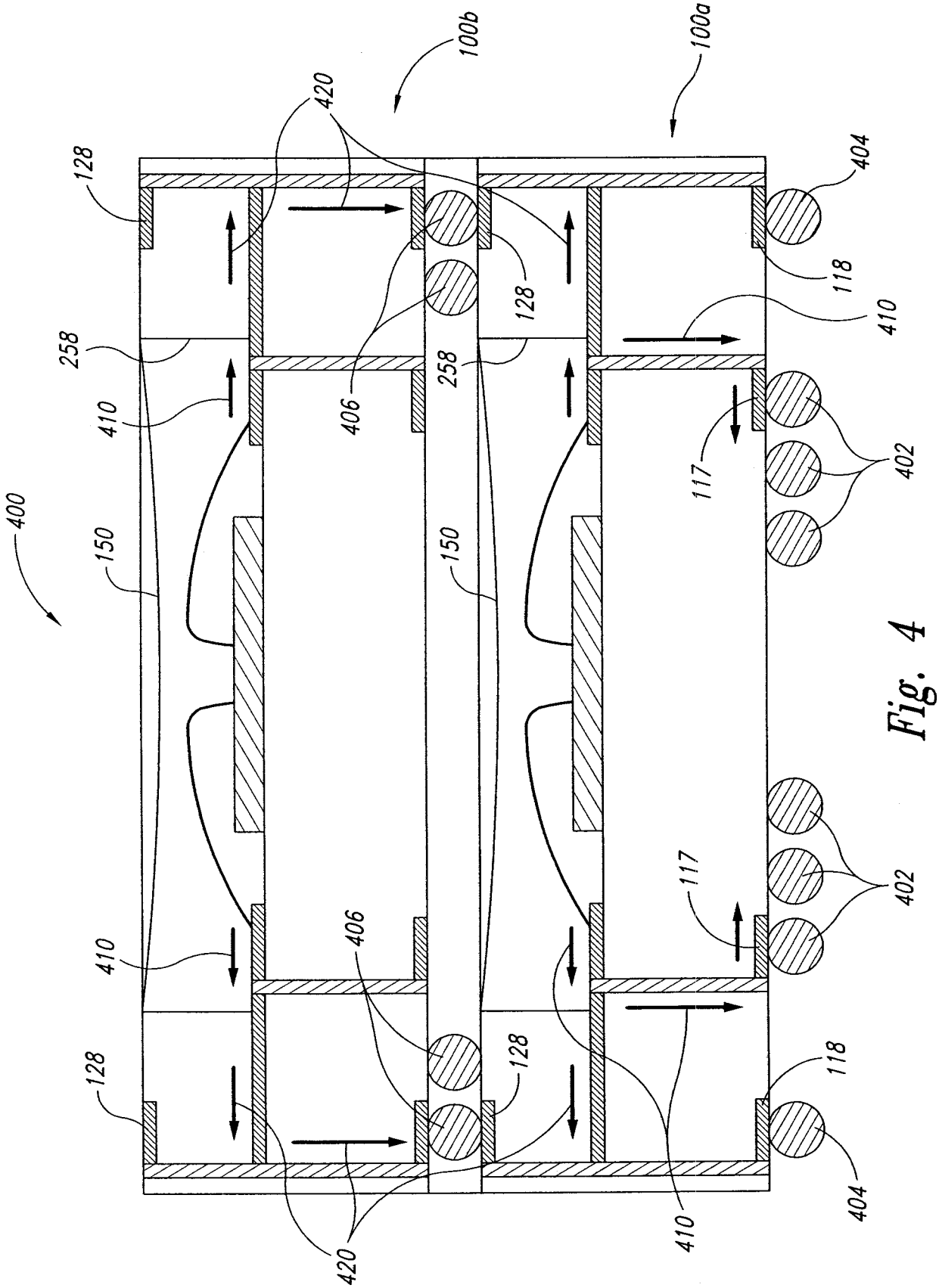

Fig. 4

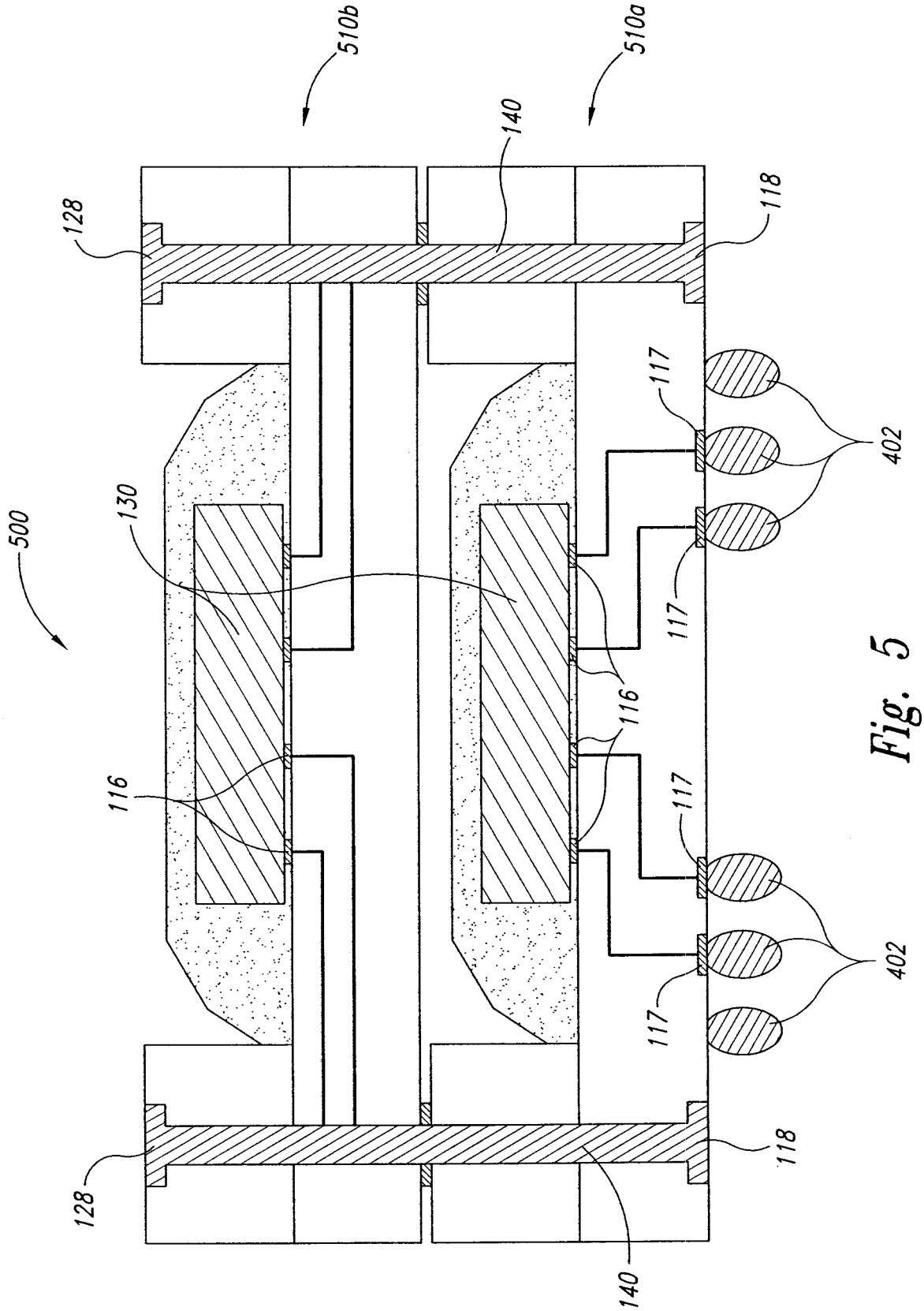
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Fig. 5

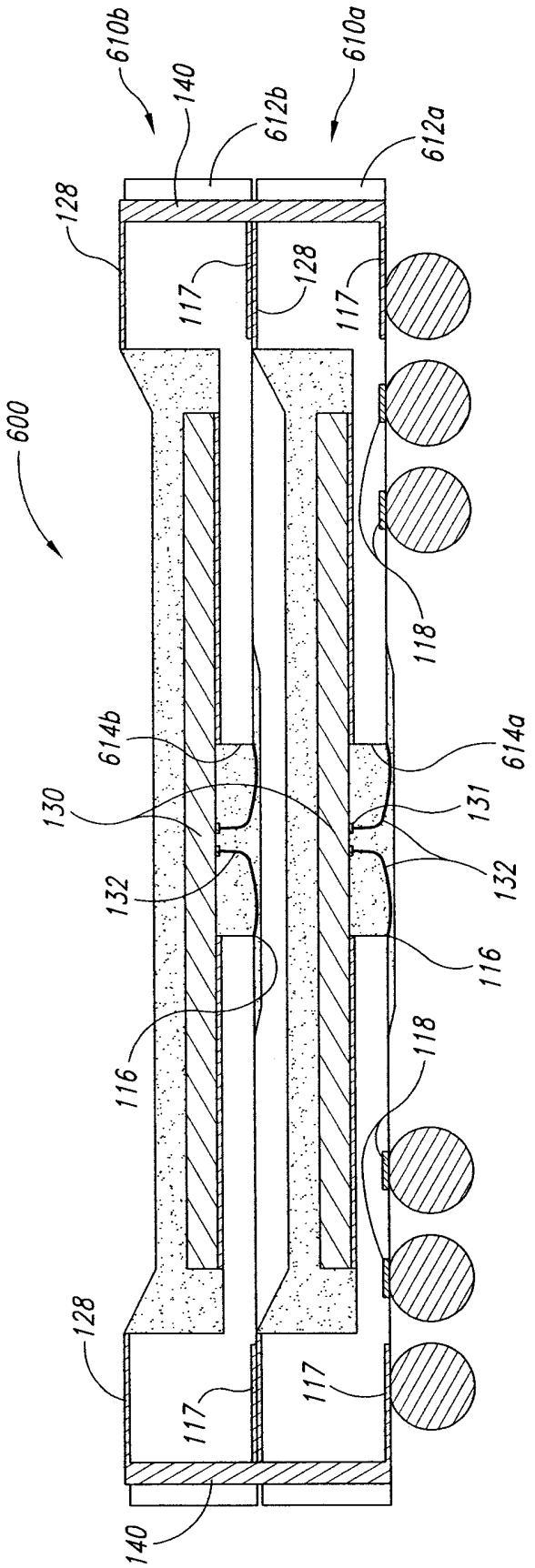
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Fig. 6

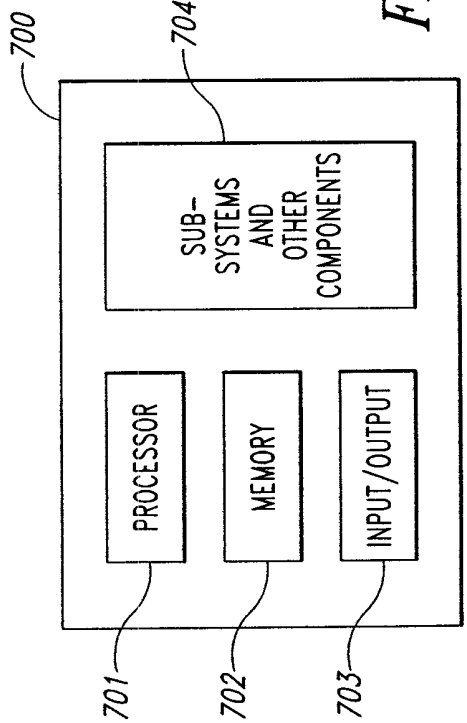
700
704
SUB-SYSTEMS AND OTHER COMPONENTS
PROCESSOR
MEMORY
INPUT/OUTPUT
701
702
703

Fig. 7

REFERENCES CITED IN THE DESCRIPTION

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