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(54) **SURFACE TREATMENT OF A SEMICONDUCTOR LIGHT EMITTING DEVICE**

OBERFLÄCHENBEHANDLUNG EINER LICHEMITTIERENDEN HALBLEITERVORRICHTUNG

TRAITEMENT DE SURFACE D'UN DISPOSITIF ÉLECTROLUMINESCENT À SEMI-CONDUCTEURS

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Description

BACKGROUND

5 FIELD OF INVENTION

[0001] The present invention relates to controlling the amount of flux emitted by a semiconductor light emitting device by treating a surface of the device.

10 DESCRIPTION OF RELATED ART

[0002] Semiconductor light-emitting devices including light emitting diodes (LEDs), resonant cavity light emitting diodes (RCLEDs), vertical cavity laser diodes such as surface-emitting lasers (VCSELs), and edge emitting lasers are among the most efficient light sources currently available. Materials systems currently of interest in the manufacture of high-brightness light emitting devices capable of operation across the visible spectrum include Group III-V semiconductors, particularly binary, ternary, and quaternary alloys of gallium, aluminum, indium, and nitrogen, also referred to as III-nitride materials. Typically, III-nitride light emitting devices are fabricated by epitaxially growing a stack of semiconductor layers of different compositions and dopant concentrations on a sapphire, silicon carbide, III-nitride, or other suitable substrate by metal-organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), or other epitaxial techniques. The stack often includes one or more n-type layers doped with, for example, Si, formed over the substrate, one or more light emitting layers in an active region formed over the n-type layer or layers, and one or more p-type layers doped with, for example, Mg, formed over the active region. Electrical contacts are formed on the n- and p-type regions.

[0003] Fig. 1 illustrates a light emitting device described in more detail in US 7,256,483 B2.

[0004] To form the device of Fig. 1, a conventional LED is formed on a growth substrate. Each LED die includes n-type layers 16, an active layer 18, and p-type layers 20. A metal (metallization layer plus bonding metal) 24 contacts the p-layer. Portions of the p-layer 20, active layer 18, and possibly metal 24 are etched away during the LED forming process, and metal 50 contacts the n-layer 16 on the same side as the p-contact metal 24. An underfill material 52 may be deposited in the voids beneath the LED to reduce thermal gradients across the LED, add mechanical strength to the attachment, and prevent contaminants from contacting the LED material. The metallization layers 50 and 24 are bonded to metal contact pads 22A and 22B, respectively, on a package substrate 12. The package substrate 12 may be formed of the electrically insulating material AlN, with metal contact pads 22A and 22B connected to solderable electrodes 26A and 26B using vias 28A and 28B and/or metal traces. The growth substrate is removed, then the light-emitting top surface of the LED (n-layer 16) is roughened for increased light extraction. For example, layer 16 may be photo-electrochemically etched using a KOH solution.

[0005] T. Fujii et al. disclose, in: "Increase in the extraction efficiency of GaN-based light-emitting diodes via surface roughening", Applied Physics Letters, Vol. 84, No. 6, 9 February 2004, pages 855-857, that roughened surfaces of LEDs provide substantial improvement in light extraction efficiency. By using laser lift-off technique followed by an anisotropic etching process to roughen the surface, an n-side-up GaN-based LED with a "cone-like" surface was fabricated. The output power of an optimally roughened surface LED showed a twofold to threefold increase compared to that of an LED before surface roughening.

[0006] US 2006/0202219 A1, US 2010/0052000 A1 and US 2010/0248407 A1 disclose further semiconductor light emitting devices also having roughened light-extraction surfaces.

SUMMARY

[0007] The present invention is directed, in accordance with the appended claim 1, to a method of manufacturing a semiconductor light emitting device where the maximum amount of flux from the device may be controlled.

[0008] According to the present invention, a method of manufacturing a semiconductor light emitting device includes: roughening a light extraction surface of the semiconductor light emitting device to form a plurality of peaks on the surface and, after said roughening, treating the roughened light extraction surface to flatten tops of the plurality of peaks in order to reduce an amount of flux extracted from the semiconductor light emitting device. The semiconductor light emitting device includes a light emitting layer. The light extraction surface includes a surface from which light is extracted from the semiconductor light emitting device.

[0009] Advantageous, further embodiments of the present invention are the object of the appended dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010]

- Fig. 1 illustrates a prior art LED from which the growth substrate has been removed.
 Fig. 2 illustrates the behavior of light at an interface between air and III-nitride material.
 Fig. 3 illustrates the behavior of light at an interface between air and roughened III-nitride material.
 Fig. 4 illustrates the behavior of light at an interface between air and III-nitride material treated according to embod-
 5 iments of the invention.
 Fig. 5 is a cross sectional view of a device manufactured according to embodiments of the invention.
 Fig. 6 illustrates a III-nitride surface after roughening.
 Fig. 7 illustrates a III-nitride surface after treatment according to embodiments of the invention.
 Fig. 8 illustrates light output as a function of treatment time for plasma treatment at low power and at higher power.
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DETAILED DESCRIPTION

[0011] The difference in index of refraction between III-nitride material and air creates total internal reflection at a smooth interface, as illustrated in Fig. 2. At a smooth interface between III-nitride material 30, which has an index of
 15 refraction of about 2.4, and air 32, which has an index of refraction of about 1, light 34 emitted at small angles relative to the growth direction escape the III-nitride material. Light 36 emitted at glancing angles is totally internally reflected at the interface and may be lost to absorption within the device.

[0012] In order to improve extraction from the device, the top surface of the III-nitride material may be roughened as described above in reference to Fig. 1. The behavior of light 38 emitted at a glancing angle toward a roughened interface
 20 is illustrated in Fig. 3. Because of the rough surface of III-nitride material 30, light emitted at a glancing angle relative to the growth direction encounters the surface of the III-nitride material 30 at an angle that allows it to escape into air 32.

[0013] However, roughening of the III-nitride surface by photoelectrochemical (PEC) etching is difficult to control. For most practical purposes, extraction of light can only be maximized with PEC etching, as the amount of extraction is difficult to adjust. Some applications, such as for example automotive applications, require a particular maximum flux
 25 that may not be exceeded. Modern, high-power LEDs with roughened top surfaces as described above may be too bright for these applications.

[0014] In accordance with embodiments of the invention, the roughened surface of a semiconductor light emitting device is treated to reduce the amount of flux extracted from the LED. The treatment creates a flatten top surface that reintroduces some total internal reflection at the interface or that causes absorption, as illustrated in Fig. 4. Roughening
 30 forms peaks as illustrated in Fig. 3. Post-roughening treatment according to embodiments of the invention flattens the tops of those peaks 44, as illustrated in Fig. 4. Glancing angle light striking the steep sides 42 of the peaks may be extracted from the III-nitride material 30 into the air 32. Glancing angle light 40 striking the flattened tops 44 may undergo total internal reflection, as illustrated. Internally reflected light may be absorbed.

[0015] Fig. 5 illustrates a semiconductor light emitting device manufactured according to embodiments of the invention. Though in the discussion below the semiconductor light emitting device is a III-nitride LED that emits blue or UV light, semiconductor light emitting devices besides LEDs such as laser diodes and semiconductor light emitting devices made from other materials systems such as other III-V materials, III-phosphide, III-arsenide, II-VI materials, ZnO, or Si-based materials may be used.
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[0016] The device illustrated in Fig. 5 may be formed by first growing a semiconductor structure on a growth substrate (not shown in Fig. 5), as is known in the art. The growth substrate may be any suitable substrate such as, for example, sapphire, SiC, Si, GaN, or composite substrates. The semiconductor structure includes a light emitting or active region 47A, 47B sandwiched between n- and p-type regions 46 and 48A, 48B. An n-type region 46 may be grown first and may include multiple layers of different compositions and dopant concentration including, for example, preparation layers such as buffer layers or nucleation layers, and/or layers designed to facilitate removal of the growth substrate, which
 45 may be n-type or not intentionally doped, and n- or even p-type device layers designed for particular optical, material, or electrical properties desirable for the light emitting region to efficiently emit light. A light emitting or active region 47 is grown over the n-type region 46. Examples of suitable light emitting regions include a single thick or thin light emitting layer, or a multiple quantum well light emitting region including multiple thin or thick light emitting layers separated by barrier layers. A p-type region 48A, 48B may then be grown over the light emitting region 47. Like the n-type region 46, the p-type region 48A, 48B may include multiple layers of different composition, thickness, and dopant concentration, including layers that are not intentionally doped, or n-type layers. The total thickness of all the semiconductor material in the device is less than 10 μm in some embodiments and less than 6 μm in some embodiments.
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[0017] A reflective metal p-contact 80A, 80B is formed on the p-type region 48A, 48B. The semiconductor structure is then patterned by standard photolithographic operations and etched to remove a portion of the entire thickness of the p-type region and a portion of the entire thickness of the light emitting region, to form at least one mesa which reveals a surface of the n-type region on which a metal n-contact 82A is formed. The n-contacts may be distributed, as illustrated by the three n-contacts 82A-82C illustrated in Fig. 5, or a single n-contact may be formed. The n- and p-contacts 82 and 80 may be electrically isolated by a gap 54A-54D, which may be filled with air, ambient gas, or a solid material such as
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a dielectric or an oxide of silicon. The mesa and p- and n-contacts may be formed in any suitable manner. Forming the mesa and p- and n-contacts is well known to a person of skill in the art. In the regions between devices on a wafer of devices, the semiconductor structure is etched down to an insulating layer, which may be an insulating semiconductor layer that is part of the semiconductor structure, or the growth substrate. The p- and n-contacts may be redistributed by a stack of insulating layers and metals as is known in the art to form at least two large electrical pads. One of the electrical pads is electrically connected to the p-type region of the semiconductor structure and the other of the electrical pads is electrically connected to the n-type region of the semiconductor structure. Electrical pads may be any suitable conductive material including, for example, copper, gold, and alloys. The electrical pads are electrically isolated from each other by a gap which may be filled with an insulating material such as a dielectric, air, or other ambient gas. The stack of layers used to redistribute the contacts and the electrical pads is well known in the art and is not illustrated in Fig. 5.

[0018] The semiconductor structure is attached to a mount 56 such that contacts 80A, 80B and 82A-82C are between the mount and the semiconductor structure. In some embodiments, a wafer of devices is diced into individual devices or groups of devices, then the diced devices or groups are attached to a mount, as described above in reference to Fig. 1. In these embodiments, the mount is often larger than the individual devices or groups of devices. In some embodiments, a wafer of devices is attached to a mount on a wafer scale, then after further processing, the wafer of devices and the mount are diced at the same time into individual devices or groups of devices. In these embodiments, the mount is the same size as the individual devices or groups of devices. Dicing can be performed by any suitable method such as scribe-and-break with a laser scribe or sawing and is well known in the art. The mount may be any suitable structure that mechanically supports the semiconductor structure, including, for example, a ceramic mount or wafer, a silicon mount or wafer, for example with conductive vias, or thick metal bonding pads which mechanically support the semiconductor structure, formed by, for example, plating. In some embodiments, mount 56 is a self-supporting structure suitable to attach the semiconductor light emitting device to a substrate such as a PC (printed circuit) board. For example, the surface of mount 56 opposite the semiconductor structure (the bottom surface of mount 56 in Fig. 5) may be reflow-solderable.

[0019] The growth substrate is removed by any suitable technique. For example, the growth substrate may be removed by laser lift-off, etching, mechanical techniques such as grinding, or a combination of techniques. The surface 58 of the semiconductor structure exposed by removing the growth substrate, typically a surface of n-type region 46, may be optionally thinned and, according to embodiments of the invention, is roughened, for example by PEC etching. Fig. 6 illustrates a surface 58 roughened by PEC etching.

[0020] The surface 58 of Fig. 6 is then treated to flatten tops of the peaks in order to reduce extraction, as illustrated in Fig. 7. In some embodiments, surface 58 is treated with plasma, which flattens the peaks formed by PEC etching, as illustrated in Fig. 7. Any suitable standard commercially-available plasma etching and/or cleaning system may be used. The plasma used may be any suitable plasma, including, for example, Ar, O, and mixtures. The spike-type (peak) features illustrated in Fig. 6 are flattened by typically plasma treatment in Fig. 7, which leads to more total internal reflection at the interface, which reduces extraction from the device. Plasma treatment may be either physical (i.e. sputter etching) or chemical (i.e. chemical etching) or a combination of physical and chemical etching.

[0021] Fig. 8 illustrates light output as a function of plasma treatment time for a surface of a III-nitride device treated with plasma at 500 W and at 600 W. The four points on the left side of the figure illustrate light output for a surface treated with plasma at 500 W and the four points on the right side of the figure illustrate light output for a surface treated with plasma at 600 W. Fig. 8 illustrates that the light output or amount of extraction is roughly linearly proportional to the treatment time. The longer the surface is treated with plasma at either energy, the less light is extracted from the surface. In addition, the reduction in extraction is proportional to the power - treatment at higher power for a given time reduced extraction more than treatment at lower power for the same time. The inventors have observed that light output can be reduced by 30% of the maximum value (i.e. light output from a roughened surface without any treatment).

[0022] The following table compares a roughened surface with no post-roughening plasma treatment with a roughened surface treated for 60 s with plasma at 600 W. R_a is the mean roughness of the surface and R_{max} is the maximum height of surface features. Light output is given in arbitrary units.

Surface	Light Output	R_a (nm)	R_{max} (nm)
No treatment	420	185.8	1598
600 W treatment, 60 s	287.28	133.4	1049

[0023] As illustrated in the above table, both light output and surface roughness are reduced for a treated surface. For example, as a result of treatment according to embodiments of the invention, the mean surface roughness may be reduced by at least 10% in some embodiments, by at least 20% in some embodiments, and by at least 30% in some embodiments. As a result of treatment according to embodiments of the invention, the maximum height of surface

features may be reduced by at least 20% in some embodiments, by at least 30% in some embodiments, and by at least 40% in some embodiments.

[0024] After post-roughening treatment as described above, one or more optional structures such as filters, lenses, dichroic materials, or wavelength converting materials may be formed over the treated surface. A wavelength converting material may be formed such that all or only a portion of the light emitted by the light emitting device and incident on the wavelength converting material may be converted by the wavelength converting material. Unconverted light emitted by the light emitting device may be part of the final spectrum of light, though it need not be. Examples of common combinations include a blue-emitting LED combined with a yellow-emitting wavelength converting material, a blue-emitting LED combined with green- and red-emitting wavelength converting materials, a UV-emitting LED combined with blue- and yellow-emitting wavelength converting material, and a UV-emitting LED combined with blue-, green-, and red-emitting wavelength converting materials. Wavelength converting materials emitting other colors of light may be added to tailor the spectrum of light emitted from the device. The wavelength converting material may be conventional phosphor particles, organic semiconductors, II-VI or III-V semiconductors, II-VI or III-V semiconductor quantum dots or nanocrystals, dyes, polymers, or materials such as GaN that luminesce. Phosphor particles may have an average diameter between 5 and 50 μm in some embodiments. Any suitable phosphor may be used, including but not limited to garnet-based phosphors such as $\text{Y}_3\text{Al}_5\text{O}_{12}:\text{Ce}$ (YAG), $\text{Lu}_3\text{Al}_5\text{O}_{12}:\text{Ce}$ (LuAG), $\text{Y}_3\text{Al}_{5-x}\text{Ga}_x\text{O}_{12}:\text{Ce}$ (YAIGaG), $(\text{Ba}_{1-x}\text{Sr}_x)\text{SiO}_3:\text{Eu}$ (BOSE), and nitride-based phosphors such as $(\text{Ca},\text{Sr})\text{AlSiN}_3:\text{Eu}$ and $(\text{Ca},\text{Sr},\text{Ba})_2\text{Si}_5\text{N}_8:\text{Eu}$.

[0025] Having described the invention in detail, those skilled in the art will appreciate that, given the present disclosure, modifications may be made to the invention without departing from the scope of the invention as defined by the appended claims only.

Claims

1. A method of manufacturing a semiconductor light emitting device comprising:

roughening a light extraction surface (58) of the semiconductor light emitting device to form a plurality of peaks on the surface, the semiconductor light emitting device comprising a light emitting layer (47) and the light extraction surface comprising a surface from which light is extracted from the semiconductor light emitting device; **characterised by:**

after roughening, treating the roughened light extraction surface to flatten tops (44) of the plurality of peaks in order to reduce an amount of flux extracted from the semiconductor light emitting device.

2. The method of claim 1 wherein treating the roughened light extraction surface comprises treating the surface with plasma.

3. The method of claim 2 wherein the plasma comprises at least one of Ar and O.

4. The method of claim 1 further comprising:

growing the semiconductor light emitting device on a growth substrate;
attaching the semiconductor light emitting device to a mount (56); and
removing the growth substrate;
wherein the roughened surface is a surface revealed by removing the growth substrate.

5. The method of claim 1 further comprising disposing a wavelength converting material over the treated surface.

Patentansprüche

1. Verfahren zur Herstellung einer lichtemittierenden Halbleitervorrichtung, umfassend:

Aufrauen einer Lichtextraktionsfläche (58) der lichtemittierenden Halbleitervorrichtung, um eine Vielzahl von Spitzen auf der Fläche zu bilden, wobei die lichtemittierende Halbleitervorrichtung eine lichtemittierende Schicht (47) umfasst, und die Lichtextraktionsfläche eine Fläche umfasst, von der Licht von der lichtemittierenden Halbleitervorrichtung extrahiert wird;

dadurch gekennzeichnet, das

nach dem Aufrauen die aufgeraute Lichtextraktionsfläche behandelt wird, um obere Seiten (44) der Vielzahl

von Spitzen abzufachen, um eine Flussmenge zu reduzieren, die aus der lichtemittierenden Halbleitervorrichtung extrahiert wird.

- 5
2. Verfahren nach Anspruch 1, wobei das Behandeln der aufgerauten Lichtextraktionsfläche das Behandeln der Fläche mit Plasma umfasst.
 3. Verfahren nach Anspruch 2, wobei das Plasma mindestens eines von Ar und O umfasst.
 - 10 4. Verfahren nach Anspruch 1, weiter umfassend:
Aufbauen der lichtemittierenden Halbleitervorrichtung auf einem Wachstumssubstrat;
Befestigen der lichtemittierenden Halbleitervorrichtung auf einer Halterung (56); und
Entfernen des Wachstumssubstrats;
wobei die aufgeraute Fläche eine Fläche ist, die durch Entfernen des Wachstumssubstrats aufgedeckt wurde.
 - 15 5. Verfahren nach Anspruch 1, weiter umfassend das Anordnen eines Wellenlängenumwandlungsmaterials über der behandelten Fläche.

20 **Revendications**

1. Procédé de fabrication d'un dispositif électroluminescent à semi-conducteur comprenant :
25 la rugosification d'une surface d'extraction de lumière (58) du dispositif électroluminescent à semi-conducteur pour former une pluralité de pics sur la surface, le dispositif électroluminescent à semi-conducteur comprenant une couche électroluminescente (47) et la surface d'extraction de lumière comprenant une surface depuis laquelle la lumière est extraite du dispositif électroluminescent à semi-conducteur ;
caractérisé par :
après la rugosification, le traitement de la surface d'extraction de la lumière brute pour aplanir les sommets (44)
30 de la pluralité de pics afin de réduire une quantité de flux extraite du dispositif électroluminescent à semi-conducteur.
2. Procédé selon la revendication 1, dans lequel le traitement de la surface d'extraction de lumière rugosifiée comprend le traitement de la surface avec un plasma.
- 35 3. Procédé selon la revendication 2, dans lequel le plasma comprend au moins l'un parmi Ar et O.
4. Procédé selon la revendication 1, comprenant en outre :
40 la croissance du dispositif électroluminescent à semi-conducteur sur un substrat de croissance ;
la fixation du dispositif électroluminescent à semi-conducteur à une monture (56) ; et
le retrait du substrat de croissance ;
dans lequel la surface rugosifiée est une surface révélée par le retrait du substrat de croissance.
- 45 5. Procédé selon la revendication 1, comprenant en outre l'étape de disposition d'un matériau de conversion de longueur d'onde sur la surface traitée.

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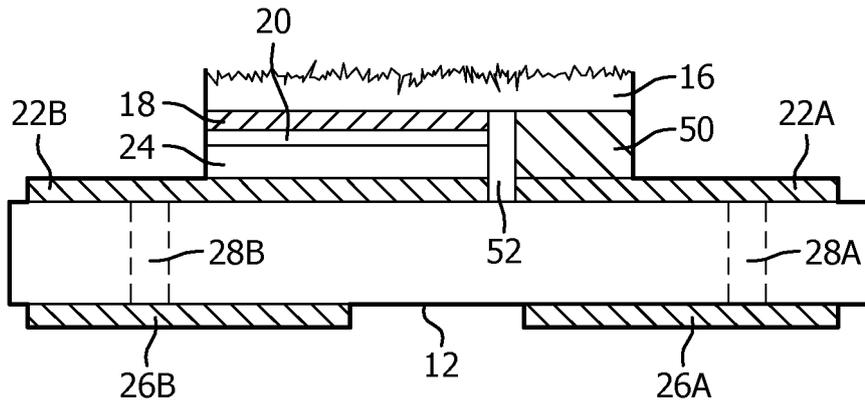


FIG. 1

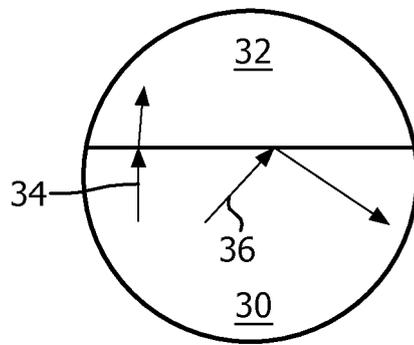


FIG. 2

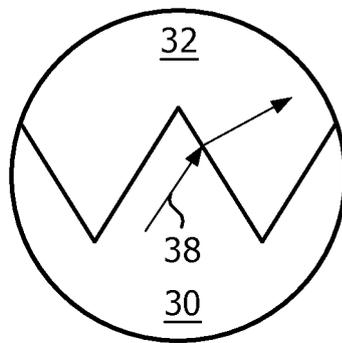


FIG. 3

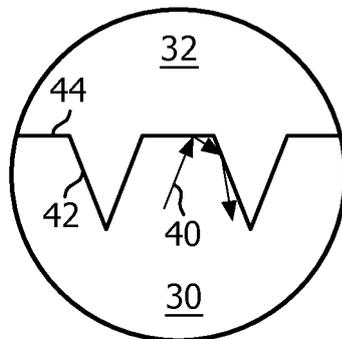


FIG. 4

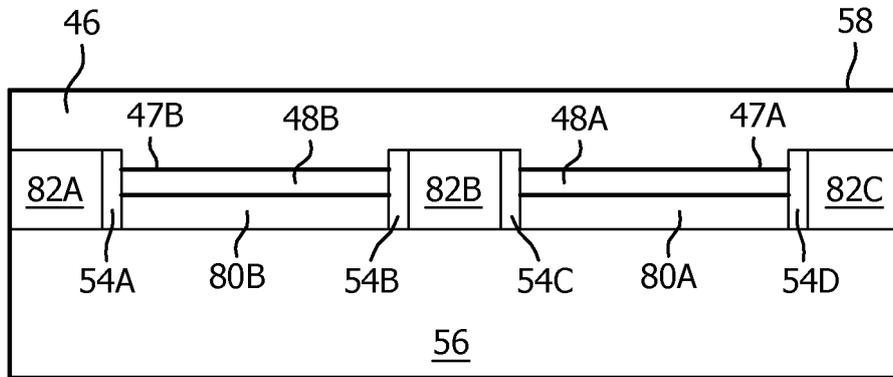


FIG. 5



FIG. 6



FIG. 7

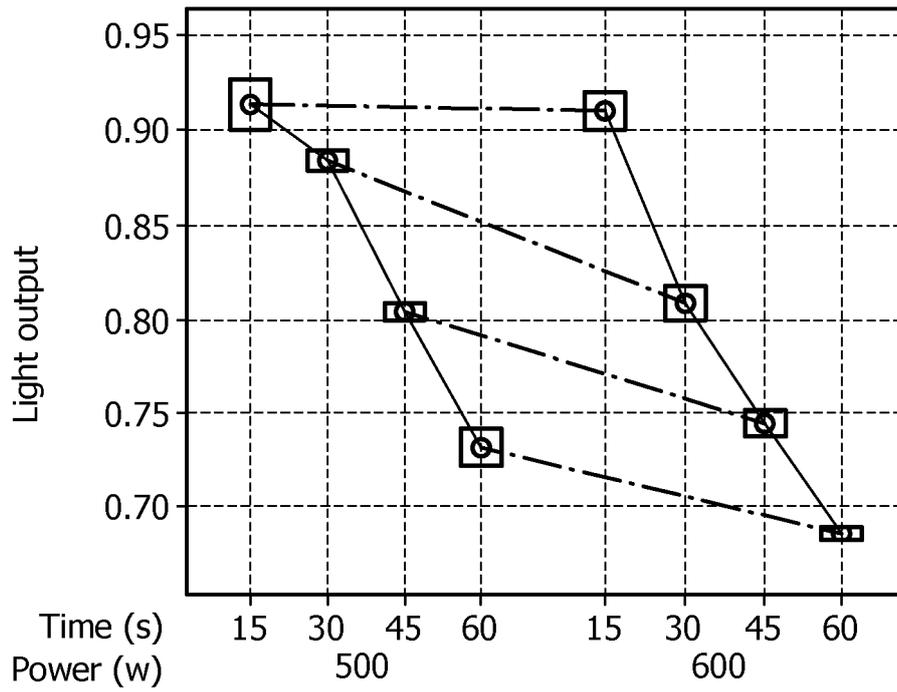


FIG. 8

REFERENCES CITED IN THE DESCRIPTION

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