(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 3 525 351 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
14.08.2019 Bulletin 2019/33

(51) Int Cl.:
H03M 3/00 *(2006.01)* *H02M 3/335* *(2006.01)*

(21) Application number: **18194219.4**

(22) Date of filing: **13.09.2018**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
KH MA MD TN

(30) Priority: **13.02.2018 KR 20180017477**

(71) Applicants:
- **Hyundai Motor Company**
  Seoul 06797 (KR)
- **Kia Motors Corporation**
  Seoul 06797 (KR)

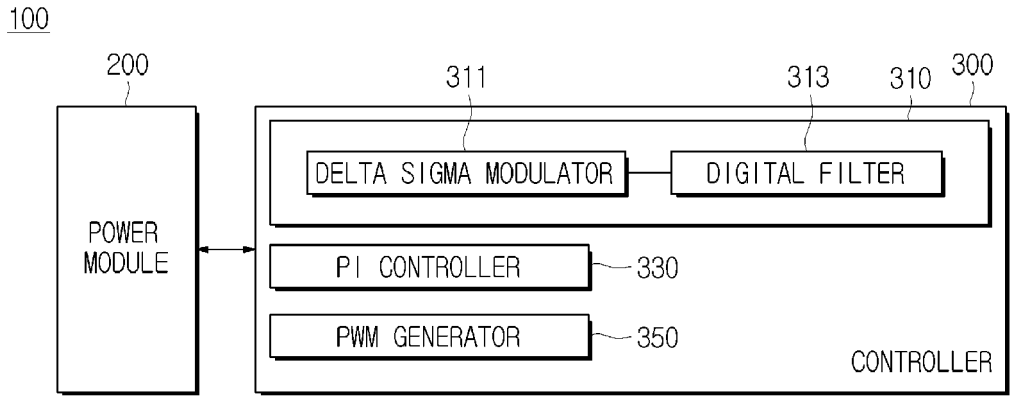
(72) Inventors:
- **CHUN, ShinHye**
  18280 Gyeonggi-do (KR)
- **IHM, Hyung Bin**
  18280 Gyeonggi-do (KR)

(74) Representative: **Viering, Jentschura & Partner mbB**
Patent- und Rechtsanwälte
Am Brauhaus 8
01099 Dresden (DE)

(54) ANALOG TO DIGITAL (A/D) CONVERTER AND POWER CONVERSION APPARATUS HAVING THE SAME

(57) A power conversion apparatus can include: a power module configured to transfer an analog sensing signal corresponding to a current of an inductor and a voltage applied at both terminals of a capacitor, and to perform power conversion by driving a power semiconductor with a pulse-width modulation signal; and a controller configured to receive the analog sensing signal from the power module, to convert the analog sensing signal to a digital signal, to generate the pulse-width modulation signal, and to transfer the pulse-width modulation signal to the power module.

FIG. 1



EP 3 525 351 A1

Description

BACKGROUND

1. Technical Field

[0001] The present disclosure relates to an Analog to Digital (A/D) converter and a power conversion apparatus having the same and, more particularly, to an A/D converter to which an A/D conversion method for improving the use efficiency of a logic block is applied, and a power conversion apparatus having the same.

2. Description of the Related Art

[0002] There is a need for high-speed switching of a DC-DC converter (e.g., according to power density, etc.) to reduce the size of the converter.. Power semiconductors, such as SiC and GaN, have been developed to meet this need. However, the ability to increase switching frequency is restrained due to limited resources in digital control using microprocessors.

[0003] In order to overcome the problem, a Field Programmable Gate Array (FPGA) can be used to generate high-speed Pulse Width Modulation (PWM) signals. The FPGA can perform parallel processing, and accordingly, the FPGA can perform tasks simultaneously at high speed.

[0004] However, since the FPGA is still at the stage of growth in industry, the FPGA remains expensive compared to microprocessors allowing multiple-purpose control. Accordingly, a method for efficiently using resources so that required control performance can be achieved with a limited number of logic blocks of a FPGA, without significant increases in cost, is needed.

SUMMARY

[0005] Therefore, it is an aspect of the present disclosure to provide an Analog to Digital (A/D) converter to which an A/D conversion method for improving the use efficiency of a logic block is applied, and a power conversion apparatus having the same.

[0006] Additional aspects of the disclosure will be set forth in part in the description which follows and, in part, will be apparent from the description, or may be learned by practice of the disclosure.

[0007] In accordance with embodiments of the present disclosure, a power conversion apparatus may include: a power module configured to transfer an analog sensing signal corresponding to a current of an inductor and a voltage applied at both terminals of a capacitor, and to perform power conversion by driving a power semiconductor with a pulse-width modulation signal; and a controller configured to receive the analog sensing signal from the power module, to convert the analog sensing signal to a digital signal, to generate the pulse-width modulation signal, and to transfer the pulse-width modulation signal to the power module.

[0008] The controller may include an Analog to Digital (A/D) converter may convert the analog sensing signal to the digital signal through a delta sigma modulation method.

[0009] The A/D converter may include: a delta sigma modulator may convert the analog sensing signal to the digital signal by converting an analog input signal to a 1-bit signal through a delta and a sigma signal for integrating the delta, wherein the delta is a difference between the analog input signal and a modulation signal that is feedback of the delta; and a digital filter may smooth the 1-bit signal.

[0010] The digital filter may be a Cascaded Integrator Comb (CIC) filter.

[0011] The delta sigma converter may include: an analog circuit including an adder and an integrator implemented with a register and a capacitor; a comparator may output a signal transferred from the analog circuit as the 1-bit signal; a quantizer configured to oversample the 1-bit signal transferred from the comparator; and an out port configured to RC-filter the oversampled value, and to feed the RC-filtered value back as a delta input.

[0012] The analog circuit may include a first register configured to receive the analog input signal, a capacitor connected to the first register at one end thereof, and a second register connected between the first register and the capacitor at one end thereof.

[0013] The comparator may include a Low Voltage Differential Signaling (LVDS) terminal having a non-inverting input terminal connected to one end of the capacitor as an input terminal.

[0014] The quantizer may include a Delay (D) flipflop including an input terminal connected to an output terminal of the LVDS terminal, a first output terminal connected to the digital filter, and a second output terminal connected to the other end of the second register through the out port.

[0015] When the controller is implemented as a digital controller, the analog circuit may be disposed outside the digital controller, and the comparator, the quantizer, the out port, and the digital filter may be disposed inside the digital controller.

[0016] The digital filter may be with a filter of a predetermined order, including a plurality of integrator stages configured to sequentially provide outputs from a predetermined number of integrators as input of a common Comb filter, and a comb stage configured to generate a comb valid signal in synchronization with a decimation ratio of the plurality of integrator stages and to selectively apply an input according to predetermined criteria for outputs from the plurality of integrator stages when a signal is generated to provide a final output.

[0017] The digital filter may include random access memory (RAM) configured to store an input to or an output from the plurality of integrator stages and the comb stage.

[0018] The RAM selectively stores the outputs from the plurality of integrator stages in corresponding addresses according to criteria set in advance by a valid signal.

[0019] Furthermore, in accordance with an aspect of the present disclosure, an Analog to Digital (A/D) converter includes: a delta sigma modulator configured to convert an analog sensing signal to a digital signal, in such a way to convert an analog input signal to a 1-bit signal through delta which is a difference between the analog input signal and a modulation signal that is feedback of the delta and a sigma signal for integrating the delta; and a digital filter configured to smooth the 1-bit signal.

[0020] The digital filter may be a Cascaded Integrator Comb (CIC) filter.

[0021] The delta sigma modulator may include: an analog circuit including an adder and an integrator implemented with a register and a capacitor; a comparator configured to output a signal transferred from the analog circuit as a 1-bit signal; a quantizer configured to oversample the 1-bit signal transferred from the comparator; and an out port configured to RC-filter the oversampled value, and to feed the RC-filtered value back as a delta input.

[0022] When the A/D converter is implemented as a digital controller, the analog circuit may be disposed outside the digital controller, and the comparator, the quantizer, the out port, and the digital filter may be disposed inside the digital controller.

[0023] The digital filter may be with a filter of a predetermined order, including a plurality of integrator stages configured to sequentially provide outputs from a predetermined number of integrators as input of a common Comb filter, and a comb stage configured to generate a comb valid signal in synchronization with a decimation ratio of the plurality of integrator stages and selectively applying an input according to predetermined criteria for outputs from the plurality of integrator stages when a signal is generated to provide a final output.

[0024] The digital filter may include random access memory (RAM) configured to store an input to or an output from the plurality of integrator stages and the comb stage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] These and/or other aspects of the disclosure will become apparent and more readily appreciated from the following description of the embodiments, taken in conjunction with the accompanying drawings of which:

FIG. 1 is a control block diagram showing a configuration of a power conversion apparatus;

FIG. 2 is a circuit diagram showing a configuration of the A/D converter of FIG. 1;

FIG. 3 is a block diagram showing a configuration of the digital filter of FIG. 2;

FIG. 4 shows a structure of a single CIC filter;

FIGS. 5 and 6 are views for describing a method of controlling a power conversion apparatus; and

FIGS. 7 and 8 are flowcharts illustrating a method of controlling a power conversion apparatus.

[0026] It should be understood that the above-referenced drawings are not necessarily to scale, presenting a somewhat simplified representation of various preferred features illustrative of the basic principles of the disclosure. The specific design features of the present disclosure, including, for example, specific dimensions, orientations, locations, and shapes, will be determined in part by the particular intended application and use environment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0027] Hereinafter, embodiments of the present disclosure will be described in detail with reference to the accompanying drawings. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present disclosure. Further, throughout the specification, like reference numerals refer to like elements.

[0028] Like numbers refer to like elements throughout this specification. This specification does not describe all components of the embodiments, and general information in the technical field to which the present disclosure belongs or overlapping information between the embodiments will not be described. The terms "portion", "module", "element", and "block", as used herein, may be implemented as software or hardware, and according to embodiments, a plurality of "portion", "module", "element", and "block" may be implemented as a single component, or a single "portion", "module", "element", and "block" may include a plurality of components.

[0029] It will be understood that when a component is referred to as being "connected" to another component, it can be directly or indirectly connected to the other component. When a component is indirectly connected to another component, it may be connected to the other component through a wireless communication network.

[0030] Also, it will be understood that when the terms "includes," "comprises," "including," and/or "comprising," when used in this specification, specify the presence of a stated component, but do not preclude the presence or addition of one or more other components.

[0031] In the entire specification, it will also be understood that when an element is referred to as being "on" or "over" another element, it can be directly on the other element or intervening elements may also be present.

[0032] It will be understood that, although the terms first, second, etc. may be used herein to describe various components, these components should not be limited by these terms. These terms are only used to distinguish one component from another.

[0033] It is to be understood that the singular forms "a," "an," and "the" include plural referents unless the context clearly dictates otherwise.

[0034] Additionally, it is understood that one or more of the below methods, or aspects thereof, may be executed by at least one controller. The term "controller" may refer to a hardware device that includes a memory and a processor. The memory is configured to store program instructions, and the processor is specifically programmed to execute the program instructions to perform one or more processes which are described further below. The controller may control operation of units, modules, parts, or the like, as described herein. Moreover, it is understood that the below methods may be executed by an apparatus comprising the controller in conjunction with one or more other components, as would be appreciated by a person of ordinary skill in the art.

[0035] Reference numerals used in operations are provided for convenience of description, without describing the order of the operations, and the operations can be executed in a different order from the stated order unless a specific order is definitely specified in the context.

[0036] Hereinafter, an operation principle and embodiments of the present disclosure will be described with reference to the accompanying drawings.

[0037] FIG. 1 is a control block diagram showing a configuration of a power conversion apparatus.

[0038] As shown in FIG. 1, a power conversion apparatus 100 may include a power module 200 and a controller 300.

[0039] Although not shown in FIG. 1, the power module 200 may include an inductor, a capacitor, a Field Effect Transistor (FET), and a gate driver to transfer an analog sensing signal corresponding to current of the inductor and a voltage applied at both terminals of the capacitor to the controller 300, and drive a power semiconductor with a pulse-width modulation signal transferred from the controller 300, thereby performing power conversion.

[0040] The controller 300 may convert the analog sensing signal received from the power module 200 to a digital signal to generate a pulse-width modulation signal, and transfer the pulse-width modulated signal to the power module 200.

[0041] As shown in FIG. 1, the controller 300 may include an Analog to Digital (A/D) converter 310, a PI controller 330, and a PWM generator 350.

[0042] The A/D converter 310 may convert an analog sensing signal to a digital signal through a delta-sigma modulation method.

[0043] The controller 300 may use sensing information converted to the digital signal by the A/D converter 310 as an input to generate a duty of an output through the PI controller 330 and the PWM generator 350. The duty may be defined as a value obtained by dividing one cycle (one period) of a PWM signal by on-time. The PWM modulation signal drives the FET which is a power semiconductor of the power module 200 to perform power conversion, thereby generating a required voltage or current as an output of the power conversion apparatus.

[0044] The A/D converter 310, the PI controller 330, and the PWM generator 350 may be implemented as a digital controller. However, some components of the A/D converter 310 may be installed outside the digital controller, instead of the inside of the digital controller, which will be described in detail, later. The digital controller may include a Field Programmable Gate Array (FPGA).

[0045] Referring still to FIG. 1, the A/D converter 310 may convert an analog sensing signal to a digital signal, and include a delta sigma modulator 311 for converting an analog input signal to a 1-bit signal through delta (Δ) which is a difference between the analog input signal and a modulation signal that is feedback of the delta and a sigma ($\sum$) signal for integrating the delta Δ, and a digital filter 313 for smoothing the 1-bit signal. The digital filter 313 may be a Cascaded Integrator Comb (CIC) filter.

[0046] The power conversion apparatus 100 may be a DC-DC converter.

[0047] FIG. 2 is a circuit diagram showing a configuration of the A/D converter 310 of FIG. 1.

[0048] As shown in FIG. 2, the delta sigma modulator 311 (e.g., 311 of FIG. 1 and A of FIG. 2) may include an analog circuit including an adder and an integrator implemented with a register R and a capacitor C, a comparator LVDS for outputting a signal transferred from the analog circuit as a 1-bit signal, a quantizer for oversampling the 1-bit signal transferred from the comparator LVDS, and an out port for RC-filtering the oversampled value to feed the RC-filtered result back as a delta input.

[0049] The analog circuit may include a first register R1 to which an analog input signal is input, a capacitor C connected to the first register R1 at one end, and a second register R2 connected between the first register R1 and the capacitor C at one end.

[0050] The comparator may include a Low Voltage Differential Signaling (LVDS) terminal which has a non-inverting input terminal connected to one end of the capacitor C as an input terminal.

[0051] The quantizer may include a Delay (D) flipflop including an input terminal connected to an output terminal of the LVDS terminal, a first output terminal connected to the digital filter (e.g., 313 of FIG. 1 and CIC filter of FIG. 2), and a second output terminal connected to the other end of the second register R2 through the out port.

[0052] If the controller (e.g., 300 of FIG. 1) is implemented as a digital controller, the analog circuit of FIG. 2 may be disposed outside the digital controller, and the comparator, the quantizer, the out port, and the digital filter may be disposed inside the digital controller.

[0053] That is, according to the present disclosure, an analog circuit of a simple configuration (R and C) may be disposed outside a digital controller to configure an adder and an integrator, and internal sources of the digital controller may be used to configure a comparator and a digital filter, thereby implementing a delta sigma modulation method.

[0054] The controller 300 may configure an analog circuit outside the digital controller, as well as inside the digital controller, to distribute the use of resources. That is, oversampled (e.g., tens to hundreds of samples of an analog signal frequency) 1-bit signal output values of the LVDS terminal and the D flipflop inside the digital controller may be down-sampled through the CIC filter. The controller 300 can reduce resources compared to when a commercial IP is used, since the controller 300 uses only a register except for the CIC filter upon delta sigma modulation.

[0055] FIG. 3 is a block diagram showing a configuration of the digital filter of FIG. 2, FIG. 4 shows a structure of a single CIC filter, and FIGS. 5 and 6 are views for describing a method of controlling a power conversion apparatus.

[0056] In the present disclosure, the digital filter (e.g., 313 of FIG. 1) may be a CIC filter. The CIC filter may use resources efficiently, since it can express all coefficients as "1" and accordingly, multiplying operations for coefficients can be omitted, compared to a Finite Impulse Response (FIR) filter.

[0057] Referring first to FIG. 3, the digital filter 313 may remove high frequency signals through a Low Pass Filter (LPF) to reduce the oversampled frequency, thereby reducing a sampling rate.

[0058] As shown in FIG. 3, the digital filter 313 may be configured with a filter of a predetermined order, by including a plurality of integrator stages cic 0, cic 1, and cic N for selectively providing outputs from a predetermined number of integrators sequentially as an input of a common Comb filter, and a comb stage Comb for generating a comb valid signal in synchronization with a decimation ratio of the integrator stages and selectively applying an input according to predetermined criteria for outputs from the integrator stages when a signal is generated to thus provide a final output.

[0059] The operation principle of the digital filter 313 may be high-frequency signal (fs) $\rightarrow$ h(z) $\rightarrow \downarrow$R $\rightarrow$ low-frequency signal (fs/R). Herein, h(z) may be a transfer function of the CIC filter, and R may be a decimation ratio.

[0060] The transfer function h(z) of the CIC filter may be expressed by Equation (1) below.

$$h(z) = \left[\sum_{i=0}^{RM-1} z^{-i}\right]^N = \frac{\left(1-z^{-RM}\right)^N}{\left(1-z^{-1}\right)^N}$$

$$\frac{1}{1-z^{-1}} \rightarrow \cdots \rightarrow \frac{1}{1-z^{-1}} \rightarrow R\downarrow \rightarrow \left(1-z^{-M}\right) \rightarrow \cdots \rightarrow \left(1-z^{-M}\right) \quad (1)$$

[0061] The transfer function h(z) of the CIC filter may be represented by N integrator stages corresponding to a denominator and N comb stages corresponding to a numerator, as seen in Equation (1). A sampling frequency may be reduced by the decimation ratio R. In Equation (1), N represents an order of the filter, and M represents a delay of the comb stage to be a value of "1" or "2".

[0062] Referring next to FIG. 4, the structure of the single CIC filter may include an integrator stage I and a Comb stage C. In this case, N is D/R, wherein R represents a decimation ratio and D represents a delay.

[0063] The digital filter 313 may reduce a sampling rate of an original signal fs to generate a decimated signal fs/R.

[0064] Operation timings of the Comb stage of FIG. 3 may be shown in FIG. 5.

[0065] The digital filter 313 may include Random Access Memory (RAM) for storing inputs and outputs from the integrator stages and the comb stage.

[0066] The RAM may selectively store outputs from the integrator stages in the corresponding addresses according to criteria set in advance by a valid signal.

[0067] When a N-order CIC filter is used, the Comb filter may share address input internal RAM by using decimation.

[0068] Referring again to FIG. 3, outputs from the N integrators may be selectively and sequentially used as inputs of the common Comb filter. Although the Comb filter needs to operate by the same number of stages as the integrators, there may be space relatively since a sampling rate at which the Comb filter operates has been reduced. Referring to FIG. 5, the comb stage may generate a comb valid signal v_comb0, v_comb1, and v_comb2 in synchronization with a decimation ratio to selectively receive outputs from the integrator stages when a signal is generated, thereby providing a final output d_out.

[0069] Simulation results of the A/D converter 310 are shown in FIG. 6.

[0070] In FIG. 6, IP corresponds to a case in which ADC IP is applied upon A/D conversion in the digital controller, and Proposal corresponds to a case in which the CIC filter and the delta sigma method according to the present disclosure are applied.

[0071] The controller 300 may be implemented with memory (not shown) that stores algorithms for controlling the operations of components in the power conversion apparatus 100 or data for programs for executing the algorithms, and a processor (not shown) that performs the above-described operations using the data stored in the memory. The memory and the processor may be implemented as separate chips. Alternatively, the memory and the processor may be integrated into a single chip.

[0072] FIGS. 7 and 8 are flowcharts illustrating a method of controlling a power conversion apparatus.

[0073] FIG. 7 is a view for describing an example of an A/D conversion process using delta sigma modulation in a digital controller.

[0074] As shown in FIG. 7, the controller 300 of the power conversion apparatus may receive an analog input signal Vin from the power module 200, in operation 410.

[0075] Then, the controller 300 may compare the analog input signal Vin to a modulation signal to output a 1-bit signal, in operation 420.

[0076] Thereafter, the controller 300 may oversample the 1-bit signal to output the oversampled 1-bit signal as an ADC 1 bit, in operation 430.

[0077] Then, the controller 300 may downsample the oversampled 1-bit signal to complete A/D conversion, in operation 440.

[0078] Although not shown in FIG. 7, the oversampled signal may be subjected to RC-filtering (DAC), and then feed back as a delta input (returning to operation 420).

[0079] Referring next to FIG. 8, downsampling of operation 440 of FIG. 7 may be performed as follows.

[0080] FIG. 8 is a view for describing an example of a case in which a CIC filter is implemented in a digital controller.

[0081] As shown in FIG. 8, the controller 300 of the power conversion apparatus may receive the 1-bit signal (ADC 1-bit signal) in operation 511, and input the 1-bit signal to a zero-order integrator stage of the CIC filter, in operation 513.

[0082] Then, the controller 300 may sequentially perform the integration stage output s (a), (b), and (c) from zero-order to predetermined number (N)-order of the CIC filter, in operations 515 to 519. The operations 511 to 519 may mean the concept of a N^{th}-order CIC filter.

[0083] Meanwhile, the controller 300 may selectively input output values of N sensing signals from the integrator stages to Comb filters by the valid signal, when there are CIC filters of CIC_0 to CIC_N, for A/D conversion of the N sensing signals, in operations 521 to 529 (see FIG. 3).

[0084] Then, the controller 300 may generate a decimation signal and a valid signal, in operation 531.

[0085] Then, the controller 300 may receive the outputs from the integrator stages as an input (a), (b), ..., or (n) to the comb stage, selectively, according to predetermined criteria, in operation 533.

[0086] Then, the controller 300 may sequentially perform the comb stages output from zero-order to predetermined number (N)-order in the CIC filter, in operations 535 to 539.

[0087] Then, the controller 300 may apply a saturator to use a value in a valid range, in operation 541. However, the operation 541 may be not necessarily performed, and may be omitted.

[0088] At this time, the controller 300 may store operation values in the internal RAM, instead of a register. The comb stage reduces a sampling rate by R (decimation ratio) compared to the integrator stages. Accordingly, the controller 300 may not operate the comb stage simultaneously with the integrator stages, since simultaneously operating every cycle is not necessary. The comb stage may share the RAM sequentially according to order. In this case, a level of sharing may be about 0.5 times of R. The outputs from the integrator stages may be stored in the corresponding addresses of the RAM selectively by a valid signal. The valid signal may be synchronized with the decimation ratio.

[0089] The comb stage may receive the inputs selectively by the valid signal, and process operations, thereby increasing the use efficiency of resources.

[0090] According to the above-described embodiments, it is possible to reduce the utilization of digital controller resources upon analog-to-digital conversion in the digital controller.

[0091] Meanwhile, the above-described embodiments may be embodied in the form of a non-transitory computer-readable recording medium to store commands executable by a computer. The commands may be stored in the form of program codes, and when executed by a processor, the commands can create a program module to perform operations of the embodiments. The recording medium may be embodied as computer-readable recording medium. The computer-readable recording medium may include all kinds of recording media storing commands that can be decoded by a computer. For example, the computer-readable recording medium may be Read Only Memory (ROM), Random Access Memory (RAM), a magnetic tape, a magnetic disk, flash memory, an optical data storage device, or the like.

[0092] Although certain embodiments of the present disclosure have been shown and described, it would be appreciated by those skilled in the art that changes may be made in these embodiments without departing from the principles and spirit of the disclosure, the scope of which is defined in the claims and their equivalents.

Claims

1. A power conversion apparatus comprising:

   a power module configured to transfer an analog sensing signal corresponding to a current of an inductor and a voltage applied at both terminals of a capacitor, and to perform power conversion by driving a power semiconductor with a pulse-width modulation signal; and
   a controller configured to receive the analog sensing signal from the power module, to convert the analog sensing signal to a digital signal, to generate the pulse-width modulation signal, and to transfer the pulse-width modulation signal to the power module.

2. The power conversion apparatus of claim 1, wherein the controller includes an Analog to Digital (A/D) converter configured to convert the analog sensing signal to the digital signal through a delta sigma modulation method.

3. The power conversion apparatus of claim 2, wherein the A/D converter includes:

   a delta sigma modulator configured to convert the analog sensing signal to the digital signal by converting an analog input signal to a 1-bit signal through a delta and a sigma signal for integrating the delta, wherein the delta is a difference between the analog input signal and a modulation signal that is feedback of the delta; and
   a digital filter configured to smooth the 1-bit signal.

4. The power conversion apparatus of claim 3, wherein the delta sigma converter includes:

   an analog circuit including an adder and an integrator implemented with a register and a capacitor;
   a comparator configured to output a signal transferred from the analog circuit as the 1-bit signal;
   a quantizer configured to oversample the 1-bit signal transferred from the comparator; and
   an out port configured to RC-filter the oversampled value, and to feed the RC-filtered value back as a delta input.

5. The power conversion apparatus of claim 4, wherein the analog circuit includes a first register configured to receive the analog input signal, a capacitor connected to the first register at one end thereof, and a second register connected between the first register and the capacitor at one end thereof.

6. The power conversion apparatus of claim 4 or 5, wherein the comparator includes a Low Voltage Differential Signaling (LVDS) terminal having a non-inverting input terminal connected to one end of the capacitor as an input terminal.

7. The power conversion apparatus of claim 6, wherein the quantizer includes a Delay (D) flipflop including an input terminal connected to an output terminal of the LVDS terminal, a first output terminal connected to the digital filter, and a second output terminal connected to the other end of the second register through the out port.

8. The power conversion apparatus of any one of claims 4 to 7, wherein, when the controller is implemented as a digital controller, the analog circuit is disposed outside the digital controller, and the comparator, the quantizer, the out port, and the digital filter are disposed inside the digital controller.

9. The power conversion apparatus of any one of claims 3 to 8, wherein the digital filter is configured with a filter of a predetermined order, including a plurality of integrator stages configured to sequentially provide outputs from a predetermined number of integrators as input of a common Comb filter, and a comb stage configured to generate a comb valid signal in synchronization with a decimation ratio of the plurality of integrator stages and to selectively apply an input according to predetermined criteria for outputs from the plurality of integrator stages when a signal is generated to provide a final output.

10. The power conversion apparatus of claim 9, wherein the digital filter includes random access memory (RAM) configured to store an input to or an output from the plurality of integrator stages and the comb stage.

11. The power conversion apparatus of claim 10, wherein the RAM selectively stores the outputs from the plurality of integrator stages in corresponding addresses according to criteria set in advance by a valid signal.

12. An Analog to Digital (A/D) converter comprising:

a delta sigma modulator configured to convert an analog sensing signal to a digital signal by converting an analog input signal to a 1-bit signal through a delta and a sigma signal for integrating the delta, wherein the delta is a difference between the analog input signal and a modulation signal that is feedback of the delta; and
a digital filter configured to smooth the 1-bit signal.

13. The A/D converter of claim 12, wherein the delta sigma modulator includes:

an analog circuit including an adder and an integrator implemented with a register and a capacitor;
a comparator configured to output a signal transferred from the analog circuit as a 1-bit signal;
a quantizer configured to oversample the 1-bit signal transferred from the comparator; and
an out port configured to RC-filter the oversampled value, and to feed the RC-filtered value back as a delta input.

14. The A/D converter of claim 13, wherein, when the A/D converter is implemented as a digital controller, the analog circuit is disposed outside the digital controller, and the comparator, the quantizer, the out port, and the digital filter are disposed inside the digital controller.

15. The A/D converter of any one of claims 12 to 14, wherein the digital filter is configured with a filter of a predetermined order, including a plurality of integrator stages configured to sequentially provide outputs from a predetermined number of integrators as input of a common Comb filter, and a comb stage configured to generate a comb valid signal in synchronization with a decimation ratio of the plurality of integrator stages and selectively applying an input according to predetermined criteria for outputs from the plurality of integrator stages when a signal is generated to provide a final output.

FIG. 1

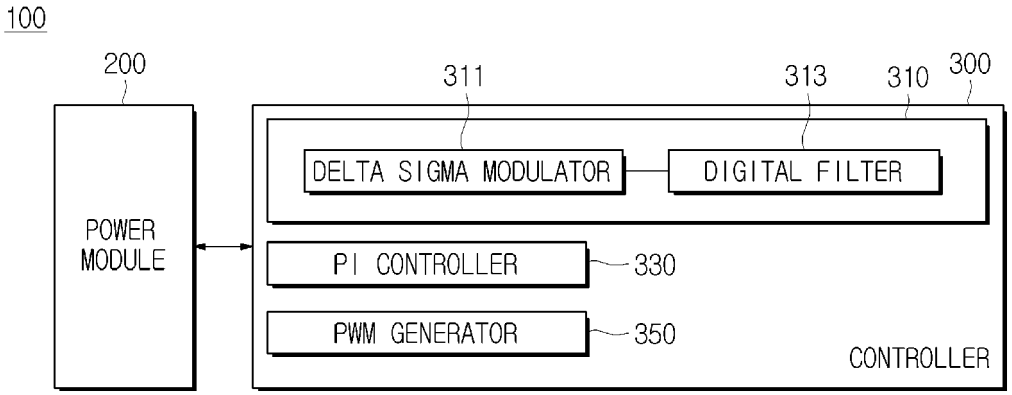

100
200
311
313
310
300
POWER MODULE
DELTA SIGMA MODULATOR
DIGITAL FILTER
PI CONTROLLER
330
PWM GENERATOR
350
CONTROLLER

FIG. 2

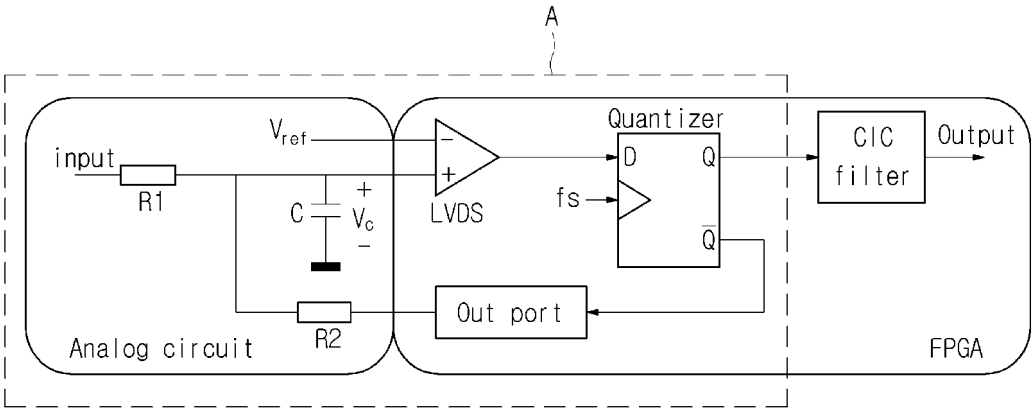

A
input
R1
V_{ref}
C
V_c
LVDS
Quantizer
D
Q
fs
$\overline{Q}$
CIC filter
Output
Out port
R2
Analog circuit
FPGA

FIG. 3

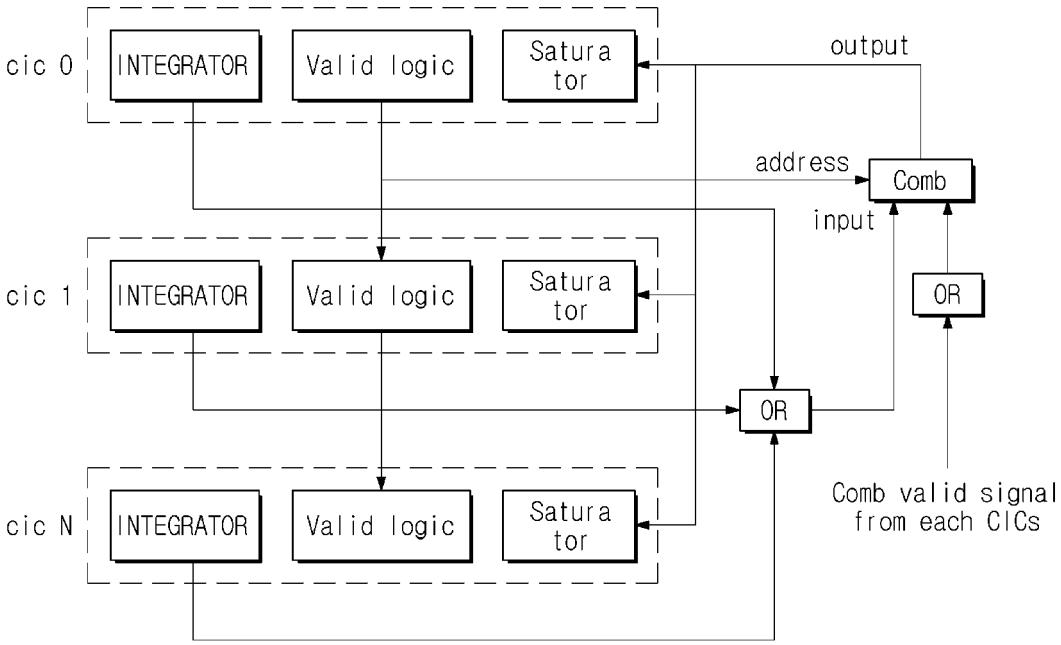

cic 0
INTEGRATOR
Valid logic
Satura tor
output
address
Comb
input
cic 1
INTEGRATOR
Valid logic
Satura tor
OR
OR
cic N
INTEGRATOR
Valid logic
Satura tor
Comb valid signal from each CICs

FIG. 4

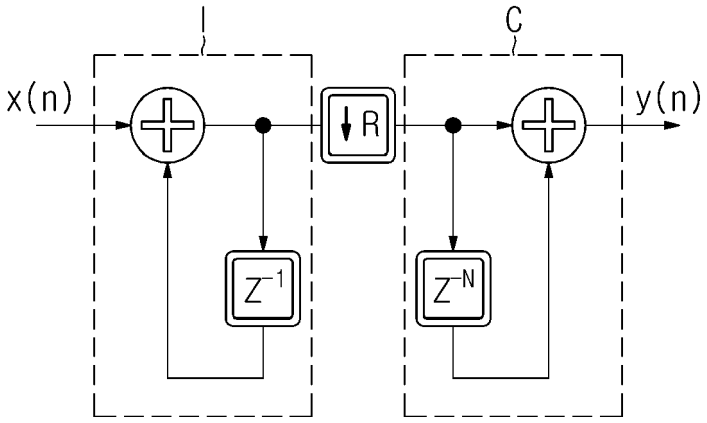


FIG. 5

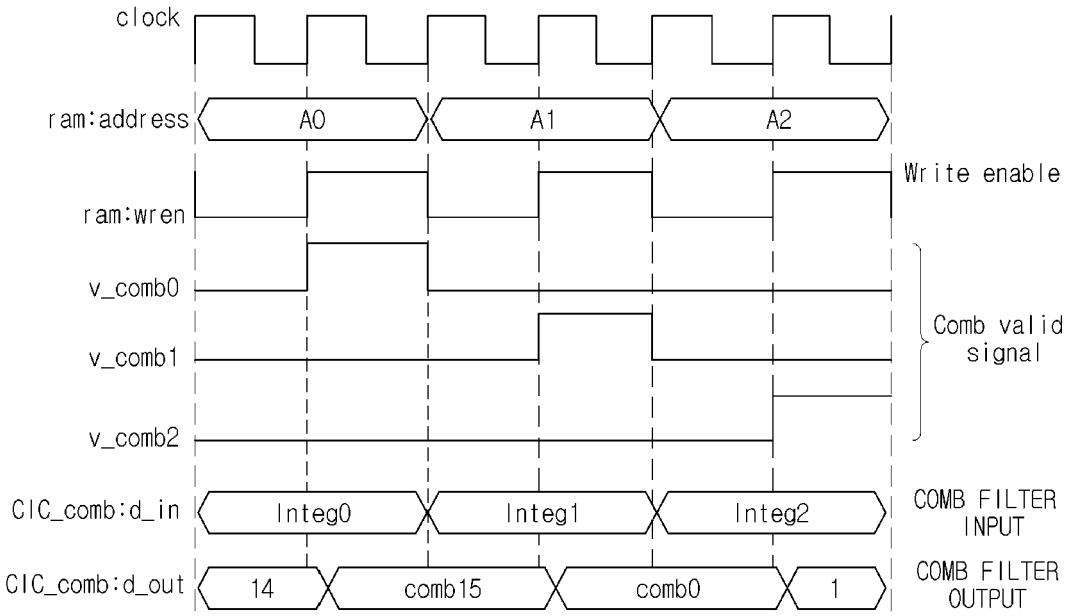

clock
ram:address
A0
A1
A2
Write enable
ram:wren
v_comb0
v_comb1
v_comb2
Comb valid signal
CIC_comb:d_in
Integ0
Integ1
Integ2
COMB FILTER INPUT
CIC_comb:d_out
14
comb15
comb0
1
COMB FILTER OUTPUT

FIG. 6

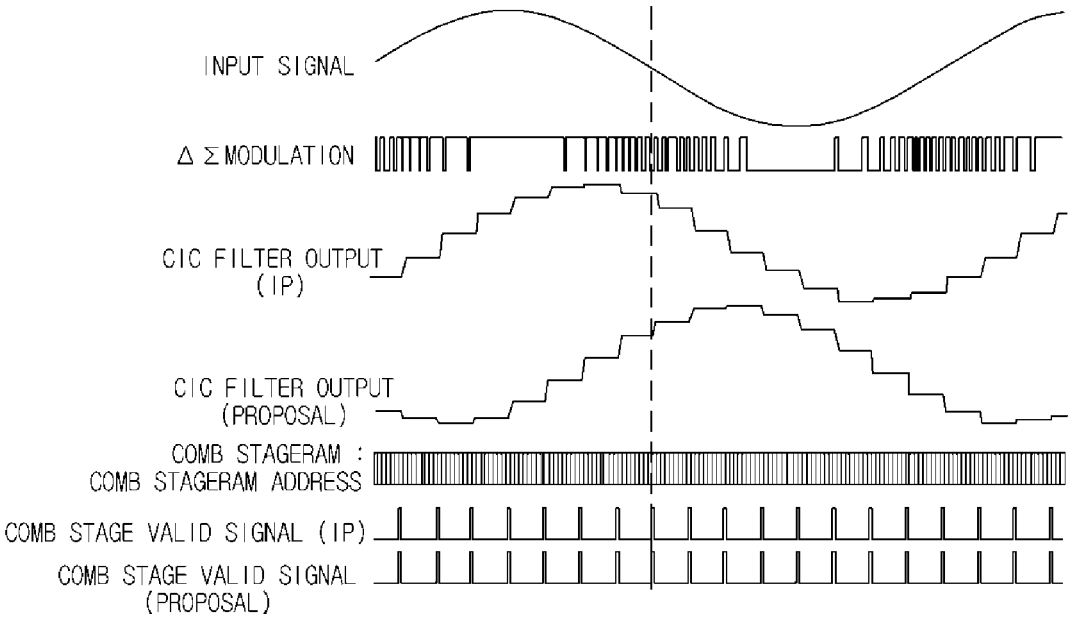

INPUT SIGNAL
Δ Σ MODULATION
CIC FILTER OUTPUT (IP)
CIC FILTER OUTPUT (PROPOSAL)
COMB STAGERAM : COMB STAGERAM ADDRESS
COMB STAGE VALID SIGNAL (IP)
COMB STAGE VALID SIGNAL (PROPOSAL)

FIG. 7

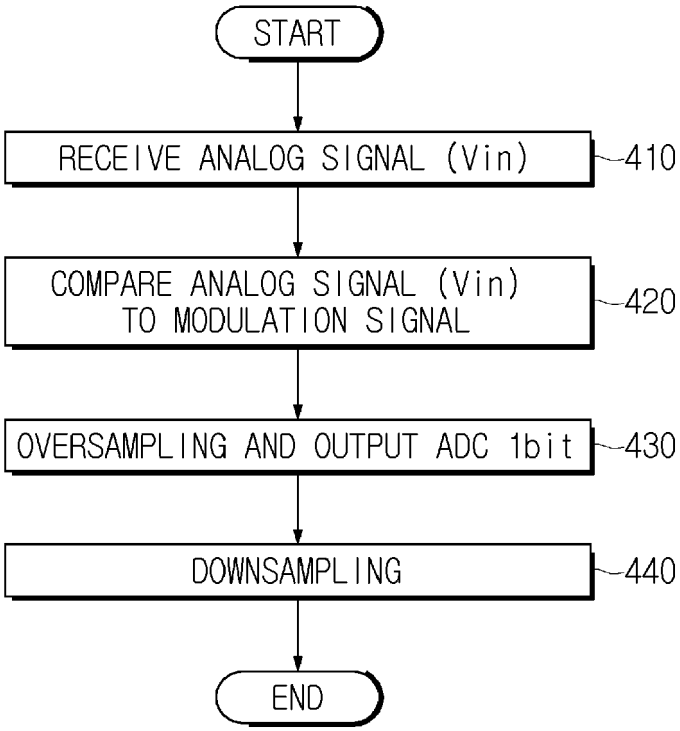
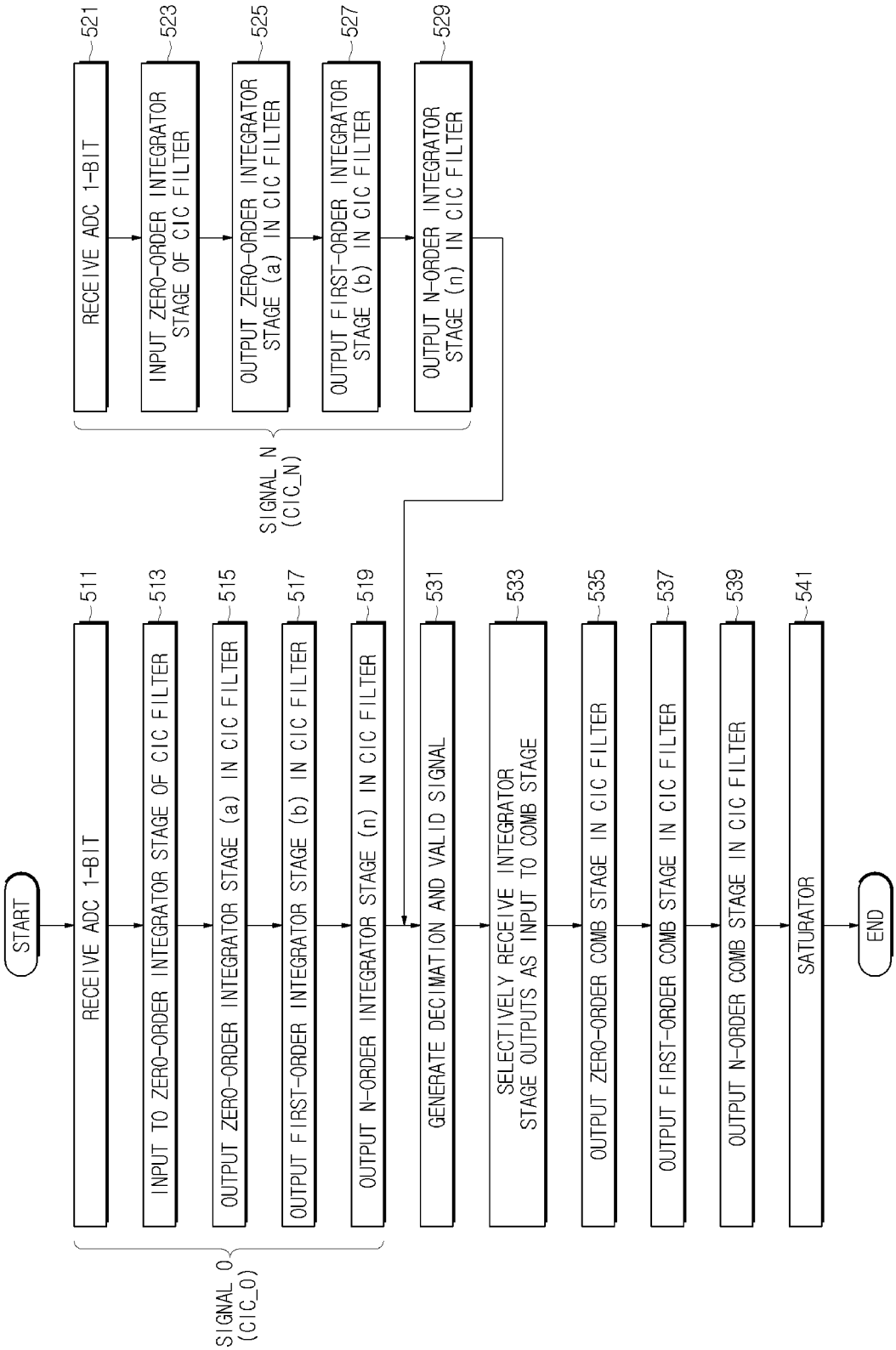

START
RECEIVE ANALOG SIGNAL (Vin)
410
COMPARE ANALOG SIGNAL (Vin) TO MODULATION SIGNAL
420
OVERSAMPLING AND OUTPUT ADC 1bit
430
DOWNSAMPLING
440
END

FIG. 8


START
RECEIVE ADC 1-BIT
511
INPUT TO ZERO-ORDER INTEGRATOR STAGE OF CIC FILTER
513
OUTPUT ZERO-ORDER INTEGRATOR STAGE (a) IN CIC FILTER
515
OUTPUT FIRST-ORDER INTEGRATOR STAGE (b) IN CIC FILTER
517
OUTPUT N-ORDER INTEGRATOR STAGE (n) IN CIC FILTER
519
SIGNAL 0 (CIC_0)
RECEIVE ADC 1-BIT
521
INPUT ZERO-ORDER INTEGRATOR STAGE OF CIC FILTER
523
OUTPUT ZERO-ORDER INTEGRATOR STAGE (a) IN CIC FILTER
525
OUTPUT FIRST-ORDER INTEGRATOR STAGE (b) IN CIC FILTER
527
OUTPUT N-ORDER INTEGRATOR STAGE (n) IN CIC FILTER
529
SIGNAL N (CIC_N)
GENERATE DECIMATION AND VALID SIGNAL
531
SELECTIVELY RECEIVE INTEGRATOR STAGE OUTPUTS AS INPUT TO COMB STAGE
533
OUTPUT ZERO-ORDER COMB STAGE IN CIC FILTER
535
OUTPUT FIRST-ORDER COMB STAGE IN CIC FILTER
537
OUTPUT N-ORDER COMB STAGE IN CIC FILTER
539
SATURATOR
541
END

Europäisches Patentamt
European Patent Office
Office européen des brevets

EUROPEAN SEARCH REPORT

Application Number
EP 18 19 4219

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	DE 10 2016 120129 A1 (INFINEON TECHNOLOGIES AUSTRIA AG [AT]) 27 April 2017 (2017-04-27)	1-3,9-12	INV. H03M3/00
Y	* column 3, lines 46-50 * * column 5, line 46 * * column 6, lines 3-4 * * column 6, lines 34-38 * * column 7, lines 7-12 * * column 7, lines 16-18 * * column 7, lines 37-40 * * column 8, lines 1-7 * * column 8, lines 34-41 * * column 9, lines 1-6 * * column 9, lines 41-49 * * column 10, lines 7-14 * * column 10, lines 22-32 * * column 10, lines 34-36 * * column 12, lines 35-39 * * Equations 3 and 5 * * figures 2-5 * -----	4-8	ADD. H02M3/335
X	Anonymous: "Simple Sigma-Delta ADC", , November 2010 (2010-11), pages 1-6, XP55571150, Retrieved from the Internet: URL:https://web.archive.org/web/20101130110354if_/http://www.latticesemi.com:80/documents/rd1066.pdf [retrieved on 2019-03-19]	12-15	TECHNICAL FIELDS SEARCHED (IPC) H03M H02M
Y	* Section "Overview"; page 1 * * Section "RC Network Design"; page 2 * * Section "SSD ADC Comparator"; page 4 * * Section "SSD ADC Sampling Element"; page 4 * * figures 1,3 * -----	4-8	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	25 March 2019	Rocha, Daniel

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 18 19 4219

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

25-03-2019

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 102016120129 A1	27-04-2017	CN 106877670 A	20-06-2017
		DE 102016120129 A1	27-04-2017
		US 2017117812 A1	27-04-2017

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82