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(54) **Method for manufacturing a native MOS P-channel transistor with a process manufacturing non-volatile memories**

Herstellungsverfahren eines nativen MOS-P-Kanal-Transistors mit Verfahren für nichtflüchtige Speicher

Procédé de fabrication d'un transistor MOS naturel à canal p avec un procédé pour mémoires non volatiles

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Description

Field of the Invention

[0001] This invention relates to a method of manufacturing a P-channel native MOS transistor in a circuit integrated on a semiconductor which also includes a matrix of non-volatile memory cells of the floating gate type with two polysilicon levels and having an interpoly dielectric layer sandwiched between the two polysilicon levels, said method comprising the steps of:

masking and defining active areas of the discrete integrated devices;

masking and defining the first polysilicon level using a Poly1 mask;

masking and defining an intermediate dielectric layer using a Matrix mask.

Background Art

[0002] As is well known, processes for manufacturing integrated electronic structures which include non-volatile memory cells, that is matrices of cells organized into rows and columns, using a dual level of polysilicon with an interpoly dielectric isolation layer interposed between the two polysilicon levels, are extensively used in the industry.

[0003] These processes provide for a first masking and implanting step to define well regions in a semiconductor substrate which have a different type of conductivity from that of the substrate.

[0004] Conventional processes provide for the initial definition of the active areas of the various integrated devices (transistors, memory cells, etc.). Usually, a subsequent oxide growing step is also provided to form field isolation regions formed by a thick oxide layer which isolates the discrete active areas from each other.

[0005] In some cases, the process may include a relatively heavy implantation for threshold raising purposes, which is usually performed in the matrix area, that is in the region where the memory cells are formed. However, this operation may be carried out at a later stage of the manufacturing process.

[0006] To enable all the aspects of the present invention to be more clearly understood, it may be useful to recall the sequence of process steps which result, at the state of the art, in the formation of an integrated circuit of non-volatile memory cells.

[0007] A thin oxide layer, called the gate oxide, is grown over the active areas.

[0008] A first layer of polysilicon, referred to as the first-level polysilicon or Poly1, is then deposited onto the gate oxide.

[0009] Thereafter, a masking and etching step is usually carried out for a preliminary definition of the Poly1 which is to form part of the floating gate regions of the memory cells.

[0010] An intermediate isolation dielectric layer, called the interpoly, is next grown and/or deposited over the entire resultant structure. This dielectric layer may be a stack structure, i.e. comprised of a first oxidation layer overlaid by a thin layer of nitride, and a third layer of nitride oxidation. All this is referred to as the ONO layer.

[0011] At this stage of the manufacturing process, a masking step is carried out to thoroughly remove the interpoly layer, except from the matrix area occupied by the memory cells. It is on this account that the mask employed here is commonly termed the Matrix mask.

[0012] Subsequently, a second layer of polysilicon, known as the second-level polysilicon or Poly2, is deposited and doped.

[0013] Inside the matrix area, the Poly2 will remain isolated from the Poly 1 by the interpoly layer. In the regions outside the area occupied by the cell matrix, i.e. the regions accommodating the transistors and other external circuitry devices, the Poly2 layer overlies instead the existing Polyl layer directly.

[0014] The above process steps are described in Patent US 4,719,184 to the Applicant.

[0015] As previously mentioned, a further masking step may become necessary in some cases to provide a slight implant for adjusting the LVS (Light Voltage SHift) threshold of certain transistors in the external circuitry. Other low-threshold transistors, or so-called native transistors, must instead be screened off this implant.

[0016] Yet another masking step, and associated etching, allows the channel length of the transistors in the circuitry to be defined. A mask, designated Poly2, is used during this step which also allows the second-level polysilicon to be defined in the matrix area, with the etching stopped short of the intermediate interpoly layer.

[0017] An improvement in the above manufacturing method has been aimed at the formation of the native transistors. This improvement is described in European Patent Application No. 96830021.0 by the Applicant.

[0018] In essence, a much more effective way of forming native transistors, within a standard manufacturing process like that just described, has been provided. This method substantially eliminates the masking step for threshold adjustment in the external circuitry transistors, thereby lowering the manufacturing costs.

[0019] It was considered of using the same Matrix mask as is used for etching away the interpoly dielectric layer in order to define the channel length of the native transistors located outside the area occupied by the matrix.

[0020] Accordingly, instead of carrying out the LVS step, the Matrix mask is suitably modified and also employed for masking the channel area within the active area of the native transistors located outside the matrix area.

[0021] These native transistors are formed unconventionally with respect to the other raised-threshold transistors. The aforementioned European Patent Application discloses all the details about this formation.

[0022] The present invention fits in the same line of research that resulted in the method just described.

[0023] The underlying technical problem of this invention is to provide a novel nethod of manufacturing a P-channel native MOS transistor, within the frame of a process for manufacturing non-volatile memories, which method has features appropriate to ensure the desired formation regardless of the threshold adjusting implantations applied to other enhancement transistors in the external circuitry of the matrix area, and therefore to avoid one masking level.

[0024] In other words, the aim is to enable a P-channel native transistor to be made without one masking level, while preventing subsequent LDD implantations from altering the threshold of the transistor.

Summary of the Invention

[0025] The solution idea behing this invention is to have the nominal length of the channel region of the native transistor defined by means of the same Matrix mask used to define the matrix regions, and to utilize a second mask of Poly2, wider than the former, to ensure an aligned overlap of the two polysilicon levels over the channel region.

[0026] Based on this solution idea, the technical problem is solved by a method as previously indicated and defined in the characterizing part of Claim 1.

[0027] The features and advantages of the inventive method will be apparent from the following description of an embodiment thereof, given by way of example and not of limitation with reference to the accompanying drawings.

Brief Description of the Drawings

[0028] In the drawings:

Figures 1 to 3 are enlarged vertical cross-section views showing schematically a portion of a semiconductor substrate subjected to successive steps of the inventive method which lead to the formation of a P-channel native transistor; and

Figures 4 and 5 are schematic views of the portion in Figures 1-3 as subjected to final steps of the manufacturing method according to the invention.

Detailed Description

[0029] Referring to the drawing figures, generally and schematically shown at 1 is a portion of a semiconductor substrate where a P-channel native MOS transistor is formed in accordance with this invention.

[0030] The method of this invention provides for the formation of well regions in the substrate 1 which have a different type of conductivity if compared to the substrate.

[0031] Similarly to conventional processes, the definition of the active areas 2 also includes the formation of isolation regions 3 by the growing of a thick layer of field oxide.

[0032] At this stage, a relatively heavy threshold-raising implantation can be performed, unless already performed at an earlier stage, in the matrix area, i.e. the region where the memory cells are formed.

[0033] A thin layer 4 of gate oxide is formed over the active areas, also by a standard process sequence.

[0034] The process goes on with the deposition of a first layer 5 of polysilicon, called the Poly1. This layer 5 is suitably doped with phosphorus.

[0035] A masking and etching step of the Poly1 layer 5 is carried out to define the floating gate regions of the cells in the memory matrix. These regions are not shown because the point of interest lies in the regions outside the matrix area, specifically in the regions where native transistors 7 associated with the external circuitry of the memory matrix are located.

[0036] Accordingly, only a portion of a semiconductor substrate is shown in Figure 1 where the P-channel MOS transistor 7 is formed by the method of this invention.

[0037] The masking and etching of Polyl spares the first-level polycrystalline layer 5 over the active areas of the native transistors 7.

[0038] The manufacturing process goes on with a thermal oxidation and/or deposition treatment which leads to a dielectric isolation layer 8, called the interpoly, being formed.

[0039] Using a modified Matrix mask 9, e.g. as described in European Patent Application No. 96830021.0, a central or channel area is defined for the transistor 7 at this stage.

[0040] This mask 9 has a predetermined width, and allows the dielectric layer 8 to be removed from the circuitry zones, and the nominal length of the native threshold of transistor 7 to be defined, as shown in Figure 1.

[0041] In fact, the dielectric layer 8 is etched away and a slight LVS implantation is performed in the channel zones of the transistors belonging to the external circuitry of the matrix area, through the openings in the Matrix mask. However, the mask 9 will be screening the native threshold channel region of the transistor 7 from the LVS implant, as shown in Figure 2.

[0042] The mask 9 is then removed, and the native threshold channel region left covered by a portion of the dielectric layer 8.

[0043] A second layer 10 of polycrystalline silicon, called the Poly2, is deposited next as shown in Figure 3.

[0044] A layer of a silicide 11, preferably of a tungsten silicide WSi_x, can also be deposited over this layer 10.

[0045] At this stage, a mask 12 of Poly2, that is one for defining the second-level polysilicon, is also used on the channel region of the transistor 7.

[0046] Advantageously in this invention, the mask 12 is wider than the Matrix mask 9, as can be seen in Figure 3.

[0047] In this way, the contact is maintained between the layers 5 and 10 of Poly1 and Poly2, both over the field oxide region 3 and the active area 2. In essence, the use of a Poly2 mask 12 of greater width than the previous mask 9 allows two levels 5 and 10 of polysilicon to overlap each other in self-alignment over the channel region.

[0048] An etching step is then carried out on the stack structure formed of the silicide 12, the Poly2 10, and the Polyl 5.

[0049] A stack structure is left to overlie the active area 2 of the transistor 7, centrally of the channel region, which comprises the layers 5 and 10 of Poly1 Poly2 in mutual contact but for a central zone which is separated by a trapped portion of interpoly 8.

[0050] At this stage, a P^- implantation of the LDD (Lightly Doped Drain) type can be carried out as shown schematically in Figure 4. This implant will affect the zones laterally of the channel region, as indicated at 13 in Figure 4.

[0051] The method of this invention includes the formation of so-called spacers 15, on opposite sides of the stack structure which rises centrally in the channel region. These spacers 15 screen at least part of the underlying P^- doped zones 13 from further implantations.

[0052] Figure 5 shows a subsequent process step of performing a P^+ implantation in the lateral zones of the channel region. By using the masking afforded by the spacers, this further P^+ implantation allows the junctions 6 of the LDD type to be defined laterally of the channel region with great accuracy.

[0053] Thus, the method of this invention enables a P-channel native MOS transistor structure 7 to be defined in which the nominal length of the native threshold channel is determined by the Matrix mask 9.

[0054] This expedient provides a device with desired characteristics, a P-channel native transistor in this case, in a manner wholly independent of LDD implantations which might be performed with sufficient energy to go through the Poly1 layer and dope the underlying substrate. In this situation, two channel zones would be produced laterally of and in series with the native transistor whose characteristics cannot be predetermined. Such zones would be activated by a gate voltage also not to be predetermined relative to that required to activate the native concentration channel region, thereby impairing the native transistor operation.

[0055] This consideration leads to conclude that the principles of the invention do not appear to be applicable to the formation of N-channel native transistors because, in this case, the two LVS zones associated in series with the channel would be turned on at a higher gate voltage than the native concentration channel region, which would shift the transistor threshold.

[0056] It will be appreciated from the foregoing description that the formation of the P-channel native MOS transistor by having the two polysilicon layers Poly1 and Poly2 overlap each other in self-alignment has the advantage of providing similar spacers to those of standard transistors, and therefore with the same drain architecture.

[0057] Furthermore, in the instance of a compensated LDD as described in US Patent No. 4,719,184, the uncertainty of an LDD implantation performed through the Poly1 layer, likely to make the threshold of the parasitic transistors associated with the structure unstable, is avoided.

Claims

1. A method of manufacturing a P-channel native MOS transistor (7) in a circuit integrated on a semiconductor (1) which also includes a matrix of non-volatile memory cells of the floating gate type with two polysilicon levels (5,10) and having an intermediate dielectric layer (8) sandwiched between the two polysilicon levels, said method comprising the steps of:

> masking and defining active areas (2) of the discrete integrated devices;
>
> masking and defining the first polysilicon level (5) using a Poly1 mask;
>
> masking and defining an intermediate dielectric layer (8) using a Matrix mask (9):

characterized in that the length of the native threshold channel of said transistor is defined by means of the Matrix mask (9) and by etching away the intermediate dielectric layer (8), and that for a subsequent step of masking and defining the second polysilicon level (10), a Poly2 mask (12) is used which covers the active area of the transistor (7) with a greater width than the previous Matrix mask (9) to enable, as by subsequent etching, the two polysilicon levels (5,10) to overlap in self-alignment over the channel region.

2. A method according to Claim 1, **characterized in that** said Matrix mask (9) covers the channel area of the native transistor (7) and is utilized for screening said channel area from a threshold adjust implant of other transistors outside the matrix area.

3. A method according to Claim 1, **characterized in that** it comprises an etching step for defining, centrally of the channel region, a stack structure formed by the first and second polysilicon levels (5,10) in mutual contact excepting at a central zone separated by a trapped portion of interpoly (8).

4. A method according to Claim 3, **characterized in that** it comprises a P^- implantation of the LDD type in the lateral zones of the channel region.

5. A method according to Claim 3, **characterized in that** it comprises the formation of so-called spacers (15) on opposite sides of the stack structure which rises centrally of the channel region.

6. A method according to Claim 5, **characterized in that** it comprises a P^+ implantation in the lateral zones (13) of the channel region, said zones being partly screened off by the spacers (15), thereby forming junctions (6) of the LDD type laterally of the channel region.

7. A method according to Claim 1, **characterized in that** said Matrix mask (9) screens the channel region from a slight light voltage shift, LVS, implantation.

Patentansprüche

1. Verfahren zum Herstellen eines nativen P-Kanal-MOS-Transistors (7) in einer Schaltung, die auf einem Halbleiter (1) integriert ist, auf dem sich auch eine Matrix nicht flüchtiger Speicherzellen des Typs mit floatendem Gate mit zwei Polysiliziumebenen (5, 10) und einer zwischen die beiden Polysiliziumebenen geschichteten Zwischendielektrikumschicht (8) befindet, wobei das Verfahren folgende Schritte aufweist:

Maskieren und Definieren von aktiven Bereichen (2) der diskreten inte-grierten Vorrichtungen;

Maskieren und Definieren der ersten Polysiliziumebene (5) unter Verwendung einer Poly1-Maske;

Maskieren und Definieren einer Zwischendielektrikumschicht (8) unter Verwendung einer Matrix-Maske (9):

dadurch gekennzeichnet, dass sich die Länge des Kanals nativen Schwellenwertes des Transistors definiert wird mittels der Matrixmaske (9) und durch Wegätzen der Zwischendielektrikumschicht (8), und dass für einen nachfolgenden Schritt des Maskierens und Definierens der zweiten Polysiliziumebene (10) eine Poly2-Maske (12) verwendet wird, welche den aktiven Bereich des Transistors (7) mit einer größeren Weite als die vorausgehende Matrixmaske (9) bedeckt, um es den beiden Polysiliziumebenen (5, 10) zu ermöglichen, beispielsweise durch nachfolgendes Ätzen, sich in Selbstausrichtung über der Kanalregion zu überlappen.

2. Verfahren nach Anspruch 1, **dadurch gekennzeichnet, dass** die Matrixmaske (9) den Kanalbereich des nativen Transistors (7) bedeckt und verwendet wird für das Abschirmen des Kanalbereichs von einer Schwellenwerteinstellimplantation anderer Transistoren außerhalb des Matrixbereichs.

3. Verfahren nach Anspruch 1, **dadurch gekennzeichnet, dass** es einen Ätzschritt aufweist zum Definieren, in der Mitte der Kanalregion, einer Stapelstruktur, gebildet durch die erste und die zweite Polysiliziumebene (5, 10) in welchselseitigem Kontakt mit Ausnahme in einer zentralen Zone, die durch einen eingeschlossenen Teil des Zwischenpolysiliziums (8) getrennt ist.

4. Verfahren nach Anspruch 3, **dadurch gekennzeichnet, dass** es eine P^--Implantation des LDD-Typs in den Seitenzonen der Kanalregion aufweist.

5. Verfahren nach Anspruch 3, **dadurch gekennzeichnet, dass** es die Bildung sogenannter Abstandsvorrichtungen (15) auf entgegengesetzten Seiten der von der Mitte der Kanalregion hochstehenden Stapelstruktur aufweist.

6. Verfahren nach Anspruch 5, **dadurch gekennzeichnet, dass** es eine P^+-Implantation in die Seitenzonen (13) der Kanalregion aufweist, wobei diese Zonen von den Abstandsvorrichtungen (15) teilweise abgeschirmt werden, wodurch Übergänge (6) des LDD-Typs seitlich von der Kanalregion gebildet werden.

7. Verfahren nach Anspruch 1, **dadurch gekennzeichnet, dass** die Matrixmaske (9) die Kanalregion abschirmt von einer eine leichte Spannungsverschiebung, LVS, bewirkenden leichten Implantation.

Revendications

1. Procédé de fabrication d'un transistor MOS natif à canal P (7) dans un circuit intégré sur un semiconducteur (1) comprenant également une matrice de cellules de mémoire non-volatile de type à grilles flottantes avec deux niveaux de silicium polycristallin (5, 10) et comportant une couche diélectrique intermédiaire (8) disposée en sandwich entre les deux niveaux de silicium polycristallin, ledit procédé comprenant les étapes :

- masquer et définir les régions actives (2) des dispositifs discrets intégrés ;
- masquer et définir le premier niveau de silicium polycristallin (5) en utilisant un masque « poly 1 » ;
- masquer et définir une couche diélectrique intermédiaire (8) en utilisant un masque de matrice (9) ;

caractérisé en ce que la longueur du canal de seuil natif dudit transistor est définie au moyen du masque de matrice (9) et en éliminant par gravure chimique la couche diélectrique intermédiaire (8) et **en ce que**, au cours d'une étape ultérieure de masquage et de définition du deuxième niveau de silicium polycristallin (10), un masque « poly 2 » (12) est utilisé qui couvre la région active du transistor (7) avec une largeur plus importante que celle du précédent masque de matrice (9) pour permettre, tel que par une gravure chimique ultérieure, aux deux niveaux de silicium polycristallin (5, 10) de se recouvrir en auto-alignement par-dessus la région de canal.

2. Procédé selon la revendication 1, **caractérisé en ce que** ledit masque de matrice (9) couvre la région de canal du transistor natif (7) et est utilisé pour constituer un écran à ladite région de canal pour un implant d'ajustement de seuil d'autres transistors à l'extérieur de la région de la matrice.

3. Procédé selon la revendication 1, **caractérisé en ce qu'**il comprend une étape de gravure chimique pour définir, de manière centrale à la région de canal, une structure d'empilement formée par les premier et deuxième niveaux de silicium polycristallin (5, 10) en contact mutuel, excepté en une zone centrale séparée par une partie emprisonnée de silicium polycristallin intermédiaire (8).

4. Procédé selon la revendication 3, **caractérisé en ce qu'**il comprend une implantation P- de type LDD dans les zones latérales de la région de canal.

5. Procédé selon la revendication 3, **caractérisé en ce qu'**il comprend la formation d'éléments dits d'espacement (15) sur des côtés opposés de la structure d'empilement, qui s'élèvent au centre de la région de canal.

6. Procédé selon la revendication 5, **caractérisé en ce qu'**il comprend une implantation P+ dans les zones latérales (13) de la région de canal, lesdites zones étant partiellement munies d'un écran ménagé par les éléments d'espacement (15), en formant ainsi des jonctions (6) de type LDD de manière latérale à la région de canal.

7. Procédé selon la revendication 1, **caractérisé en ce que** ledit masque de matrice (9) fait écran à la région de canal relativement à une légère implantation de décalage de basse tension, LVS.

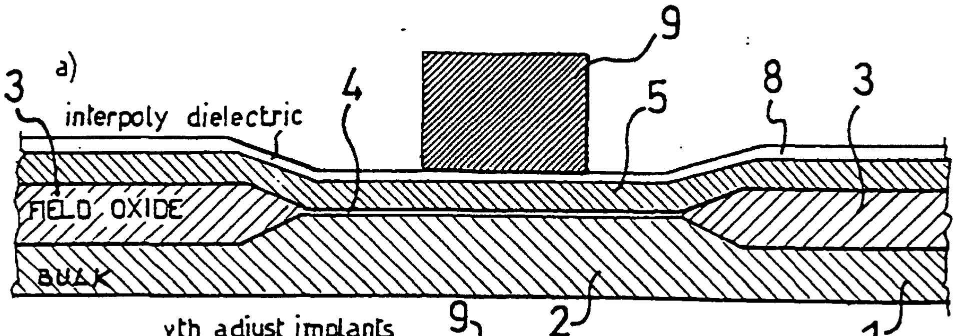

FIG.1

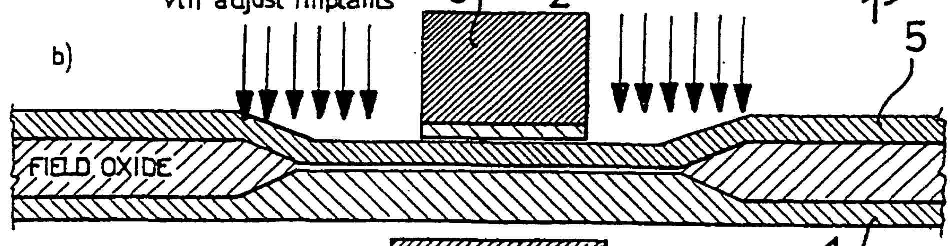

FIG.2

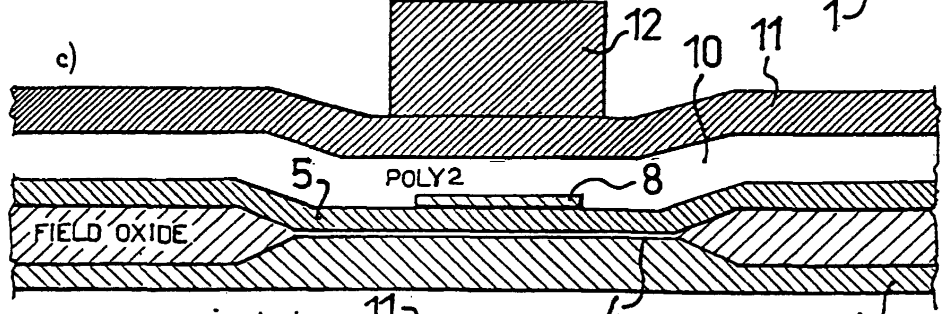

FIG.3

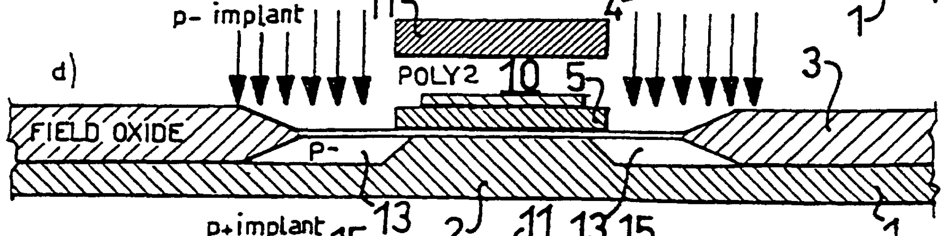

FIG.4

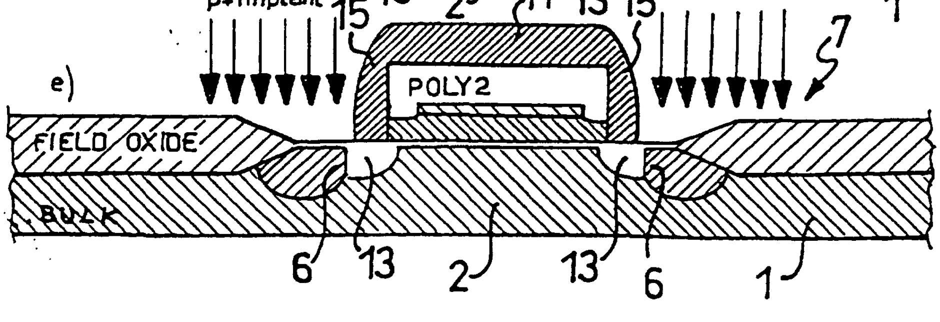

FIG.5