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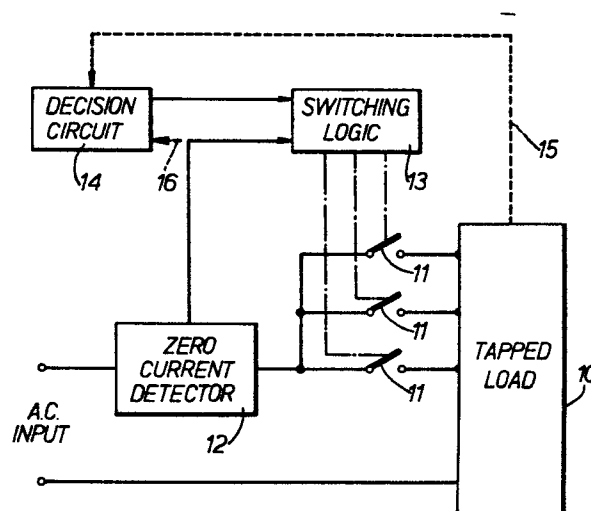
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54 **AC control apparatus.**

57 AC control apparatus includes a plurality of selectable switches (11) connected to a tapped load (10) and arranged to alter the magnitude of the volt-amp product consumed by the load. The switches (11) are activated by control means which includes a zero current detector (12), a decision circuit (14) and switching logic (13). The switching logic is responsive to a decision in the decision circuit and to the detector (14) to change switch at zero switch current.

The decision circuit (14) may be made responsive to an input or load parameter, and where the tapped load (10) comprises a tapped transformer having an output for connection to an external load, the parameter may be a function of the output voltage. The switches (11) as preferably semiconductor devices such as triacs. As an alternative, the tapped load may comprise a motor.



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"AC Control Apparatus"

The present invention relates to AC control apparatus for controlling a tapped load.

Apparatus for controlling AC to a tapped load is known wherein taps are selected by relay
5 switches in accordance with a required change in a particular parameter of the load. The tapped load typically includes a tapped transformer arranged to be connected to an external load and the relay switches may for example be energised in response to changes
10 in a particular parameter of the output waveform. Such known apparatus may initiate a change in tap at any time during a cycle of the AC waveform being fed to the tapped load, and consequently may introduce discontinuities into the output waveform. The result is that
15 such apparatus is electrically noisy and cannot be used satisfactorily with reactive loads; furthermore, severe distortions of the output waveform may be produced.

The present invention provides AC control
20 apparatus for controlling a tapped load comprising a plurality of selectable switches connected to the load to alter the magnitude of the volt-amp product consumed by the load, and control means including means for determining which of the switches should be
25 operative and zero current detecting means for detecting

when the switch current is substantially zero, whereby a change in switch can be accomplished at a current zero.

Embodiments of the present invention
5 utilising semiconductor switches such as triacs or S.C.R.'s provide fast switching between taps, and since the switching is arranged to occur at substantially zero currents, lead to greatly reduced electromagnetic interference (E.M.I.). Furthermore, such
10 zero current switching eliminates the possibility of two switches conducting at the same time (e.g. if the current through a semiconductor switch does not fall below the holding current prior to a different switch being energised), which would lead to large circulating
15 currents in the case of a tapped inductance, and possible consequent failure of the output.

Embodiments of the invention will be described wherein the tapped load comprises a tapped inductance such as a transformer or a motor. However, it is
20 intended that the tapped load include other reactive and/or resistive components; for example a capacitive load comprising a chain of capacitors connected in series may be provided, the tapping points being
25 arranged at the connections between adjoining capacitors; or a heating element may be provided with tapping points to form the load.

In order that the present invention may be more readily understood, embodiments thereof will now be described, by way of example with reference to
30 the accompanying drawings, in which:-

Figure 1 shows a generalised block diagram of a preferred form of AC control apparatus;

Figure 2 shows a more detailed block diagram of one embodiment of the apparatus shown in Figure 1;

35 Figure 3 shows a circuit diagram in

accordance with the embodiment shown in Figure 2;
and

Figure 4 shows waveforms at selected points
of Figure 3.

5 Referring to Figure 1, AC control apparatus
includes a tapped load 10 connected to a plurality of
switches 11. A zero current detector 12 detects current
through the switches 11 from the AC input, and provides
a signal to switching logic 13 when the current has
10 dropped to substantially zero. The switching logic
13 is preferably arranged to activate selected
switches 11 upon receipt of the signal from the zero
current detector 12, the switches being selected in
accordance with instructions received from a decision
15 circuit 14. The decision circuit 14 may be activated
by external signals in order to select the switch 11
to be made conductive, or may be made responsive to
a function of the load 10 as shown by the broken line
connection 15. A further alternative (not shown) is
20 that the decision circuit may be made responsive to a
parameter of the input to constitute a feedforward
rather than a feedback circuit.

As described above, a decision is made in
the decision circuit 14 as to whether a tap change is
25 required on the load, and if so which switch 11 is
to be energised to effect such tap change. The
decision is fed to the switching logic 13, and when
the detector 12 next detects a current zero, the
logic 13 is responsive to the current zero signal to
30 effect the necessary change of switch. Switching
therefore takes place at current zeros, and in the
case of a current sinewave, will take place at
current zero crossing points during each cycle.

In apparatus as described above, a decision
35 concerning a possible tap change is reached and held

until the next detected current zero enables the tap change to be effected. An alternative arrangement is that a signal indicative of a current zero is fed from the detector 12 to the decision circuit 14 (as shown
5 by broken line 16) and the decision is made at that instant and fed to the switching logic 13. In such an arrangement, there is no need to make a decision subsequent to detecting a current zero and thereafter holding that decision.

10 Figure 2 shows a circuit which may be used as an electronic line corrector, for stabilising variations in the input mains or line supply so that such variations in the output of the circuit are controlled to within limits set by the circuit.

15 In the embodiment to be described with reference to Figure 2, the AC mains supply is fed to a winding of a transformer and connection to the
20 tapplings of the transformer is controlled such that the output voltage from the transformer is constant within preset limits. If the electrical apparatus to be fed from the mains supply via the AC line stabiliser is an electric motor, it is not essential that an intermediary transformer be provided; the tapplings
25 may instead be provided directly on the motor windings. The transformer, if provided, may for certain applications be an isolating transformer having primary and secondary windings; alternatively, and in general preferably, it may be an auto-transformer having a
30 single winding provided with a plurality of tapplings for input and output.

Referring to Figure 2, the load 10 comprises an auto-transformer provided with a fixed tapping point, from which the output supply is derived. A
35 plurality of tapping points, in this case six, are also provided and each is connected to the corresponding switch 11 for connection to the input mains supply.

The switches 11 may be semiconductor triacs and are controlled in such a manner that a particular triac is operated in order to connect its tapping point to the input supply under the control of a control signal derived in this case from the output voltage. The control signal may be derived directly from the output tapping as shown, or may be produced by a separate isolated winding as will be described hereinafter.

The decision circuit 14 includes a peak detector, sample and timing circuit 20. The circuit 20 detects the peak of the input voltage waveform and a clock 21 is responsive to the detected peaks to provide a square wave, the transitions of which coincide with the peaks of the input voltage waveform to the stabiliser. The positive transitions of the square wave are preferably used to perform various timing operations within the circuits.

The circuit 20 also samples the output voltage peaks and compares each sample with pre-determined maximum and minimum values. Each sample is taken instantaneously at the peak of the input waveform and stored until it is updated by the next sample which occurs at the next peak of the same polarity. This approach yields a one cycle response time to errors.

The decision circuit 14 further includes an output error polarity and limit detector 22 which detects whether an output error exists and the polarity of this error. The detector 22 is responsive to the sample held in the circuit 20 and also detects whether either the top or the bottom taps are selected and inhibits attempts to select a higher tap when the top tap is selected, or a lower tap when the bottom tap is selected.

Circuit 14 also includes an up/down counter

23 which is clocked in the appropriate direction
by the error detector 22 when an output error exists.
During the first few cycles of operation this counter
is preset to the count corresponding to the tap which
5 produces the lowest output voltage.

The zero-current detector 12 is preferably
a non-linear resistance which has a high resistance
at low current and a low resistance at high current.
By sensing the voltage across the current detector 12,
10 low current levels can be detected without large power
losses at high currents. When the switches 11 are semi-
conductor devices such as triacs, the current detector
12 may be made responsive to a current below 3 milli-
amps, and preferably below 3 microamps, to indicate
15 a 'current zero'.

The switching logic circuit 13 includes a
gate drive timing circuit 24 which senses the voltage
across the current detector 12 and produces timed
pulses starting at zero current and lasting for a
20 pre-determined period. This section also provides a
pulse every alternate current zero; the rising edge
of this pulse clocks the up/down counter 23 thus
initiating a tap change if necessary. Clocking of
alternate current zeros ensures that a tap change
25 can only occur an even number of half cycles after
the previous tap change. If tap changes were allowed
to occur periodically after odd numbers of half
cycles, DC could be developed resulting in the
saturation of any transformer loads and of the
30 internal transformer 10.

The outputs of the up/down counter 23 and
the gate drive timing circuits 24 are fed to a drive
steering logic circuit 25 which steers the drive to
the required switch 11 and inhibits drive to the
35 remainder. If the up/down counter 23 is a BCD counter

as shown, a BCD-decimal converter 26 may be provided intermediate the counter 23 and the steering logic circuit 25. A drive circuit 27 amplifies the current from the steering logic 25 to a suitable level to
5 trigger the switches 11.

The apparatus preferably includes a start-up and shut down sequencing circuit 28 responsive to the input in order to inhibit the switches 11 when the apparatus is initially turned on. This allows the
10 auxiliary supplies to establish and the various capacitors in the control circuit to charge to their correct operating levels, thus avoiding spurious firing pulses and consequent tap changes during this period. During this inhibit period the up/down counter 23 is
15 pre-set to select the lowest voltage tap, i.e. the tap giving the lowest output voltage. At the end of the inhibit period, the pre-set tap selection is maintained for a number of e.g. the first six, cycles of operation thus giving the transformer and
20 non-linear loads time to settle down before attempting a tap change. The up/down counter 23 is then allowed to correct errors in the output by effecting changes of tap.

Transformers can draw a large inrush current
25 under certain circumstances. It is desirable to limit this current to ensure long life of the switches 11, particularly when these are semiconductor devices. This current is caused because when the transformer is disconnected from the supply, a remnant flux may
30 remain in the core; if power is restored at the beginning of a voltage half cycle that will flux the transformer in a direction nearer to saturation from remnance, the core can be fluxed to almost three times its working peak flux density. To minimise this effect,
35 the start-up inhibit period is timed to end on a peak

of the input voltage waveform, thus limiting the peak flux excursion immediately after switch-on.

5 In the event of more than a few half cycles being missing from the input waveform, there is the danger that the supply may be restored at a different amplitude to that at which it failed. There will have been no input voltage/^{peaks}during this period and so the up/down counter 23 will not have been clocked, therefore the possibility of an over voltage will exist.

10 To avoid this possibility a failed supply detector is incorporated in the sequencing circuit 28 to detect more than one cycle missing and initiate a full start-up sequence.

15 The start-up sequence is dependent on the method utilised to change taps. In one embodiment, which will be described in greater detail with reference to Figure 3 hereinafter, the lowest voltage tap is initially selected. During the first cycle, the output voltage is sensed at the peak of the input waveform by the circuit 20 and the output error detector 22 decides whether the output voltage is 'low' or 'correct'. If the output is low, a tap change to the next lowest voltage tap is enabled. The timing of this and of any further tap changes is set by the current zero detector 12 as described above.

25 The output voltage is thereafter sampled each cycle by the circuit 20 and further tap changes are initiated when required, but timed to occur at the next current zero. At each instant of voltage sense, the decision circuit 14 effectively decides if the output is 'low', 'correct' or 'high' and by altering the count in the up/down counter 23 in the requisite sense, will enable the unit to change one tap in the required direction, if necessary. Therefore the arrangement

35 is that the first tap to be selected is the one which

provides the lowest output voltage and the taps are then sequentially selected once every cycle of the input voltage, until the correct output voltage is achieved.

5 An alternative method is to provide a circuit which, rather than sequentially stepping through the switches 11, determines which tap should be selected on the basis of error detected in the output voltage, and enables the corresponding switch 11 to be rendered conductive without stepping through any
10 intermediate switches 11.

A circuit which may conveniently be used to effect such a method provides a series of voltage bands or windows, the width of which is proportional to corresponding voltages between transformer taps.
15 The output voltage is sampled as in the circuit 20 and is compared with the series of voltage windows. Thus, if the output of the sampling circuit 20 is in the n^{th} window, the n^{th} tap should be selected by closing the appropriate switch 11. If the switches 11 are
20 semiconductor devices such as triacs, they will turn off at zero current; therefore it is necessary to provide a memory so that if the input mains voltage is reasonably constant for a set period of time, the same triac will be conductive almost continuously. The
25 memory may be provided by an up/down counter similar to counter 23.

A more detailed circuit diagram of a line corrector which effects tap changes sequentially as described above is shown in Figure 3. In this Figure,
30 the switches 11 are shown as triacs and are referenced CSR1 to CSR6. Integrated circuit IC1 provides the control functions of peak detector 20, output error detector 22, up/down counter 23, BCD-decimal converter 26, drive steering logic 25, gate timing circuit 24
35 and sequencing circuit 28. Integrated circuit IC2

provides drive to the triacs and is equivalent to the drive circuit 27 of Figure 2.

At switch-on, an auxiliary transformer T2 provides a low voltage supply which is rectified by a bridge rectifier MR1 and regulated by an integrated circuit regulator IC4 to provide a stable DC supply of, for example 5V. During the time taken for the DC supply to be established, connection of the incoming AC line to the auto-transformer (10) input taps (t1-t6) is inhibited for a time as described above, e.g. approximately $2\frac{1}{2}$ seconds, i.e. there is no output from the unit during this inhibit period.

A further secondary winding on the auxiliary transformer T2 provides an A.C. signal to the clock circuit 21 which includes integrated circuit IC5, during and after the inhibit period. The clock circuit 21 provides a square waveform, the positive and negative edges of which occur at the same time as the voltage peaks of the incoming line voltage. The clock frequency therefore corresponds to mains frequency. At the end of the initial inhibit period the first positive going clock edge enables the control circuit to connect the incoming line to the lowest voltage tap t1 (i.e. the bucking tap). This is done to ensure that whatever the input line voltage is, within the operating range (e.g. 155V. to 265V.), an excessively high output voltage is avoided.

The AC signal from the transformer T2 for the clock circuit 21 is applied via resistor R1 to the inverting input of an operational amplifier IC5A, which acts as an integrator, the time constant of which is defined by capacitor C10 and resistor R1. The DC operating conditions are fixed, by DC feedback resistors R4 and R5 and AC decoupling capacitor C4, at half rail.

The output of the integrator, which leads the supply waveform by 90° , is fed via resistor R39 to the inverting input of comparator IC5B. In the absence of signal the non-inverting input is approximately at half rail (junction of R4 and R5) and to prevent multiple transitions, AC hysteresis is applied via C25, R37 and R38. The comparator IC5B output (square wave clock with edges coincident with supply voltage peaks) is supplied to pins 5 of IC1 (28 pin chip) to time various internal functions. The various waveforms associated with the integrator and comparator of the clock circuit 21 are drawn in Figure 4.

One of these functions is a "sample and hold" sequence which samples the output voltage as described for the peak detector sampling circuit 20 in Figure 2. The output from a low voltage secondary winding 30 on the auto-transformer 10 is applied via a potential divider comprising resistors R2/R3 and R36 to the control circuit IC1 at pin 6, the negative half cycles being clamped by a diode in IC1 as shown in the corresponding waveform in Figure 4. The positive half cycles are monitored by the circuit IC1 and samples are taken at times corresponding to negative going edges of the square wave clock and compared with upper and lower reference voltage window limits. The upper window limit is set by resistor R6 and zener diode D1 and applied to pin 7 of IC1, and is not adjustable once set by the component values. The upper tap change point is set by adjusting the proportion of voltage from the secondary 30 of transformer 10 fed to the circuit by means of changing the value of R3 in parallel with R2 in the potential divider chain.

The lower window limit (or lower tap change point) is then set by adjusting the reference voltage

obtained from the potential divider R8/R10 and R9, which is applied to pin 8 of IC1. These two adjustments are independent.

5 When correctly set up, the circuit compares the peak values of the positive half cycles of the output voltage of the apparatus with the latter upper and lower reference voltages, within the control circuit (IC1) and the control circuit generates a tap change enable instruction up or down, as required. This
10 corresponds to the function of the decision circuit 14 of Figures 1 and 2.

To further enable the tap change, and to ensure it actually takes place at a triac current zero the detector circuit 12 is used. This detector
15 comprises a resistor R24 which carries the triac current and two diodes (D2 and D3) in inverse parallel which afford a voltage clamp as the triac current exceeds a level which would develop more than approximately 1 volt across R24. A substantially square
20 wave is therefore developed across the detector 12 and is coupled to the control circuit IC1 via capacitor C9 and resistor R33, the latter limiting current into pin 9 during fault conditions e.g. if the voltage across R24 becomes significantly larger than 1 volt.
25 The control circuit IC1 generates a negative going edge coincident with triac current zero (=R24 voltage zero) which initiates drive to the next triac, up or down, further enabled by the sampled voltage as described above, at the current zero immediately
30 following.

Triac drive is supplied by darlington driver stages within integrated circuit IC2 and drive to a particular device is continuous until removed as a result of the control circuit indicating an
35 imminent tap change. This event is coincident with

the tap change enable instruction provided by the decision circuit 14 section of the control circuit and is prior to the actual tap change occurring at the next triac current zero.

5 The inhibit function of the sequencing circuit 28 which permits stabilisation of DC levels in the control circuit at switch-on, comprises C3, R7 and pin 28 of IC1 where, until C3 has charged to more than half the supply rail, no drive current is supplied to
10 any of the switches 11. An "Inhibit Reset" function is included, which as described above detects temporary line failure e.g. of more than three half cycles, and switches the unit off by triggering an inhibit period followed by a "switch-on" sequence.
15 This is to prevent the unit functioning erratically if the auxiliary supply rails decay, due to missing cycles of line voltage.

To provide the "Inhibit Reset" function current is taken from the positive output of bridge
20 rectifier MR1 via R12 to the base of transistor TR1, turning it on and thus discharging capacitor C6 which otherwise charges via resistor R11. (D4 prevents C11 turning on TR1). The voltage on C6 is monitored by the control circuit IC1 via pin 27
25 and an "Inhibit Reset" is initiated if it rises above half of the rail voltage (caused by three or more missing half-cycles). As long as the AC supply is present, TR1 is on and the potential of C6 remains near zero volts. Should pin 27 exceed the half rail
30 voltage, C3 is discharged by IC1 and a complete inhibit of, for example, $2\frac{1}{2}$ seconds is generated.

Capacitors C7 and C8 are for decoupling purposes.

Chokes L1 to L6 increase the high frequency
35 source impedance of the supply so that R-C networks (R25 and C24), (R26 and C23), (R27 and C22), (R28 and C21), (R29 and C20), and (R30 and C19) can snub

the dv/dt across the triacs. Once commutation of load current is complete the conducting choke is allowed to saturate. It may be possible to dispense with the chokes L1 to L6 dependent on the leakage characteristics of the transformer IO.

The varistor, VDRI is included to protect the triacs and attached equipment from voltage transients on the supply rails.

A capacitor C28 is included to suppress spurious resonances on the output, occurring between the snubber capacitors and transformer leakage inductances etc.

The sequence of operation is therefore that after the inhibit period and during the first cycle of connection to tap t1, the output voltage is sensed at a time dictated by the clock 21, and the control circuitry decides whether the output voltage is "low" or "correct". If the output is low, a tap change to tap t2 is enabled. The timing of this, and any further tap changes, is dictated by the current zero detector circuit 12.

The output voltage of the unit is sampled each cycle, timed by the "peak detector" clock 21 and further tap changes are initiated, when required, at "current zero" crossings. At each instant of voltage sense, the control circuit decides if the output is "low", "correct" or "high", and if necessary will enable the unit to change one tap in the required direction.

When a triac is conducting, it cannot turn off unless the current flowing between its two main terminals falls below the holding current. In the case of an AC load, this will occur just before the current reaches zero. If a tap change is required, the triac previously selected should not be conducting

when the new triac is triggered, otherwise both will conduct simultaneously and short the intermediate turns on the transformer resulting in very large circulating currents and possible failure of the output. If the triac, selecting the previous tap has been non-conducting for any length of time, the output voltage will have been absent for that length of time causing brown-outs of the load. The present circuit clocks the up-down counter and triggers the triacs on 'current-zeros', thus avoiding discontinuities of load current without having two triacs conducting simultaneously.

If the triac is driving a power factor load, the triac will turn off at zero current and must be turned back on immediately to avoid discontinuities. In the present circuit, this is achieved by providing a constant drive to the relevant triac which is interrupted only at zero current when a tap change is required. An alternative arrangement would be to provide a pulsed drive at a relatively high frequency which would be interrupted at zero current to provide a tap change when required.

Although as described above, the positive peaks of the output voltage are sampled and used to provide a tap-changing decision, other parameters may be sensed and a decision based thereon. For instance, the r.m.s. voltage may be sampled, or an average of the r.m.s. or peak voltages over several cycles, of either the output or the input voltages.

The above-described embodiment uses selectable taps on the input side of the transformer; however it is possible to alter the arrangement, such that the taps and associated switching devices can be on the output side of the transformer.

Although the switching devices have been

described as triacs, any other semiconductor switching device may be utilised depending on the particular application and load current required, for instance thyristors connected in inverse-parallel, or power MOSFETS might be utilised to select the transformer taps. Furthermore, mechanical switches such as relays may be suitable if designed so as to have a sufficiently rapid response time and therefore be capable of switching sufficiently close to the current zeros.

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CLAIMS:-

1. AC control apparatus for controlling a tapped load comprising a plurality of selectable switches connected to the load to alter the magnitude of the volt-amp product consumed by the load, and control means including means for determining which of the switches should be operative and zero current detecting means for detecting when the switch current is substantially zero, whereby a change in switch can be accomplished at a current zero.
2. Apparatus according to claim 1, wherein said means for determining which of the switches should be operative is arranged to make and hold a decision until a current zero has been detected thereby to enable the determined change in switch.
3. Apparatus according to claim 1 or 2 wherein said determining means is responsive to a parameter of the load.
4. Apparatus according to claim 1 or 2 wherein said determining means is responsive to a parameter of the input to the apparatus.
5. Apparatus according to claim 3 or 4 wherein said parameter is an instantaneous peak voltage.
6. Apparatus according to claim 3 or 4 wherein said parameter is the peak voltage averaged over a period of time.
7. Apparatus according to claim 3 or 4 wherein said parameter is the r.m.s. voltage averaged over a period of time.

8. Apparatus according to claim 3 or 4 wherein said parameter is the mean voltage averaged over a period of time.
9. Apparatus according to claim 6, 7 or 8 wherein said period of time is one or more half cycles of the input to the apparatus.
10. Apparatus according to claim 1 wherein said determining means is responsive to maintain a voltage parameter of the load substantially constant.
11. Apparatus according to claim 10 further including an error detecting means for detecting error in said voltage parameter.
12. Apparatus according to claim 10 wherein said determining means includes a clock circuit responsive to input voltage peaks for providing clock signals, and peak voltage detecting means responsive to said clock signals.
13. Apparatus according to any one of the preceding claims wherein said determining means is arranged to change switches no more than once in a cycle of the input voltage.
14. Apparatus according to any one of the preceding claims wherein said determining means is arranged to change switches in a manner to connect taps on said load sequentially.
15. Apparatus according to claim 14 wherein said control means further includes switching logic means responsive to signals from both said determining means and said zero current detecting means to effect a change in switch.

16. Apparatus according to claim 15 wherein said determining means includes counting means, said switching logic means being responsive to count information in said counting means to effect a change in switch.

17. Apparatus according to claim 16 as dependent on claim 2 wherein said counting means holds the count information and said switching logic means is responsive to said count information and to said signal from said zero current detecting means to effect a change in switch.

18. Apparatus according to claim 1 wherein said determining means is responsive to said current detecting means thereby to make a decision substantially instantaneously with a detected current zero.

19. Apparatus according to claim 18 wherein said determining means is further responsive to a parameter of the load.

20. Apparatus according to claim 18 wherein said determining means is further responsive to a parameter of the input.

21. Apparatus according to any one of the preceding claims wherein said load comprises an inductance device.

22. Apparatus according to claim 21 wherein said load comprises a transformer, a winding of said transformer being arranged to be connected to an external load.

23. Apparatus according to claim 22 wherein said switches are connected to a tapped input winding of said transformer.

24. Apparatus according to claim 22 wherein said switches are connected to a tapped output winding of said transformer.
25. Apparatus according to claim 21 wherein said load comprises a motor having tapped windings.
26. AC control apparatus for controlling a tapped load, said tapped load comprising a transformer having an output arranged to be connected to an external load, said apparatus further comprising a plurality of selectable switches connected to taps on said transformer, and control means including means responsive to a parameter of said output for determining which of the switches should be operative and zero current detecting means for detecting when the switch current is substantially zero, whereby a change in switch can be accomplished at current zero to control said output parameter.
27. Apparatus according to any one of the preceding claims wherein said switches comprise semiconductor switching devices.
28. Apparatus according to claim 27 wherein said switches comprise triacs.
29. Apparatus according to claim 28 further including drive means connected to said triacs for providing drive signals to said triacs, said triac drive means being responsive to said determining means and to said zero detecting means to provide said drive signals throughout substantially the whole of a cycle of the input voltage except when a change in triac is to be enabled.
30. Apparatus according to claim 29 wherein said drive signals comprise substantially D.C. signals.
31. Apparatus according to claim 29 wherein said drive signals comprise pulsed signals at a frequency substantially higher than the input AC frequency.

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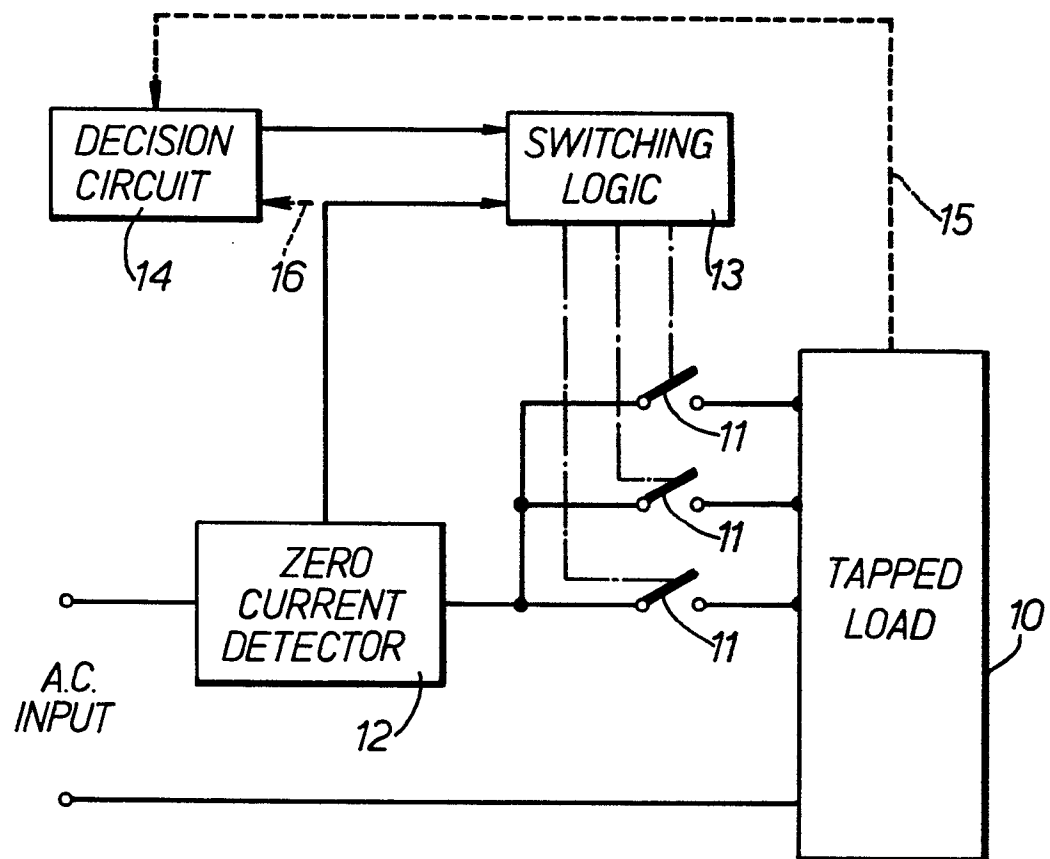


FIG. 1.

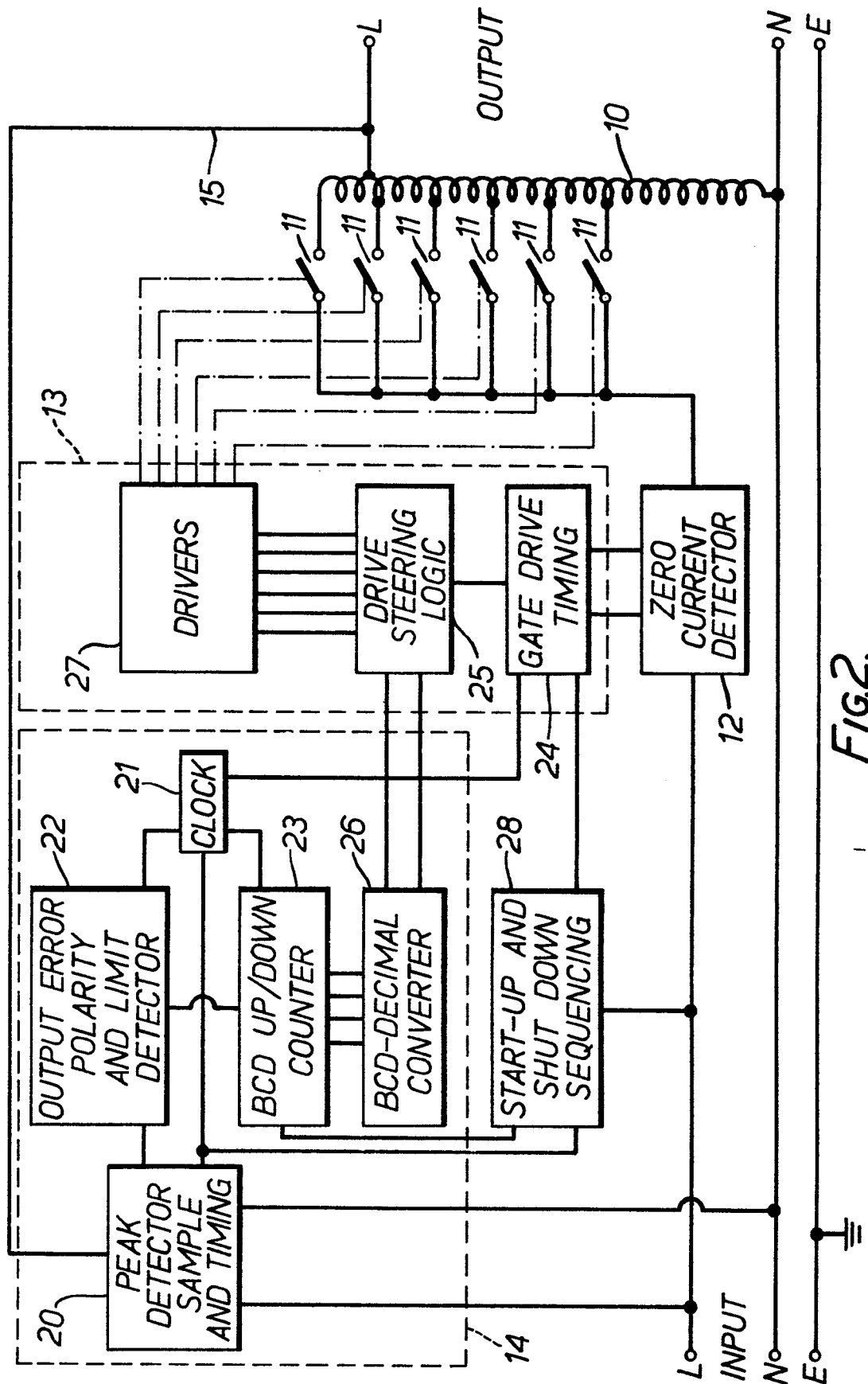


FIG. 2.



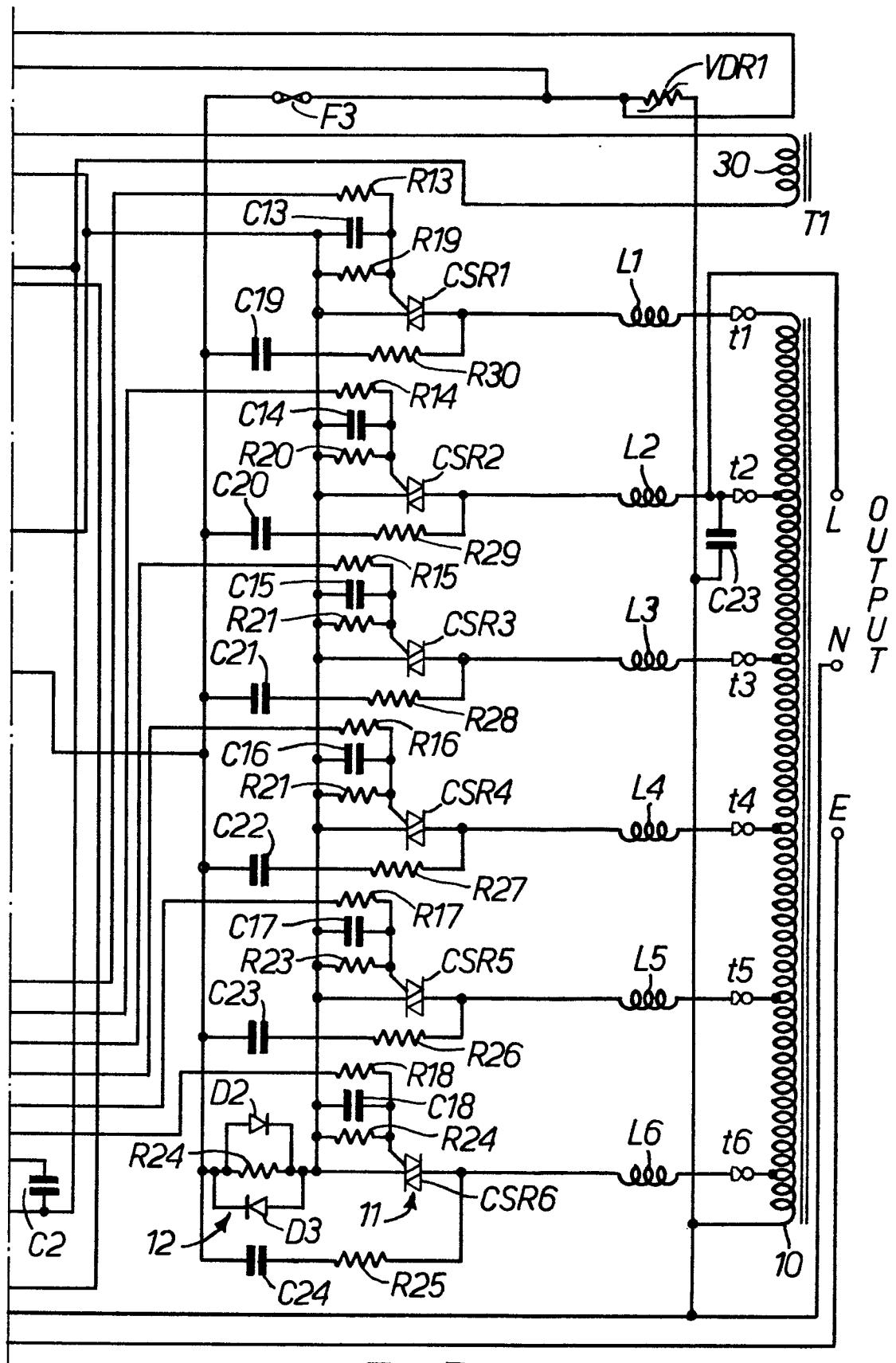


FIG. 3B.

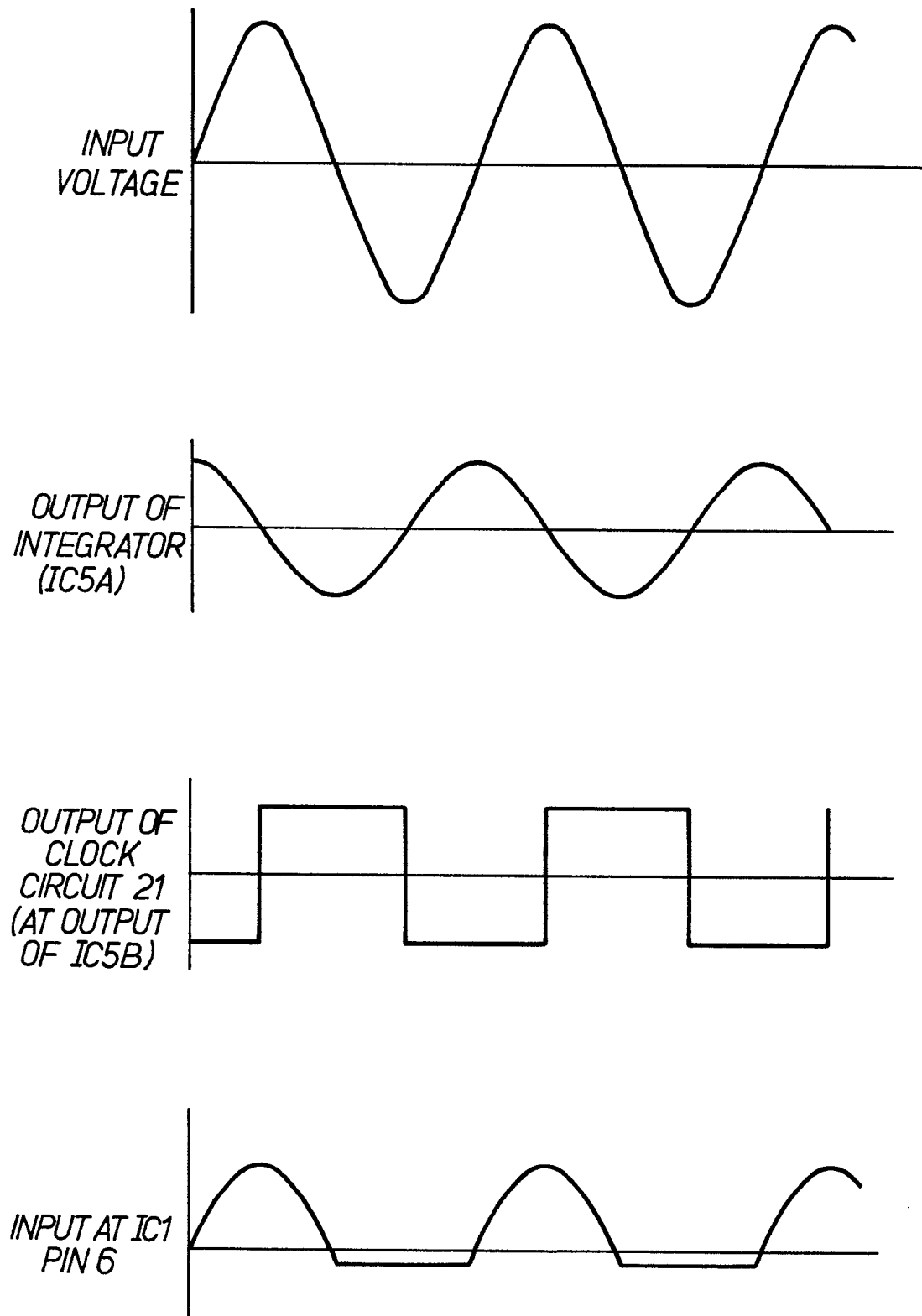


FIG. 4.



European Patent
Office

EUROPEAN SEARCH REPORT

0004462
Application number

EP 79 30 0461

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int. Cl. ²)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
X	<u>FR - A - 2 066 163</u> (SIEMENS AKTIEN GESELLSCHAFT) * Entire patent *	1-4, 10-11, 13, 15, 18-24 26-29	G 05 F 1/20
	-- <u>US - A - 3 388 319</u> (D.A. PAYNTER) * Column 1, line 1 - column 2, line 62 *	1-3, 7, 10-11, 18-19, 22-23, 26-27	
	-- <u>US - A - 3 818 321</u> (K. WILLNER et al.) * Whole patent *	1-4, 10, 11, 13, 15, 24, 26- 27	TECHNICAL FIELDS SEARCHED (Int. Cl. ²) G 05 F 1/20 1/14 1/16 1/18 1/22 1/30
			CATEGORY OF CITED DOCUMENTS
			X: particularly relevant A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention E: conflicting application D: document cited in the application L: citation for other reasons
			&: member of the same patent family, corresponding document
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
The Hague	29-05-1979	OOSTERLINCK	