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(54) **A digital eddy current apparatus for identifying specimens of electrically conductive material of unknown composition.**

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(73) Proprietor: **SENSOR CORPORATION**
303 Scottdale Avenue
Scottdale Pennsylvania 15683 (US)

(72) Inventor: **Mordwinkin, George**
303 Scottdale Avenue
Scottdale Pennsylvania 15683 (US)

(74) Representative: **Kern, Ralf M., Dipl.-Ing.**
Kern, Lang, Barg & Partner Patent- und Rechtsanwältsbüro Postfach 14 03 29
D-8000 München 5 (DE)

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Description

This invention relates to eddy current apparatus for identifying specimens of electrically conductive material of unknown composition, comprising

(a) driving means producing a square wave electrical signal;

(b) sensing means connected to the driving means and comprising an inductance, the impedance of which varies depending on eddy currents in the specimen induced by said inductance, and a capacitance connected with the inductance;

(c) converting means connected to the sensing means and converting the voltage waveform across the inductance into a rectangular pulse output, the rectangular pulse output being positioned at the center of one half of said square wave electrical signal when said capacitance is of such a value that the circuit comprising said inductance and capacitance resonates;

(d) means for varying the value of said capacitance over a range including the value at which said capacitance resonates with said inductance, and other values of capacitance larger and smaller than the resonating value, which other values produce voltage waveforms across the inductance which are out of phase with the square wave, the rectangular pulse resulting from the voltage waveforms produced with said larger and smaller values of capacitance being offset from the center of one half of the square wave, said offset being a function of the phase shift of the voltage waveforms relative to said square wave; and

(e) means coupled with the converting means for monitoring the values of the offset of the waveforms corresponding to the respective capacitance values so as to provide signals representing the relationship between capacitance and offset, which relationship is a function of the metallurgical characteristics of the specimen, the monitoring means comprising means for digitizing the amounts of the offsets of the converting means output pulses, and include a memory connected with the varying means holding capacitance-offset relations for specimens of electrically conductive material of known composition, and comparing means connected to the output of the digitizing means and the output of the memory so as to compare the successive digitized outputs of the offsets of the unknown specimen related to the successively varied capacitance values with the correspondingly digitized offsets of known specimens in the memory.

An eddy current testing equipment with the above features is known from US—A—4059795. This equipment presents the information in a form which can be digitized and used in a computer for instant analysis of metal characteristics or digitally displayed.

Prior to the technique disclosed in US—A—4059795 eddy current testing apparatus identified metals in accordance with their eddy current characteristics related to composition, hardness, heat treatment and the like, but did not present the information in a form which could be digitized and digitally displayed or used in a computer for rapid analysis. The apparatus disclosed in US—A—4059795 presents the desired information in digital form. It is not, however, fully automated because the optimum operating point in terms of the frequency of the probe current must be determined experimentally by the operator and exhibits a thermal drift of the inductance because of eddy currents generated in the metallic specimen.

It is an object of the invention to provide a fully automated apparatus which identifies metal specimens in digital terms, too, and which further automatically compares the digitized identification with predetermined digitized identifications of various metals and alloys stored in its memory so as to produce an output in terms of the grade of generic name of the specimen material, within a short time and without thermal drift of the inductance.

To solve this object the present invention provides an apparatus having the above features (a) to (e) and which is characterized in that the driving means are coupled to the sensing means through a constant-current driving device whereby thermal drift of the inductance of the sensing means is minimized and that the means for varying comprises an array of capacitors of different values, an array of control transistors and an address generator for sequencing the switching of said control transistors so that different combinations of capacitors are connected in sequence in circuit with said inductance such as to vary the value of said capacitance in steps over said range.

The resonating circuit comprises a coil and a capacitance connected in parallel. When a specimen to be identified is brought in proximity to the coil in a predetermined air gap, the eddy currents induced in the specimen bring about a change in the impedance of the coil and so change the resonant condition of the coil-capacitance combination. The output voltage, therefor, is thus altered both in amplitude and phase.

Means are provided for automatically changing in discrete steps the value of the resonating capacitance. Thus, the specimen is scanned, or its output phase measured for each resonant condition corresponding to a capacitance step. The non-linear change of phase of the signal voltage, which may be called a metallurgical signature of the specimen, is then stored in a computer-type memory.

The apparatus includes a reference memory in which are stored the metallurgical signatures of commercial grades of various metals and alloys, and means for comparing the metallurgical signature of the specimen with signatures stored in the reference memory.

The sensitivity of the apparatus is high enough

that it could present difficulties where metal grades with wide tolerances are concerned, or where there may be overlap between grades. To overcome that difficulty, the apparatus may comprise a digital tolerance control circuit which accommodates deviations between signatures, typically up to plus or minus nine counts.

The apparatus also may include means for displaying the stored signature which best matches the signature of the specimen, in terms of its commercial grade number or generic name.

A waveform generator provides a set of logic waveforms required for phase digitizing, for driving the inductance element, for automatic resonance scanning of the inductance and for automatic tolerance adjustment. All those waveforms are functions of the frequency input to the waveform generator so that change in that input frequency brings about automatic adjustment of all timing waveforms. In this way multiple frequency scanning operation is readily carried out.

Thermal drift in the inductance is circumvented in the present apparatus by the constant-current driving device for that inductance which maintains a constant current through the inductance regardless of change of resistance of the inductance winding. That constant current maintains the inductance of the winding at a constant value. Phase readings of the inductance output will therefore remain accurate regardless of the change in the ambient temperature. The amplitude of the output signal will vary in proportion to resonance change, and to the change in the resistive component of the sensing coil impedance, but in the apparatus, the phase change only is measured.

The apparatus includes a bias generator for the input stage of the signal amplifier that tracks the threshold level of the amplifier integrated circuit and compensates the input stage for thermal variations. This refinement makes possible extremely stable amplifier operation.

One way of carrying out the invention is described in detail below with reference to drawings which illustrate only one specific embodiment, in which:

Figure 1 is a block diagram of the apparatus in accordance with the invention;

Figure 2 is a timing diagram showing the waveforms developed by the present waveform generator;

Figure 3 is a schematic diagram of a crystal oscillator, constant current driver, and bias generator; and

Figure 4 is a schematic diagram of a resonance, scan control means.

The sensing means comprise an inductive sensing head 15 parallel by a capacitance selected from capacitor bank 16.

Figure 3 is a schematic diagram of the crystal oscillator 11, constant current driver 17, amplifier 18 and bias generator 19. These are all comprised in six-element buffer inverter integrated circuit U1 and JFET U8, together with auxiliary components to be mentioned.

Oscillator 11 comprises one element 36 of circuit U1 paralleled by feedback resistor 37, and crystal 38 in series with capacitor 39.

Constant-current driver 17 comprises transistor 40, which is element U8, connected in series with driver input voltage DR and ungrounded sensing input terminal SI. A limiting resistor 42 is interposed between terminal SI and the drain of transistor 40 to provide isolation between those elements and to prevent reactive shift influence on the constant-current supply and distortion of the square waveform of voltage DR.

Amplifier 18 comprises four elements 44—47 inclusive of buffer inverter U1 connected in cascade, the input of first stage 44 being coupled to ungrounded terminal SI by capacitor 43.

Bias generator 19 comprises element 48 of circuit U1 having its input connected to its output and to the input of element 44 through resistor 49.

The operation of the sensing means is the same as that of the sensing means in the aforementioned U.S. Patent 4,059,795.

The crystal controlled oscillator 11 of the driving means has a frequency in the range 1 MHz—10 MHz. The oscillator generates a square wave, F1 in Figure 2. A square wave, of course, is one having a very rapid rise and fall and a flat top so that its corners are right angles. The square wave F1 is supplied to a conventional frequency divider 12 which produces a range of frequencies F2 from MHz to KHz as may be required. The selected output F2 from frequency divider 12 is introduced into waveform generator 13. As will be described, that generator generates a number of frequencies, including a sensing or driving frequency, DR which is a square wave.

Sensing driving pulses DR which, as has been mentioned, have a frequency which is a derivative of frequency F2, are applied to the inductive sensing head 15 through constant current driver 17. The advantages of a constant current driver have been mentioned above.

The amplifier 18 is operated in the class C (saturated) mode so as to produce rectangular output pulses AM. The width of a pulse AM is proportional to the amplitude of the signal. The bias generator 19 is adjusted so that an output of amplifier 18 is secured at the lowest signal amplitude, which occurs at the extreme point of phase change. The signal pulse AM is located with reference to the driving waveform DR in direct proportion to the phase relation between those two signals, the signal pulse AM for resonance condition being positioned in the center of one half of the rectangular wave DR.

The basic cause of thermal drift in semiconductors is change in threshold voltage level at the semiconductor junction. That change directly affects the stability of the stage when it is used for amplification of small analog signals. The integrated circuit U1 used in amplifier 18 and bias generator 19 is uniquely adapted to thermal drift stabilization because all six elements are made from the same material and are closely spaced so as to display the same thermal drift

characteristics. Bias generator 19, having input of element 48 connected to its output, generates a DC voltage equal to the threshold voltage of the semiconductor junction of element 48 and all other elements of U1, as they are on the same silicon chip. That voltage instantaneously reflects any change in threshold voltage of all other elements on the same chip connected thereto and provides perfect drift compensation.

Resonance scan control and address generator

Resonance scan control 20 switches capacitors of capacitor bank 16 across inductive sensing head 15. It comprises buffer-drivers U11 and JFET analog gates U12 and U13.

The capacitor bank comprises 8 capacitors which are incorporated for convenience in two units, as is shown in Figure 1. The capacitors have values of 100, 200, 400, 800, 1600, 3200, 6400 and 12,800 mmf respectively, but other values may be used.

Figure 4 is a schematic diagram of the resonance scan control circuit 20 and its address generator 21. Eight capacitors 51—58 each have one terminal connected to a lead to ungrounded sensing terminal SI. The remaining terminals of each capacitor 55—58 are connected respectively to the drains of JFET transistors 65—67, and the remaining terminals of capacitors 51—54 are connected respectively to the drains of JFET transistors 59—62. The sources of transistors 64—67 are connected together and through compensating transistor 68 to ground. The sources of transistors 59—62 are connected together and through compensating transistor 63 to ground. The junctions of transistors 59—62 and 64—67 are connected to the outputs of buffer drivers 70—77, respectively. The inputs of those buffer drivers are connected to the outputs of eight-bit address generator 21 and also to reference memories 29 and 30, to be described hereinafter.

Address generator 21 comprises dual binary up-counter U20. Reset signal R from waveform generator 13 is connected to the clock input of the up-counter. Eight Q lines are used as addresses to select eight lower order addresses of memories 29 and 30, used to store the reference signatures. The same eight lines are used to switch sequentially analog gates U12 and U13 of resonance scan control 20 through buffer drivers 70—77.

The JFET transistors in analog gates U12 and U13 are bipolar and require no DC potential on their drains. The AC voltage across sensing inductance 15 is applied to the drains of transistors 59—62 and 64—67 through the capacitors in capacity bank C3 and C4, as appears from Figure 4.

A pulse from address generator 21 transmitted to buffer driver 77, for example, is passed on to the junction terminal of transistor 67, rendering it conductive so that the terminal of capacitance 58 connected to the drain of transistor 67 is connected to ground. That capacitor is thus shunted across terminals SI—SI_{com}. Other pulses from address generator 21 cause other capacitor elements to be connected to ground in the same way, so that an aggregate of 256 values of capacitance are switched in sequence across terminals SI—SI_{com}.

When a given specimen is positioned in inductive sensing head 15 there is, of course, only one value of capacitance from capacitor bank 16 which resonates the inductive sensing head at the frequency of sensing driver voltage DR. The voltage applied to amplifier 18 will have its maximum amplitude at that frequency, and will be approximately sinusoidal. All other values of capacitance will produce voltage inputs to amplifier 18 which are of lower amplitude and are out of phase with driver voltage DR, lagging or leading. Thus, if all 256 values of capacitance 16 are switched in sequence, the apparatus will provide 256 different outputs from amplifier 18, each differing from all others in amplitude and/or phase, constituting the metallurgical signature of the specimen. Apparatus to be described hereinafter digitizes this phase change only, and compares it with reference signatures stored in a memory to identify metal specimens of unknown composition.

Waveform generator

Waveform generator 13 comprises conventional integrated circuits conventionally connected to generate a set of logic waveforms all of which are submultiples of its input frequency F2, so that a change of input frequency automatically adjusts all timing frequencies.

Waveform generator 13 comprises decoder counter divider U3, dual flip-flops U4, U5 and U6, and hex "and" gate U10.

The driving frequency DR is a fixed submultiple of frequency F2. Preferably it is one-fortieth of F2. It is generated through decoder counter divider U3 and D type dual flip-flop U5. Tolerance control frequency TC is preferably fixed at one-tenth of frequency F2 and is generated by the same elements as is frequency DR, utilizing the other half of the dual flip-flop. Control pulses LE, update, and R, reset, are generated by "and" gating through one element of hex gate U10 frequency F2:2, which is one-half frequency F2, and an output from terminal 9 of decoder counter divider U3. Frequency F2:2 is generated by decoder counter divider U3 and half of flip-flop U4. Sensing window frequency WD is likewise generated through element U3 and half of flip-flop U6.

The decode counter divider U3 has 16 terminals, a number of which produce binary related timed outputs. Driving waveform DR is generated by the leading edge of pulses from terminals 3 and 1 which are used to set and reset one of the flip-flops U5. Tolerance control waveform TC is generated by the leading edge of pulses from terminals 5 and 9 applied to the other flip-flop of U5. Control pulses LE and R are generated by gating F2:2, generated by the pulses form terminal 13 and one flip-flop of U4, with the pulses

from terminal 9 of U3. Sensing window waveform WD is generated by the leading edges of the pulses from terminal 11 of U3 which set one flip-flop of element U6. The end of that waveform is generated by the pulses from terminal 5 of U3 which reset that flip-flop.

The waveform F2:4 in Figure 2 is a waveform used internally in waveform generator 13. It has a frequency one-fourth that of frequency F2 and is generated therefrom through one-half of flip-flop U4. It is used as a clock for decoder counter U3 in the generation of waveforms WD, DR, TC, LE and R.

The elongated width of the sensing window waveform WD is to allow proper digitizing of the phase component of the sensing pulse AM, to be described hereinafter, even in extreme locations of plus or minus 90 degree phase, when the signal pulse width could extend beyond the edges of the waveform DR.

Sensing window WD sets the time limits where the phase relation between DR waveform and signal output waveform AM is digitized. Waveform TC defines the time when the tolerance control circuit 14 is operative. Waveform LE defines the time when display and logic circuits 31—34 inclusive are updated. Waveform R is the system reset signal, resetting all elements connected thereto before the start of each sensing cycle. Pulse $U/_{DN}$ described in more detail hereinafter controls the up/down counters 23.

The TOLIN waveform to tolerance control 14 is waveform F2 but is gated by tolerance control waveform TC so as to be transmitted only during tolerance control period TC, generating ten pulses at the input of rate multiplier U23.

Phase digitizers and counters

Phase digitizer 22 comprises CMOS analog gate U24, two D type flip-flops U6 and U7, and "and" gate U9. Counters 23 comprise BDC Up/Down counters U14 and U15.

The purpose of the phase-digitizing circuit is to represent digitally the phase relation between driver reference waveform DR and the amplifier output pulse AM. That relation between two above mentioned signals is measured by counting the number of oscillator 11 pulses between the leading edge of the waveform WD and the center of the amplifier pulse AM.

The waveform WD is used instead of waveform DR so as to prevent a digitizing error when the pulse AM extends beyond the limits of waveform DR, especially when the phase angle of the signal is in the extreme position.

To achieve this goal the pulse train PC (phase count) is formed as follows:

At the leading edge of the waveform WD one of the analog gates of U24 is closed, feeding the F1 system clock pulses through terminal PC to counters U14 and U15.

As soon as the leading edge of pulse AM appears, the analog gate which feeds the F1 pulses opens, discountinuing further connection between F1 pulses and counters. At the same time another analog gate closes and feeds F1:2 pulses, which are at half rate of the F1 frequency, and which are generated by dividing F1 in one element of the flip-flops. When the trailing edge of AM appears, the second analog gate is also open.

No other pulses will reach line PC and counters 23 until the tolerance control period, during which a number of pulses (at the rate of frequency F2) may appear, if A=B condition of the digital comparator is not reached.

Digital tolerance control

The digital tolerance control circuit 14 consists of the rate multiplier U23 and tolerance switch 24.

In order to overcome the problem due to slight variations in the same alloys and grades of different heats, a special digital tolerance control circuit was developed. The purpose of this circuit is to provide a number of additional pulses through the phase count line PC to the counters, and achieve A=B condition between references and test signatures.

Selector switch 24 selects the maximum allowed digital deviation between reference and the sample. A single switch will allow up to +nine pulses to achieve a match, and acceptance of the metal under test. An extended range of tolerance control can be achieved by using more than one switch and rate multiplier U23.

The principle of the operation of the tolerance control circuits is as follows:

Ten pulses at the rate of the frequency F2 are fed to the input terminal CL of U23 (TOLIN).

The number of outputs (TOLOUT) will be determined by the setting of switch 24.

As soon as terminal A=B of the digital comparator connected to the terminal STR of U23 becomes "true", the rate multiplier U23 is inhibited until the next sensing cycle.

Tolerance control circuit 14 is reset by the system reset pulse R.

Reference, reference select and select switch

References 29 and 30 are CMOS EPROM memories U18 and U19 each having a storage capacity of 512×8 bits. In those reference memories 29 and 30 are stored the signatures of known metals and alloys for comparison purposes, as will be described. Select switch 27 provides manual selection of any signature from references 29 and 30 through reference select 28, which is a 4 bit latch/4-to-16 decoder. References 29 and 30 are also connected to be scanned by address generator 21.

Reference memories 29 and 30 are programmed by external memory programming means. Memories 29 and 30 store two signatures of 256 resonant points. They may also be programmed to store generic names of metallurgical signatures by reducing the number of resonance

points stored, for example to 240, and utilizing the remaining 16 locations for generic names of codes numbers, such as "SAE 1010" and the like.

Digital comparator and output latch

Digital comparator 26 comprises two digital comparator units U16 and U17. Their A inputs are connected to counters U14 and U15 of counter 23. Their B inputs are connected to one or the other of reference memories 29 and 30. The outputs of comparator 26 are A=B and A>B.

Output latch 25 is a D type flip-flop U7. The A=B signal of comparator 26 is applied to the "Data" input of output latch 25, and to tolerance control 14. The update LE signal is connected to the clock input. The A>B signal is applied to waveform generator 13.

The A=B signal operates latch 25 to the accept position ACC and inhibits tolerance control 14. This occurs only when the signals from counter 23 and reference memory 29 or 30 match at the time the LE signal arrives.

The A>B signal triggers a pulse $U/_{DN}$ from waveform generator 13 which controls the up/down mode of the BCD up/down counters 23 during the tolerance control period TC. When the counter input to comparator 26 is larger than the reference input, the A>B signal will switch counter 23 to the count-down method until A=B condition is reached, or until the end of the TC period is reached. In the latter event latch 25 will latch in the reject position REJ. The accept or reject signals ACC and REJ may be applied to any convenient visual display, audible signal means or machine control function.

Digital comparator 26 also has an A<B output which is unused. Counters 23 are normally in the up-count mode and when the A<B condition obtains those counters automatically count up until the A=B condition is reached, or until the end of the TC period is reached.

Display

The display apparatus is conventional and comprises display memory and decoder 31 comprising 32×8 random access memory U25 and 4 bit latch/4-to-16 decoder U26, segment drivers 32, alpha-numeric display 33, comprising 14 segment alpha-numeric LED display DP1 and DP2, and digit selector 34, 4 bit latch/4-to-16 decoder U26.

The outputs of reference memories 29 and 30 are connected to the input of display memory and decoder 31, as are the outputs of resonance scan control 20 and the accept signal ACC. The outputs of resonance scan control 20 are also connected to digit selector 34.

When address position 240 is reached and all 240 positions show a match between the stored signature and the signature of a specimen, the address signal is advanced through positions 241—256 of the reference memory 29 or 30, and the contents of those locations are transferred to random access memory 31. As long as the A=B condition obtains at the output of digital comparator 26 during the time of up-date signal LE, that memory is continuously multiplexed through digit selector 34 and displays the transferred data which contains the generic name or code of the specimen.

The 16 digits, 241—256 accommodate all generic names or grades of signatures stored in memories 29 and 30.

A list of standard and commercially available components used in the above described equipment is as follows:

Code	Designation	Function	Source
U1	MC14049	Buffer/Inverter	Motorola
U2	MC14040	Frequency Divider	Motorola
U3	MC14017	Decode Counter/Divider	Motorola
U4, U5, U6 and U7	MC14013	"D" type Flip/Flop	Motorola
U8	2N5457	Transistor	Motorola
U9	MC14081	"AND" Gate	Motorola
U10	MC14572	Hex Gate	Motorola
U11	DS8863	Buffer/Drivers	National
U12, U13	IH5009	Analog Gate (2 FET)	Intersil
U14, U15	CD4029	BCG Up-Down Counter	RCA
U16, U17	MC14585	Digital Comparator	Motorola
U18, U19	IM6604	EPROM (512×8)	Intersil
U20	MC14520	Dual Binary Up Counter	Motorola
U21	MC14515	4 Bit Latch/4-to-16 Decoder	Motorola
U23	MC14527	BCD Rate Multiplier	Motorola
U24	MC14066	CMOS Analog Gate	Motorola
U25	CDP 1824	32×8 RAM	RCA
U26	MC14514	4 Bit Latch/4-to-16 Decoder	Motorola
DP1, DP2	MAN2815	14 Segment Alpha-Numeric LED Display	Monsanto
DP3	UDN2982	Segment Drivers	Sprague

Claims

1. Digital eddy current apparatus for identifying specimens of electrically conductive material of unknown composition, comprising

(a) driving means (17) producing a square wave electrical signal (DR);

(b) sensing means connected to the driving means (17) and comprising an inductance (15), the impedance of which varies depending on eddy currents in the specimen induced by said inductance, and a capacitance (16) connected with the inductance;

(c) converting means (C2, 18) connected to the sensing means and converting the voltage waveform across the inductance into a rectangular pulse output, the rectangular pulse output being positioned at the center of one half of said square wave electrical signal when said capacitance is of such a value that the circuit comprising said inductance and capacitance resonates;

(d) means (13, 20, 21) for varying the value of said capacitance over a range including the value at which said capacitance resonates with said inductance, and other values of capacitance larger and smaller than the resonating value, which other values produce voltage waveforms across the inductance which are out of phase with the square wave, the rectangular pulse resulting from the voltage waveforms produced with said larger and smaller values of capacitance being offset from the center of one half of the square wave, said offset being a function of the phase shift of the voltage waveforms relative to said square wave (F1); and

(e) means (22, 23, 26, 31, 21, 29, 14, 13) coupled with the converting means for monitoring the values of the offset of the waveforms corresponding to the respective capacitance values so as to provide signals representing the relationship between capacitance and offset, which relationship is a function of the metallurgical characteristics of the specimen, said monitoring means comprising means (22) for digitizing the amounts

of the offsets of the converting means output pulses, and including a memory (29, 30, 31) connected with the varying means holding capacitance-offset relations for specimens of electrically conductive material of known composition, and comparing means (26) connected to the output of the digitizing means (22) and the output of the memory (30, 31) so as to compare the successive digitized outputs of the offsets of the unknown specimen related to the successively varied capacitance values with the correspondingly digitized offsets of known specimens in the memory characterized in that the driving means (17) are coupled to the sensing means through a constant-current driving device whereby thermal drift of the inductance (15) of the sensing means is minimized and that the means for varying comprises an array of capacitors (51—58) of different values, an array of control transistors (59—67) and an address generator (21) for sequencing the switching of said control transistors so that different combinations of capacitors are connected in sequence in circuit with said inductance such as to vary the value of said capacitance in steps over said range.

2. Apparatus according to claim 1 characterized in that the constant-current driving device comprises a transistor (40) connected in series with the driving means (17) and the sensing means (15).

3. Apparatus according to claim 1, characterized in that the converting means (e.g. 13) comprise a class-C operated signal amplifier (18).

4. Apparatus according to claim 3, characterized in that the signal amplifier (13) is an integrated circuit, and that said apparatus includes a bias generator (19) connected to the input of the amplifier (18), said bias generator (19) being physically a part of said integrated circuit and being adjusted to generate a direct current bias voltage equal to the threshold voltage of the input of the amplifier (18).

5. Apparatus according to claim 4 characterized in that the bias generator (19) is an amplifier element having its input connected to its output and to the input of the signal amplifier (18).

6. Apparatus according to one of preceding claims 1—5 characterized by a tolerance control apparatus (14) comprising means connected with the means (22) for digitizing the amounts of the offsets for adding thereto a fixed predetermined number of pulses.

7. Apparatus according to one of preceding claims 1—5 characterized in that the memory (29, 30) holds in conjunction with capacitance-digitized offset relations for specimens of electrically conductive materials of known composition the common designation of those specimens, and that the apparatus further includes display means (31, etc.) connected with that memory (29, 30) and with the scanning means (e.g. 20, 15) for displaying the common designation corresponding to the capacitance-digitized offset relation of the unknown specimen.

Patentansprüche

1. Auf Wirbelstrombasis arbeitendes Detektorgerät zur Identifizierung von Testkörpern aus einem elektrisch leitfähigen Material unbekannter Zusammensetzung, bestehend aus folgenden Einheiten:

(a) einem Treiberkreis (17), welcher ein Rechtecksignal (DR) erzeugt,

(b) einem mit dem Treiberkreis (17) verbundener Abtastkreis, welcher aus einer Induktivität (15) und einer Kapazität (16) aufgebaut ist, wobei die Induktivität in Abhängigkeit der durch Induktion innerhalb des Testkörpers auftretenden Wirbelströme veränderlich ist,

(c) eine mit dem Abtastkreis verbundene Wandlerschaltung (C218), welche das von der Induktivität (15) abgegebene Signal in ein Rechtecksignal umwandelt, wobei die einzelnen Impulse des Rechtecksignals im Bezug auf das Rechtecksignal (DR) des Treiberkreises (17) mittig angeordnet sind, sobald die Induktivität (15) und die Kapazität (16) sich in Resonanz befinden,

(d) einem Einstellkreis (13, 20, 21), mit welchem die Kapazität über einen weiten Kapazitätsbereich veränderbar ist und Kapazitätswerte größer und kleiner als der Resonanzwert eingestellt werden können, bei welchen Werten das von der Induktivität (15) abgegebene Signal phasenmäßig gegenüber dem Rechtecksignal des Treiberkreises versetzt ist und demzufolge die Rechteckimpulse des abgeleiteten Rechtecksignals bei den betreffenden größeren und kleineren Kapazitätswerten gegenüber dem Mittelwert des Rechtecksignals des Treiberkreises (17) verschoben sind, wobei die zeitliche Versetzung eine Funktion der Phasenverschiebung des abgeleiteten Rechtecksignals in Bezug auf das Ausgangssignal (F1) ist und

(e) eine mit dem Verstellkreis verbundene Auswertschaltung (22, 23, 36, 31, 21, 29, 14, 13), welche die Werte der Versetzung der Rechtecksignale entsprechend jeweiligen Kapazitätswerten überwacht und Signale entsprechender Beziehung zwischen der Kapazität und der Versetzung abgibt, wobei diese Beziehung eine Funktion der metallurgischen Eigenschaften des Testkörpers ist, wobei die Auswertschaltung einen Phasendigitalisierkreis (22) zur Digitalisierung der Größe der Versetzungen der umgewandelten Ausgangsimpulse, Speicher (29, 30, 31) zur Einspeicherung der Kapazitätsversetzungsabhängigkeiten für Testkörper aus einem elektrisch leitfähigen Material unbekannter Zusammensetzung sowie eine mit dem Phasendigitalisierkreis (22) und den Ausgängen der Speicher (29—30) verbundene Digitalvergleichsschaltung (26) aufweist, welche aufeinanderfolgende digitalisierte Ausgangssignale mit Verschiebungen des unbekannten Testkörpers in Bezug auf aufeinanderfolgende veränderte Kapazitätswerte mit entsprechenden digitalisierten Versetzungen von bekannten Testkörpern vergleicht, dadurch gekennzeichnet, daß der Treiberkreis (17) mit dem Abtastkreis über eine

Konstantstromquelle verbunden ist, welche die thermische Drift des induktiven Detektorkopfes (15) geringhält, und daß der Verstellkreis mit einer Mehrzahl von unterschiedlichen Kapazitätswerte aufweisenden Kondensatoren (51—58) versehen ist, welche über entsprechende Steuertransistoren (59—67) von einem Adressiergenerator (21) derart ansteuerbar sind, daß die unterschiedlichen Kombinationen von Kondensatoren zeitlich hintereinander mit der Induktivität (15) verbindbar sind, um auf diese Weise den Kapazitätswert stufenweise über einen weiten Bereich zu verändern.

2. Detektorgerät nach Anspruch 1, dadurch gekennzeichnet, daß die Konstantstromquelle mit einem Transistor (40) versehen ist, welcher in Serienschaltung zu dem Treiberkreis (17) und dem Detektorkopf (15) angeordnet ist.

3. Detektorgerät nach Anspruch 1, dadurch gekennzeichnet, daß der Wandlerkreis (beispielsweise 13) ein in der Klasse C betriebener Signalverstärker (18) ist.

4. Detektorgerät nach Anspruch 3, dadurch gekennzeichnet, daß der Signalverstärker (18) ein integrierter Schaltkreis ist, und daß zusätzlich ein mit dem Eingang des Verstärkers (18) verbundener Vorspannungsgenerator (19) vorgesehen ist, welcher in physischer Hinsicht Teil des integrierten Kreises ist und dabei derart eingestellt ist, daß er ein Gleichspannungssignal erzeugt, welches gleich der Schwellwertspannung am Eingang des Verstärkers (18) ist.

5. Detektorgerät nach Anspruch 4, dadurch gekennzeichnet, daß der Vorspannungsgenerator (19) eine Verstärkerstufe (48) aufweist, deren Ausgang mit ihrem Eingang und dem Eingang des Signalverstärkers (18) verbunden ist.

6. Detektorgerät nach einem der Ansprüche 1 bis 5, dadurch gekennzeichnet, daß ein Toleranzsteuerkreis (14) vorgesehen ist, welcher mit dem Phasendigitalisierkreis (22) derart verbunden ist, daß zu der Größe der Phasenversetzungen eine vorgegebene Anzahl von zusätzlichen Impulsen hinzuaddierbar ist.

7. Detektorgerät nach einem der Ansprüche 1 bis 5, dadurch gekennzeichnet, daß zwei Referenzspeicher (29, 30) vorgesehen sind, in welchen die kapazitätsdigitalisierten Phasenversetzungen für Testkörper aus elektrisch leitfähigem Material bekannter Zusammensetzung einspeicherbar sind, und daß die beiden Referenzspeicher (29, 30) sowie der Abtastkreis (beispielsweise 20, 15) mit einer Anzeige (31 etc.) verbunden ist, mit welcher die gewöhnliche Bezeichnung entsprechend der kapazitätsdigitalisierten Phasenversetzung eines unbekannten Testkörpers zur Anzeige bringbar ist.

Revendications

1. Appareil digital de courant parasite pour identifier des specimens d'un matériel conductif d'une composition inconnue comprenant:

(a) un circuit d'exitateur produisant un signal rectangulaire DR.

(b) un circuit de mesure lié au circuit d'exitateur (17) et comprenant une inductance dont l'impedance varie suivant les courants parasites dans le specimen induit par l'inductance et une capacitance (16) liée à l'inductance.

(c) un circuit de conversion (C2 18) lié au circuit de mesure et convertant le signal apparaissant à l'inductance à des impulsions rectangulaires étant positionnés au centre du signal d'exitation, quand la capacitance a une telle valeur que l'inductance et la capacitance sont en resonance.

(d) des moyens (13, 20, 21), pour varier la valeur de la capacitance à travers un rayon, lequel inclut aussi la valeur à laquelle la capacitance est en résonnance avec l'inductance et incluant aussi d'autres valeurs de capacitance plus larges et plus petites que la valeur de résonnance les autres valeurs produisant des ondes à l'inductance défasées par rapport au signal rectangulaire, le défasement par rapport au centre du signal rectangulaire étant une fonction du déplacement de phase des ondes relative au signal rectangulaire F1, et

(e) des moyens (22, 23, 26, 31, 21, 29, 14, 13) accouplés avec le circuit de conversion pour registrer les valeurs de déplacement des ondes correspondant à des valeurs de capacitance ainsi produisant des signaux représentant la relation entre la capacitance et le déplacement de phase qui est une fonction des caractéristiques métallurgiques du spécimen, ces moyens comprenant un circuit de digitalisation de phases (22) pour digitaliser le déplacement de phases des impulsions et des mémoires (29, 31, 30) pour mémoriser les relations de capacité déplacement de phases pour des spécimens de matériaux conductifs de composition connue et un circuit de comparaison digital (26) lié à la sortie du circuit de digitalisation de phase (21) et des mémoires (30, 31) pour comparer les sorties digitalisées successives de déplacement de phases d'un spécimen inconnu avec le déplacement de phase digitalisée d'un spécimen connu mémorisé dans la mémoire, caractérisé en ce que, le circuit d'exitation (17) est lié à travers un exitateur de courant constant à la tête de mesure (17), ainsi réduisant la dérivée thermique de l'inductance de la tête de mesure (15) et qu'il est prévu additionellement un arrangement de condensateurs (16) avec des condensateurs (51—58) de valeur différente et un arrangement de transistors (59—67) et un générateur d'adresses (21) pour commuter ces transistors (59—67) d'une telle manière que, des combinaisons différentes de capaciteurs (51—58) sont liés en séquences aux circuit de mesure avec la tête de mesure (15) variant ainsi la valeur de capacitance en marche à travers le rayon donné.

2. Appareil suivant revendication 1, caractérisé en ce que, l'exitateur de courant constant (17) comprend un transistor à effet de champ à jonction (40) lié en série avec l'exitateur (17) et la tête de mesure (15).

3. Appareil suivant revendication 1, caractérisé en ce que, le circuit de conversion (13) est prévu avec un amplificateur (18) opéré dans la classe C.

4. Appareil suivant la revendication 3, caractérisé en ce que, l'amplificateur (18) est formé d'un circuit intégré et qu'il est prévu un générateur de tension de polarisation (19) lié à l'entrée de l'amplificateur (18), ce générateur (19) physiquement formant partie du circuit intégré et étant ajusté d'une telle manière qu'il produit une tension de polarisation de courant continu égal à la valeur de celle de tension à l'entrée de l'amplificateur (18).

5. Appareil suivant la revendication 4, caractérisé en ce que, le générateur de tension de polarisation (19) est un élément de l'amplificateur (48) dont la sortie est liée à son entrée et à l'entrée de l'amplificateur (18).

6. L'appareil suivant une des revendications précédentes caractérisé en ce que, le circuit de réglage de tolérance (14) comprend un élément lié au circuit de digitalisation de phase (22) en ajoutant un nombre d'impulsion prédeterminées au déplacement de phases digitalisés.

7. Appareil suivant une des revendications 1 à 5 caractérisé en ce que, les mémoires de référence (21, 30) servant à la mémorisation des relations de capacitance et de déplacement de phases digitalisées pour des spécimens de matériaux conductifs de composition connue mémorise aussi les désignations communes de ces spécimens et qu'en outre, il est prévu un appareillage d'affichage (21, etc) lié au mémoire de référence (29, 30) et au circuit de mesure (par ex. 20, 15) pour afficher la désignation commune du spécimen inconnu.

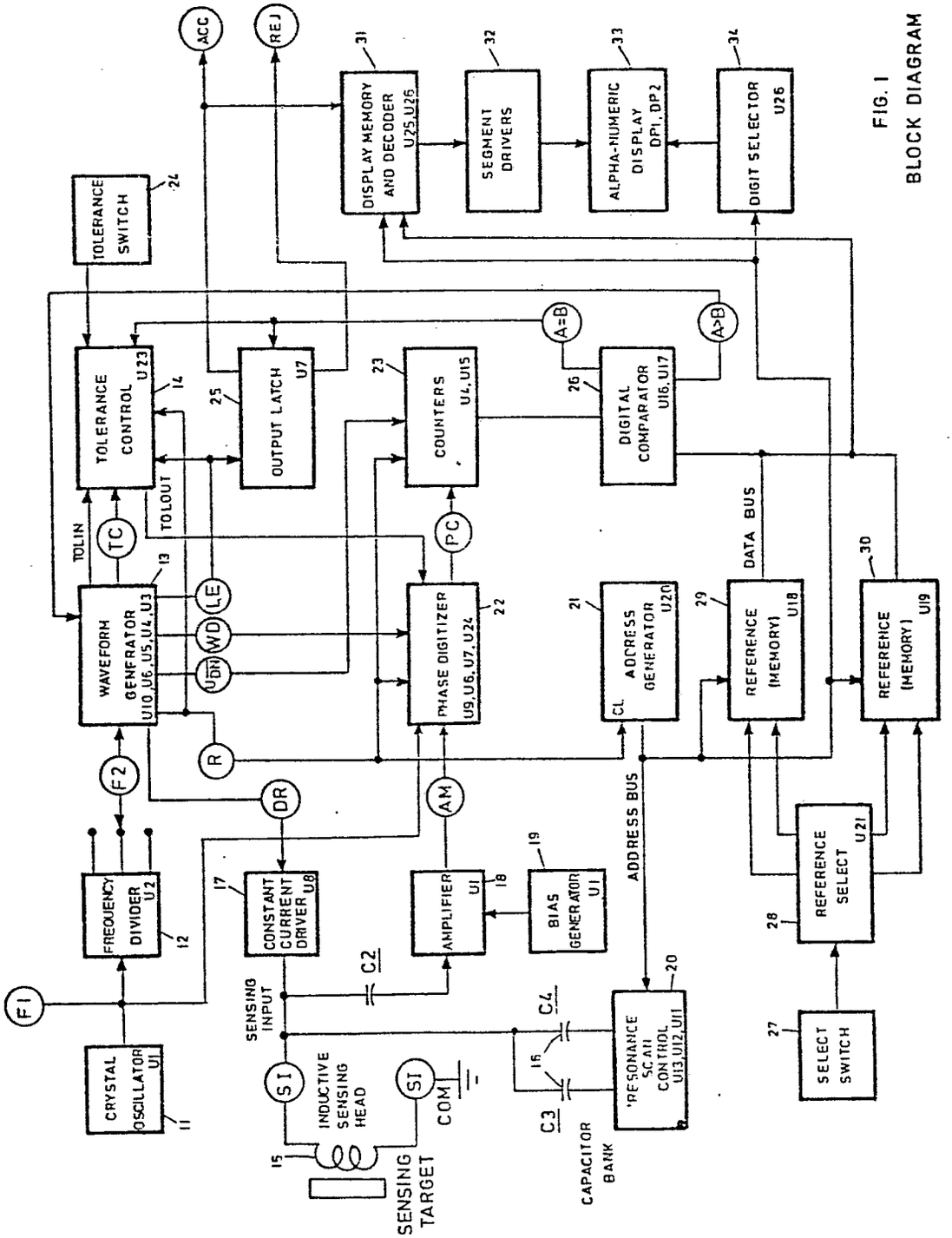

FIG. 1
BLOCK DIAGRAM

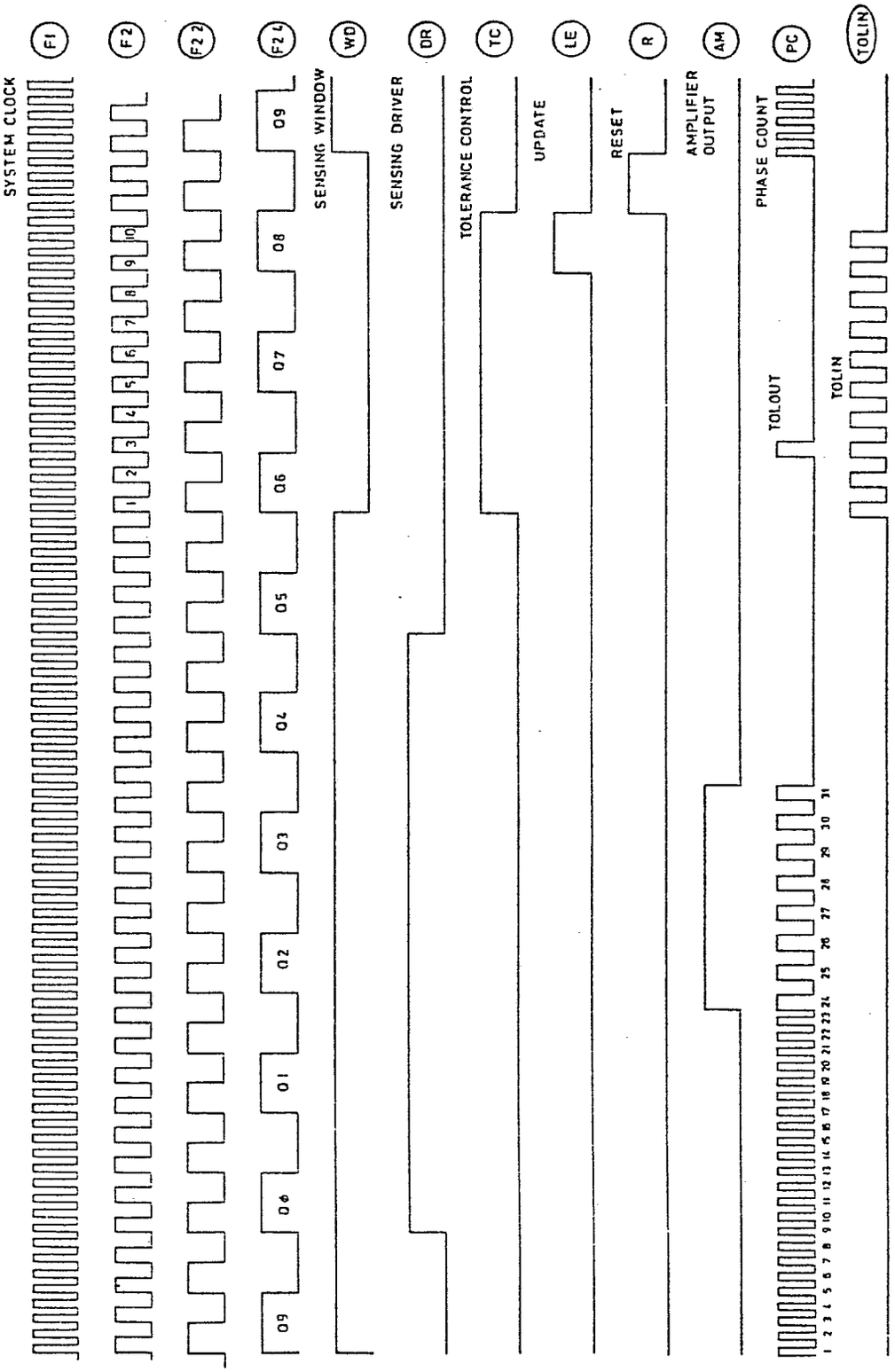

FIG. 2
TIMING DIAGRAM

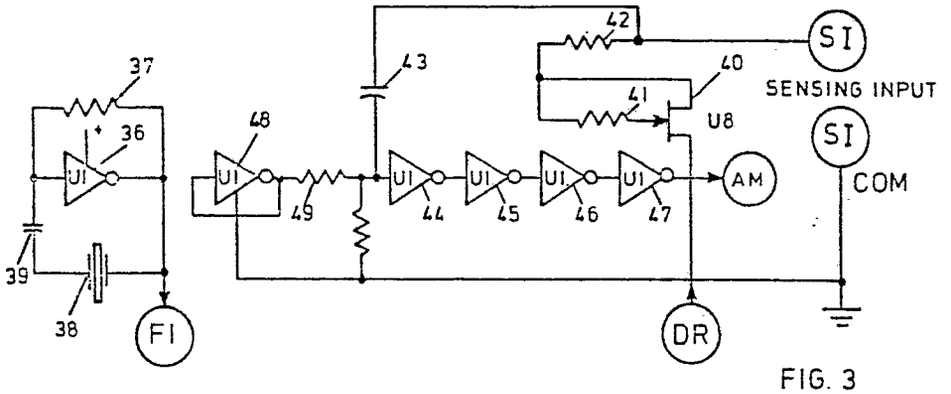
37
36
U1
39
38
FI
48
49
43
42
40
41
U8
SI
SENSING INPUT
SI
COM
44
45
46
47
AM
DR

FIG. 3

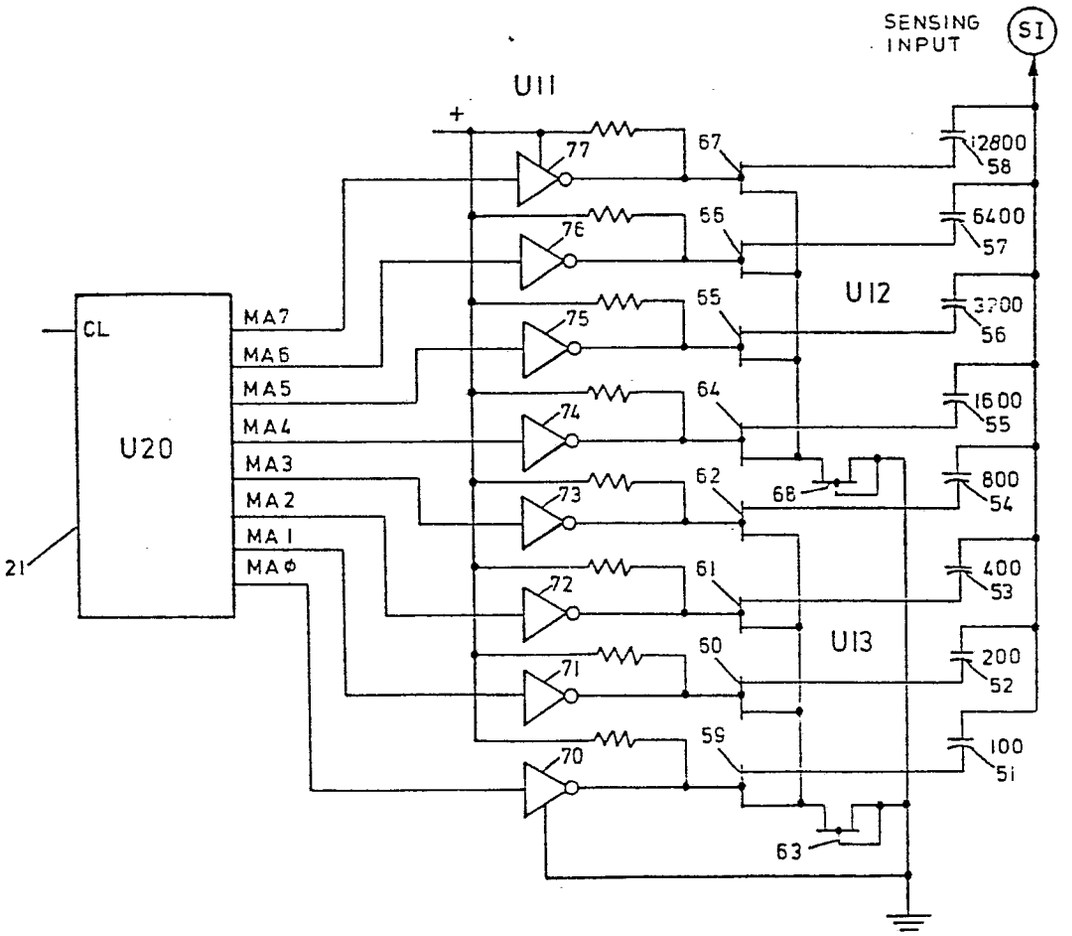
SENSING INPUT
SI
U11
+
77
76
75
74
73
72
71
70
67
66
65
64
62
61
60
59
2800
58
6400
57
3200
56
1600
55
800
54
400
53
200
52
100
51
U12
U13
68
63
CL
U20
21
MA7
MA6
MA5
MA4
MA3
MA2
MA1
MAΦ

FIG. 4