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(54) **Alpha-numeric character display.**

(57) An alpha-numeric character generator arrangement having as a character store a "read-only" memory in which characters are stored in a character format composed of a co-ordinate matrix (e.g. a 7 x 5 dot matrix) of discrete character elements. One aspect of the invention resides in storing the descender letters g, j, p, q and y such that those elements forming the "tail" of the descender letter are stored in character element rows which in a given row addressing sequence for the store precede the character element rows in which the remaining elements for the descender letter are stored. Another aspect of the invention resides in addressing the character element rows of the character store in a partially cyclic manner such that descender letters are read-out for display in a "lowered", correctly aligned, position in a row of displayed characters.
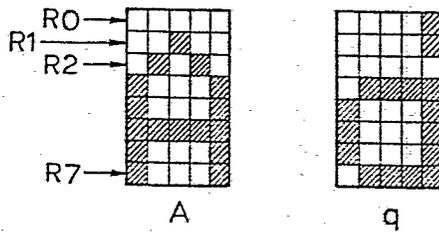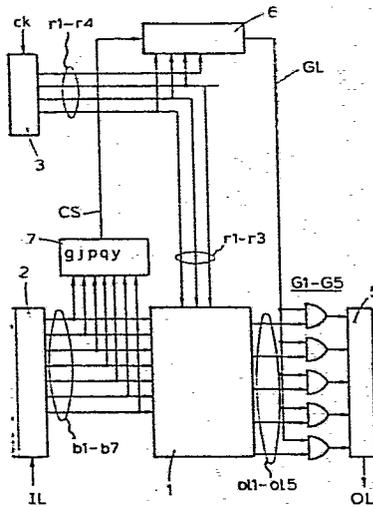
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Fig.6

Fig. 8

ALPHA-NUMERIC CHARACTER DISPLAY

This invention relates to alpha-numeric character display by electrical means (e.g. on the screen of a television monitor or using an electrically-operated printer device), and more especially to character generator arrangements for controlling the display of
5   characters in a character display system.

It is known to use in such a character generator arrangement a "read-only" memory device, which serves as a character store in which characters are stored in a manner representing a character format composed of a co-ordinate matrix of discrete character
10   elements, and which is responsive to character input data representing alpha-numeric characters to produce character generating data which can be used for the display of the alpha-numeric characters.

Such a character generator arrangement may therefore be of
15   a kind comprising, in addition to the character store, input addressing means for addressing the character store with character input data for a character selected for display, row selection means for producing row addresses for selecting for a read-out operation from the character store those character elements in a
20   particular character element row of the character matrix, data output means for producing in said read-out operation the character generating data for the character elements in the selected character element row of the selected character, and logic control means for so controlling the input addressing means and the row

selection means as to cause, for a plurality of characters to be
displayed as a row of characters, the selection in turn of the
character elements in a first character element row of each of said
plurality of characters, then the selection in turn of the character
elements in a second character element row thereof, and so on for
their remaining character element rows, so that said plurality of
characters are built-up element row-by-element row, as a whole,
for display.

In order to limit the size of a "read-only" memory device
which serves as a character store, it is known to provide for a
particular character format a co-ordinate character matrix of n
character element rows which is just large enough to accommodate
each of the upper case letters of the alphabet. The same size of
character matrix can also accommodate each of the corresponding
lower case letters. However, the lower case letters g, j, p, q,
and y, which are known as descender letters because they have "tails"
which should descend below the bottom of a displayed character row
in which they occur, can only be accommodated in their respective
character matrix if they are, in effect, stored in a "raised"
position in the matrix, since otherwise their "tails" would lie
outside the matrix and thus would not be accommodated therein. As
a consequence, a character generator arrangement of the above kind
having such a character store requires additional circuitry in its
logic control means for the read-out of these descender letters in
order to "lower" a descender letter, as displayed, into its correct
position in a character row. Without such additional circuitry a
displayed descender letter would be out of alignment in the
character row.

It is known for the additional circuitry to include an adder
circuit to which the row addresses from the row selection means are
applied and which is made operable by detector means when said
character input data represents a descender letter to add to each
successive row address applied to it a number appropriate for
changing the row address to delay the read-out operation in respect
of the descender letter by a number of character element rows
corresponding to said number, whereby the descender letter as

displayed is lowered in position by such number of character

element rows so as to be in correct alignment in a displayed

character row.

The lowering of the descender letters in this way requires

the row selection means to provide a number of additional row

addresses, and the character generator arrangement further includes

enabling means responsive to said detector means for enabling said

data output means to produce character generating data for a first

$\underline{n}$ successive row addresses for normal read-out operation and for a

second different, $\underline{n}$ successive row addresses for descender letter

read-out operation. Mullard Technical Note 7 (TP1404), October,

1974, describes a character generator arrangement in which the

character store is a ROM (Read Only Memory) for which, essentially,

the ASCII code is used for the read out of characters stored on a

7 x 5 dot matrix basis, and in which arrangement an adder circuit

is used, as aforesaid, to effect $\underline{inter}$ $\underline{alia}$ the correct alignment

of descender letters in a row of characters.

However, this additional circuitry which is required for the

correct alignment of the descender letters has the disadvantage

that because the adder circuit has to operate at the read out rate

for the character generating data, which will usually be a fast

rate, of for example 1MHz, this adder circuit will be complex in

implementation.

It is an object of the present invention to avoid this

disadvantage.

According to one aspect of the invention there is provided a

character store in which characters are stored in a manner

representing a character format composed of a co-ordinate matrix

of discrete character elements, and which is responsive to

character input data representing alpha-numeric characters to

produce character generating data which can be used for the display

of the alpha-numeric characters, characterized in that the co-

ordinate matrix for each descender letter has the character elements

for the descender letter so arranged that those elements forming

the "tail" of the descender letter are stored in character element

rows which in a given character element row addressing sequence for

the store in respect of characters other than descender letters,
precede the character element rows in which the remaining elements
for the descender letter are stored.

According to another aspect of the invention, a character
generator arrangement of the kind referred to, including detector
means for detecting when received character input data pertains to
a descender letter, together with enabling means responsive to the
detector means for enabling said data output means to produce
character generating data for a particular n successive row
addresses as produced by the row selection means and pertaining to a
normal character or to a descender letter, as the case may be, n being
the number of character element rows of the character format; is
characterised in that the character store of the arrangement is as
set forth in the preceding paragraph, and the row selection means
is controlled by the logic control means so as in a read-out
operation to repeat at least part of its addressing sequence such
that at least these row addresses pertaining to character element
rows which contain the elements forming the "tails" of descender
letters occur twice.

With such a character generator arrangement the correct
alignment of descender letters in a row of displayed characters is
achieved in the read-out operation without the use of an adder
circuit as is required in the known arrangement mentioned above.

In order that the invention may be more fully understood
reference will now be made by way of example to the accompanying
drawings, of which:

Figures 1 to 6 shows some character shapes using a 7 x 5
character element format;

Figure 7 shows, diagrammatically, a known character generator
arrangement;

Figure 8 shows, diagrammatically, a character generator
arrangement according to the invention; and

Figure 9 shows, diagrammatically, a display system embodying
the character generator arrangement of Figure 8.

Referring to the drawings, Figure 1 shows by way of
illustration the character shapes for the five letters B, b, c, D
and d, using a 7 x 5 character element format comprised by a

character matrix of 7 rows R1 to R7 and 5 columns C1 to C5 of
discrete character elements. Figure 2 shows the character shapes
for the five lower case descender letters g, j, p, q and y, using
the same character format. As can be seen from Figure 3, as
exemplified by the two descender letters y and p in the word "typed",
the descender letters are, in effect, in a "raised" position in
their respective character matrix as compared with the position of
non-descender letters. However, in displaying the word "typed",
the descender letters y and p would have to be "lowered" relative
to the other letters in the word so that their "tails" lie below
the line of the word; that is, when the word "typed" is displayed,
the "tails" of the descender letters y and p lie in additional
character element rows R8 and R9, as shown in Figure 4.

A known character generator arrangement for reading out such
characters for display and including means for determining the
correct alignment of descender letters relative to non-descender
letters in a row of displayed characters, is shown in Figure 7.
This known character generator arrangement comprises a character
store 1 in the form of a "read-only" memory device in which the
characters for display are stored. The character store 1 is
arranged to be addressed with character input data for a character
selected for display from an input addressing circuit 2. This
addressing is effected in parallel over 7 addressing leads b1 to b7
using binary coding. The input addressing circuit 2 serves as a
serial-to-parallel converter for producing in parallel as character
input data, 7-bit groups of input signals applied to it over an
input lead IL. Thus, 128 different characters can be stored in the
character store 1 and identified by a unique 7-bit binary code on
the addressing leads b1 to b7. Conveniently, as aforesaid, ASCII
coding can be used. The arrangement also comprises a row selection
circuit 3 for producing row addresses for selecting in turn the
character element rows of the character matrix. In order to cater
for the display of descender letters, in a manner to be described,
the row addresses are applied to the character store 1 over row
addressing leads ar1 to ar3, via an adder circuit 4. Binary coding
is also used for the row addresses.

In response to the application thereto of a particular character

code and a particular row address code, the character store 1

produces on a group of 5 output leads ol1 to ol5 a combination of

output signals (e.g. a combination of '1's and '0's) corresponding

to the combination of character elements in the selected character

5   element row of the selected character. Thus, if row R3 of the

lower case letter e (see Figure 3) is selected, the output signal

combination would be, say, 01110. The output signals on the leads

ol1 to ol5 are applied through a group of AND-gates G1 to G5 to

an output buffer stage 5. This output buffer stage 5 serves as a

10   parallel-to-serial converter for producing in series as character

generating data on an output lead OL the groups of 5 parallel

output signals from the character store 1.

The row selection circuit 3 is suitably a counter which is

driven by clock pulses ck. In a practical embodiment of the

15   arrangement, the clock pulse period may be 64 uS, with a new

character code being applied to the character store 1 every 1 uS.

In order to cater for descender letters, the row selection circuit

3 provides a number of row addresses additional to the number (7)

of character element rows of the character matrix. In the present

20   instance, it is assumed that the row selection circuit 3 provides

a recurrent cycle of 9 row addresses which are produced as respective

binary codes on four leads r1 to r4. These row address codes are

applied to the adder circuit 4 and also to a gate enabling circuit

6 which has a "gate enable" output lead GL connected in common to

25   one input of each of the AND-gates G1 to G5. The arrangement

further comprises a detector circuit 7 which detects when a character

code on the leads b1 to b7 pertains to a descender letter to produce

a control signal on an output lead CS. This control signal is

applied to both the adder circuit 4 and the gate enabling circuit 6.

30   When a character code pertaining to a non-descender letter

is applied from the input addressing circuit 2 to the character

store 1, there is no control signal on the output lead CS, so

that the adder circuit 4 remains unresponsive in that it adds a

naught to each row address code applied to it. Thus, the first 7

35   row address codes of a cycle on the leads r1 to r3 (r4 is not

needed) are passed unmodified onto the leads ar1 to ar3 to select

in turn the 7 character element rows of the character matrix.
Because of the absence of the control signal on the output lead
CS, the gate enabling circuit (which itself is suitably composed
of gate logic) produces the "gate enable" signal on the output

5   lead GL for the occurrence of each of the first 7 row address
codes. As a result, the gates G1 to G5 pass to the output buffer
stage 5 the output signal combinations from the character store 1
for the first 7 row address codes of a cycle from the row selection
circuit 3.

10   When a character code pertaining to a descender letter is
applied from the input addressing circuit 2 to the character
store 1, this character code is detected by the detector circuit 7
which thus produces the control signal on the output lead CS. The
effect of this control signal as applied to the gate enabling

15   circuit 6 is to cause the latter to produce the "gate enable" signal
on the output lead GL for the occurrence of each of the last 7 row
address codes in the cycle produced by the row selection circuit 3.
The effect of the control signal as applied to the adder circuit 4
is to cause the latter to add minus two (-2) to each row address

20   code applied to it. Thus, the last 7 row address codes of a cycle
on the leads $\underline{r}1$ to $\underline{r}4$ are changed by the adder circuit 4 to become
the first 7 row address codes on the leads $\underline{ar}1$ to $\underline{ar}3$. The effect
of this can be seen from Figure 4. If the character element rows
R1 to R9 correspond to display lines T1 to T9 for a row of displayed

25   characters, then for a non-descender letter such as $\underline{T}$, the
character element rows R1 to R7 are addressed during the occurrence
of their own row address codes to display the letter $\underline{T}$ in the
display lines T1 to T7. However, for a descender letter such as $\underline{y}$,
the character element rows R1 to R7 are addressed during the

30   occurrence of the address codes R3 to R9, respectively, to display
the letter $\underline{y}$ in the display lines T3 to T9; that is, the display
of the descender letter is delayed by two row address periods to
bring it into correct alignment in the character row.

        The known arrangement just described has the disadvantage,
35   mentioned previously, that the adder circuit 4 has to operate at
the character input data rate (e.g. at 1MHz as aforesaid), which

requires the adder circuit to be complex in implementation. The
character generator arrangement according to the invention shown
in Figure 8 avoids this disadvantage by dispensing with with adder
circuit.

5   Referring to Figure 8, in the arrangement there shown, elements
which correspond to elements in the arrangement of Figure 8 have
been given the same reference letters and numerals. Since in
Figure 8 the adder circuit has been dispensed with, the output leads
$r1$ to $r3$ from the row selection circuit 3 are connected directly
10   to the character store 1. In accordance with one aspect of the
invention, in the character store 1 the character matrix for each
descender letter has the character elements for the descender letter
so arranged, as shown in Figure 5, that those elements forming the
"tail" of the descender letter are stored in character element rows
15   R1 and R2 above (or before in the addressing sequence) the
character element rows R3 to R7 in which the remaining elements for
the descender letter are stored. In accordance with the second
aspect of the invention, in the arrangement of Figure 8 the row
selection circuit 3 provides on the leads $r1$ to $r3$ at least some of
20   the 7 row address codes twice in a read-out operation, and it also
provides on the lead $r4$ an indication to the gate enabling circuit
6 as to whether in a read-out operation it is the first or the
second occurrence of a row address code. Conveniently, this can be
achieved using a conventional 4-bit binary code for the row
25   address codes. A '0' or '1' bit on the lead $r4$ signifies to the
gate enabling circuit 6 whether the remaining eight 3-bit codes
on the leads $r1$ to $r3$ are occurring for the first or for the second
time. Since there are only seven character element rows in the
character format, one of the eight 3-bit codes on the leads $r1$ to
30   $r3$ needs to be "slipped" (e.g. by switchable gating in the row
selection circuit 3 in order to provide a recurrent cycle of only
7 row address codes. Alternatively, the character format in the
character store can include a spare row as illustrated in Figure 6
for the letters $\underline{A}$ and $\underline{q}$ in order to achieve a natural 3-bit binary
35   count of eight. The position of the spare row in the character
format depends on the character, being at the top or bottom for a

non-descender letter and at an intermediate position for descender
letters. More than one spare row may be provided, the only
requirement being that for both descender letters and non-descender
letters there is a continuous sequence of 7 character element rows
5   which can be addressed by seven successive row address codes of a
cyclic count in which at least some of the row address codes occur
twice.

Consider now the operation of the arrangement of Figure 8, for
a non-descender letter, the gate enabling circuit 6 responds to
10   the '0' on lead $r4$ to enable the gates G1 to G5 for the first 7
row address codes produced on the leads $r1$ to $r3$ in a first cycle.
For a descender letter, the circuit 6 responds to the '1' on lead
$r4$, due to the presence of the control signal on the lead CS, to
enable the gates G1 to G5 for the last 5 row address codes produced
15   on the leads $r1$ to $r3$ in the first cycle and the first 2 row
address codes produced in the second cycle. This provides for the
"lowering" of the descender letters into their correct alignment in
a row of characters, without the need of an adder circuit.

Where the row selection circuit provides a natural binary
20   count of eight 3-bit row address codes, the character element
rows, including the space row, of the character format as shown
in Figure 6 may be identified with row address codes in accordance
with the following Table.

25   TABLE

Row	Address Code							
	1st cycle				2nd cycle			
	$r4$	$r3$	$r2$	$r1$	$r4$	$r3$	$r2$	$r1$
R0	0	0	0	0	1	0	0	0
R1	0	0	0	1	1	0	0	1
R2	0	0	1	0	1	0	1	0
R3	0	0	1	1				
R4	0	1	0	0				
R5	0	1	0	1				
R6	0	1	1	0				
R7	0	1	1	1				

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Thus, for a non-descender letter the spare row is RO and has
the unused code 0 000, whereas for a descender letter the spare
row is R2 and has the unused code 0 010.

Referring now to Figure 9 of the drawings, which shows
diagrammatically a display system in the form of a television
receiver arrangement which embodies the invention and which is for
displaying selectively either a television picture which is produced
from picture information in a normal broadcast or cable television
video signal, or alpha-numeric text or other message information
which is produced from coded data pulses which are transmitted in
the video signal in vertical or field-blanking intervals thereof.

An incoming television video signal VS appears at an input
lead 1 of the television receiver arrangement via its front end 2
which comprises the usual amplifying, tuning, i.f. and detector
circuits. The front end 2 is assumed to be adapted to receive the
video signal VS from a television transmitter 3 via a conventional
over-air broadcast or cable transmission link 4.

For normal picture display in the television receiver
arrangement, the received video signal is applied to a selector
circuit 5 which included a selector switch 6. When the switch 6
is closed, the video signal VS is applied to a colour decoder 7
which produces the R, G and B component signals for the picture
display, these component signals being applied via a video interface
circuit 8 to the red, green and blue guns of a colour television
picture tube 9. Scanning circuits 10 for the tube 9 receive the
usual line and field synchronising pulses LS and FS from a synch.
separator circuit 11 which extracts these synchronising pulses from
the incoming video signal VS.

Coded data pulses representing message information in the
video signal VS do not affect the picture display because they occur
in one or more lines in the field-blanking interval when there is
no picture display. Of the lines occurring in the field-blanking
interval, most could be used to transmit coded data pulses
representing message information. However, in the BBC/IBA Teletext
System at present, only lines 17/18 of even fields and lines 330/331
of odd fields of the 625 line broadcast television system are used

in the United Kingdom. (See "Broadcast Teletext Specification",
September 1976, published jointly by the British Broadcasting
Corporation, Independent Broadcasting Authority and British Radio
Equipment Manufacturers' Association).

5   The video signal VS on the input lead 1 is also applied to a
data acquisition circuit 12 which includes a data clock pulse
generator (not shown) for deriving a data clock pulse train from
the coded data pulses representing the message information.

          It is assumed that the message information represented by the
10   coded data pulses contained in the video signal VS is divided into
different pages of information, and that each page is for display
as a whole on the screen of the picture tube 9, with the coded data
pulses representing each page of information being repeated
periodically in a recurrent cycle with or without updating of the
15   information. It is further assumed that each page of message
information is identified by means of a unique page address code
which is included in the coded data pulses and defines the page
number. The television receiver arrangement includes a code selector
circuit 13 which controls the particular coded data pulses that are
20   acquired by the data acquisition circuit 12 at any time. (This
control is indicated by broad-arrow connection $\underline{n}$ representing the
presence of a group of $\underline{n}$ parallel channels which form an $\underline{n}$-bit
channel link for carrying $\underline{n}$ bits of information required for data
selection - other groups of parallel channels forming multi-bit
25   channel links in the television receiver arrangement are represented
similarly as $\underline{m}$, $\underline{o}$, and $\underline{q}$ numbers of channels and bits).

          The acquired coded data pulses are clocked serially into the
data acquisition circuit 12 by the data clock pulse train produced
in the latter. From the data acquisition circuit 12, the acquired
30   coded data pulses are fed in parallel groups of $\underline{m}$ bits to a parity
bit error detector circuit 14 over an $\underline{m}$-bit channel link, an $\underline{m}$ bit
byte being required for each character (or other item of information)
contained in the message information. It is assumed that $\underline{m}$ = 8,
so that a character byte comprises a character code consisting of
35   7 bits plus a single parity bit, and that the circuit 14 functions
to check for odd parity in each character byte and to pass the

character code for storage only if the odd parity is detected.

The 7-bit character codes which satisfy the odd parity check
are fed from the detector circuit 14 in parallel over an o-bit
channel link (o = 7) to a data store 15. The data store 15 can

5   store a complete page of message information. In a typical Teletext
transmission, each page of message information would contain up to
24 rows of characters, with each row containing up to 40 characters.
Thus, in order to identify the different characters of a page, it
is furthermore assumed that the coded data pulses also include an

10   address code for each character, this address code employing q bits
and being fed to the data store 15 over a q-bit channel link to
control the storage therein of the character codes.

In view of the restricted transmission time which is available
for transmitting the coded data pulses representing message

15   information, for instance, sufficient time to transmit the coded
data pulses for only one character row during a television line in
the field-blanking interval, character data for a page of message
information has to be stored row-by-row in the data store 15 over
a relatively large number of television fields. This storing of

20   character data row-by-row in the data store 15 is under the
control of the address codes received from the data acquisition
circuit 12 over the q-bit channel link.

The television receiver arrangement includes a character
generator arrangement 16 embodying the present invention. This

25   arrangement 16 is responsive to the character data stored in the
data store 15 to produce character generating data which can be
used to derive what is effectively a new picture signal for
displaying the characters represented by the stored character data.

In order to effect character display on the screen of the

30   picture tube 9 using standard line and frame scans, the logic of
the television receiver arrangement in respect of character display
is so organised that for each row of characters to be displayed, all
the characters of the row are built up television line-by-television
line as a whole, and the rows of characters are built up in succession.

35   It takes a number of television lines to build up one row of
characters. In the first television line of each field, character

data from the data store 15 to the character generator arrangement
16 would cause the latter to produce character generating data
in respect of the first row of discrete elements for the first
character of the row, then in respect of the first row of discrete
5   elements for the second character, and so on for the successive
characters of the row. In the second television line, character
generating data in respect of the second row of discrete elements
for each character of the row would be produced in turn, and so on
for the remaining television lines concerned.

10   The logic of the television receiver arrangement is organised
by means of a clock pulse and timing pulse chain circuit 17 which
provides appropriate clock and timing pulses to the data store 15,
to the character generator arrangement 16, to the data acquisition
circuit 12 and to the parity bit error detector circuit 14. The
15   circuit 17 is synchronised in operation with the scanning circuits
10 of the picture tube 9 by the line and field synchronising pulses
LS and FS extracted from the incoming video signal VS by the sync.
separator circuit 11.

The output from the character generator arrangement 16 is
20   applied to a colour coder 18 which produces R^1, G^1 and B^1 component
signals for character display, these component signals being also
applied to the video interface circuits 8. The colour coder 18 can
be controlled (in a manner not shown) by selected items of the
character data in the data store 15 to provide a controlled colour
25   character display. Of course, black-and-white picture and character
display is also possible, in which event the colour decoder 7 and
colour coder 19 would be omitted.

The invention is, of course, also applicable to other display
systems, such as television monitors for computer read-out
30   terminals.

Also, the character generator arrangement 16 can be arranged
to receive the bits of a character code directly in parallel from
the data store 15, in which case the input addressing circuit (2)
of the arrangement would not need to perform any serial-to-parallel
35   conversion and could be implemented by a simple buffer stage.

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CLAIMS:

1.   A character store in which characters are stored in a manner
representing a character format composed of a co-ordinate matrix of
discrete character elements, and which is responsive to character
input data representing alpha-numeric characters to produce
5   character generating data which can be used for the display of the
alpha-numeric characters, characterised in that the co-ordinate
matrix for each descender letter has the character elements for
the descender letter so arranged that those elements forming the
"tail" of the descender letter are stored in character element rows
10   which in a given character element row addressing sequence for the
store in respect of characters other than descender letters,
precede the character element rows in which the remaining elements
for the descender letter are stored.
2.   A character store as claimed in Claim 1, characterised in
15   that it is in the form of a "read-only" memory device.
3.   A character store as claimed in Claim 1 or Claim 2, characterised
in that the character format is a 7 x 5 dot matrix.
4.   A character store as claimed in Claim 1, Claim 2 or Claim 3,
embodied in a character generator arrangement which comprises, in
20   addition to the character store, input addressing means for
addressing the character store with character input data for a
character selected for display, row selection means for producing

row addresses for selecting for a read-out operation from the

character store those character elements in a particular character

element row of the character matrix, data output means for producing

in said read-out operation the character generating data for the

5   character elements in the selected character element row of the

selected character, and logic control means for so controlling the

input addressing means and the row selection means as to cause, for

a plurality of characters to be displayed as a row of characters,

the selection in turn of the character elements in a first character

10 element row of each of said plurality of characters, then the

selection in turn of the character elements in a second character

element row thereof, and so.on for their remaining character element

rows, so that said plurality of characters are built-up element

row-by-element row, as a whole, for display, the arrangement further

15 including detector means for detecting when received character

input data pertains to a descender letter, together with enabling

means responsive to the detector means for enabling said data output

means to produce character generating data for a particular n

successive row addresses as produced by the row selection means and

20 pertaining to a normal character or to a descender letter, as the

case may be, n being the number of character element rows of the

character format, the row selection means being further controlled

by the logic control means so as in a read-out operation to repeat

at least part of its addressing sequence such that at least those

25 row addresses pertaining to character element rows which contain

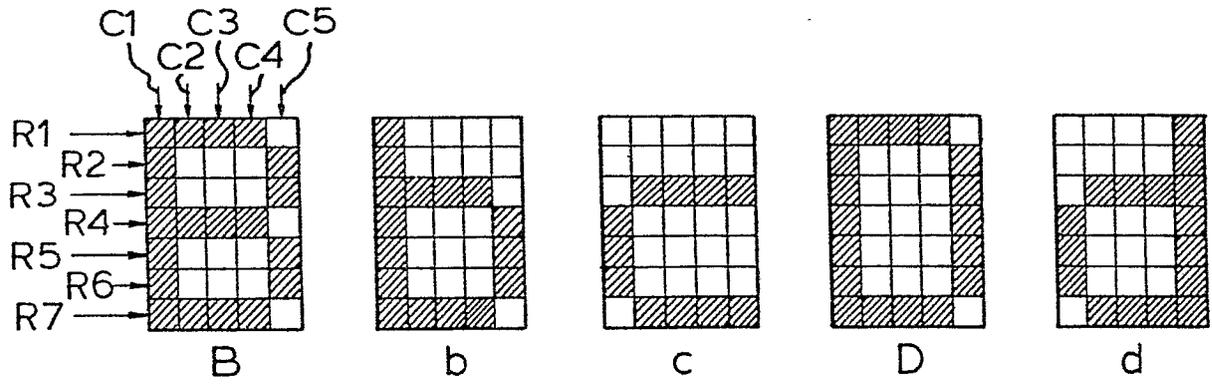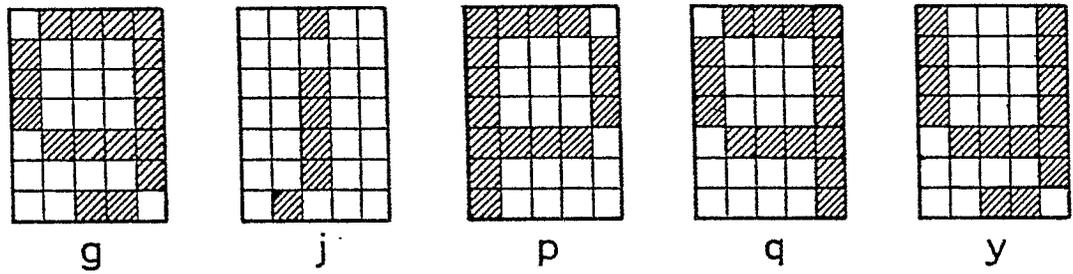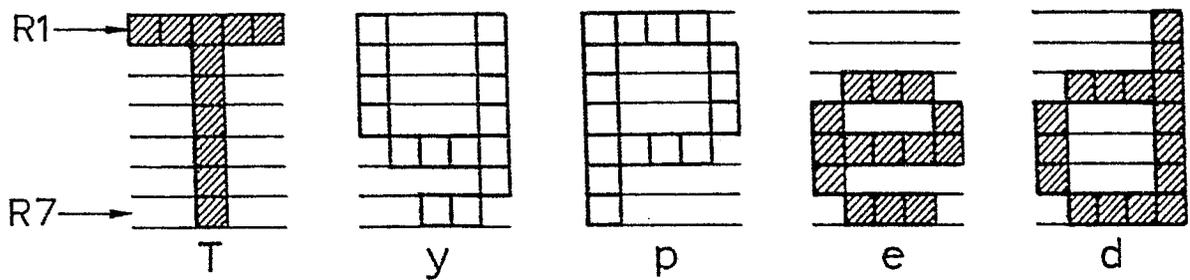the elements forming the "tails" of descender letters occur twice.

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Fig.1

Fig.2

Fig.3

T1,R1→

R7→
R8→
T9,R9→

Fig.4

R1→

R7→

g   j   p   q   y

Fig.5

R0→
R1→
R2→

R7→

A   q

Fig.6

Fig.7

Fig. 8

Fig.9

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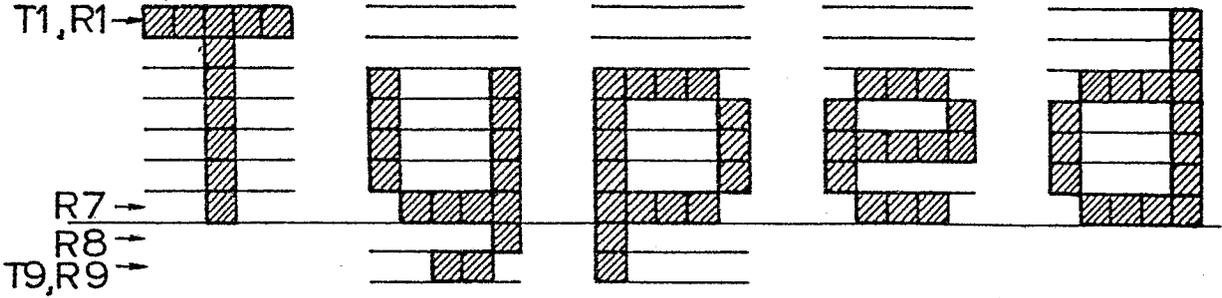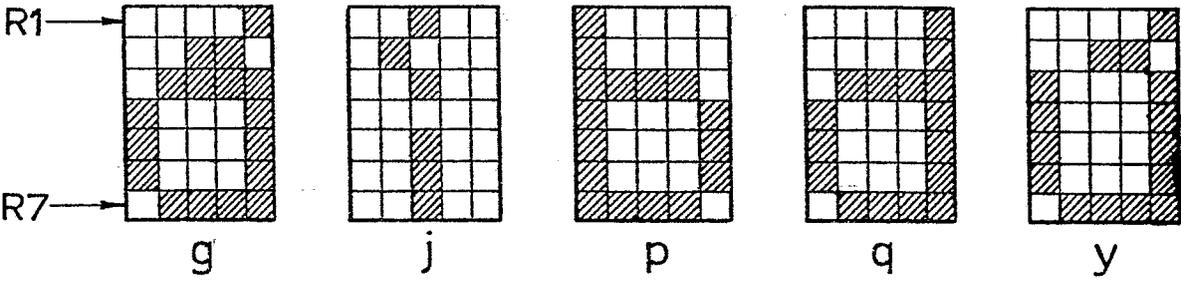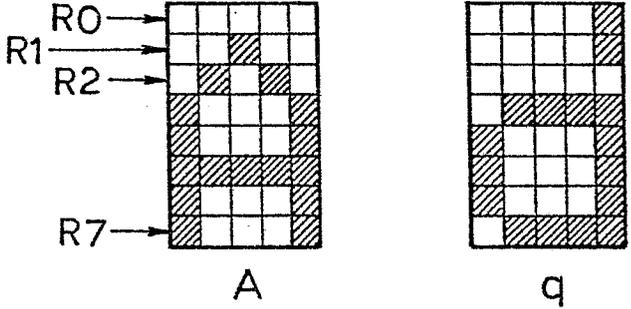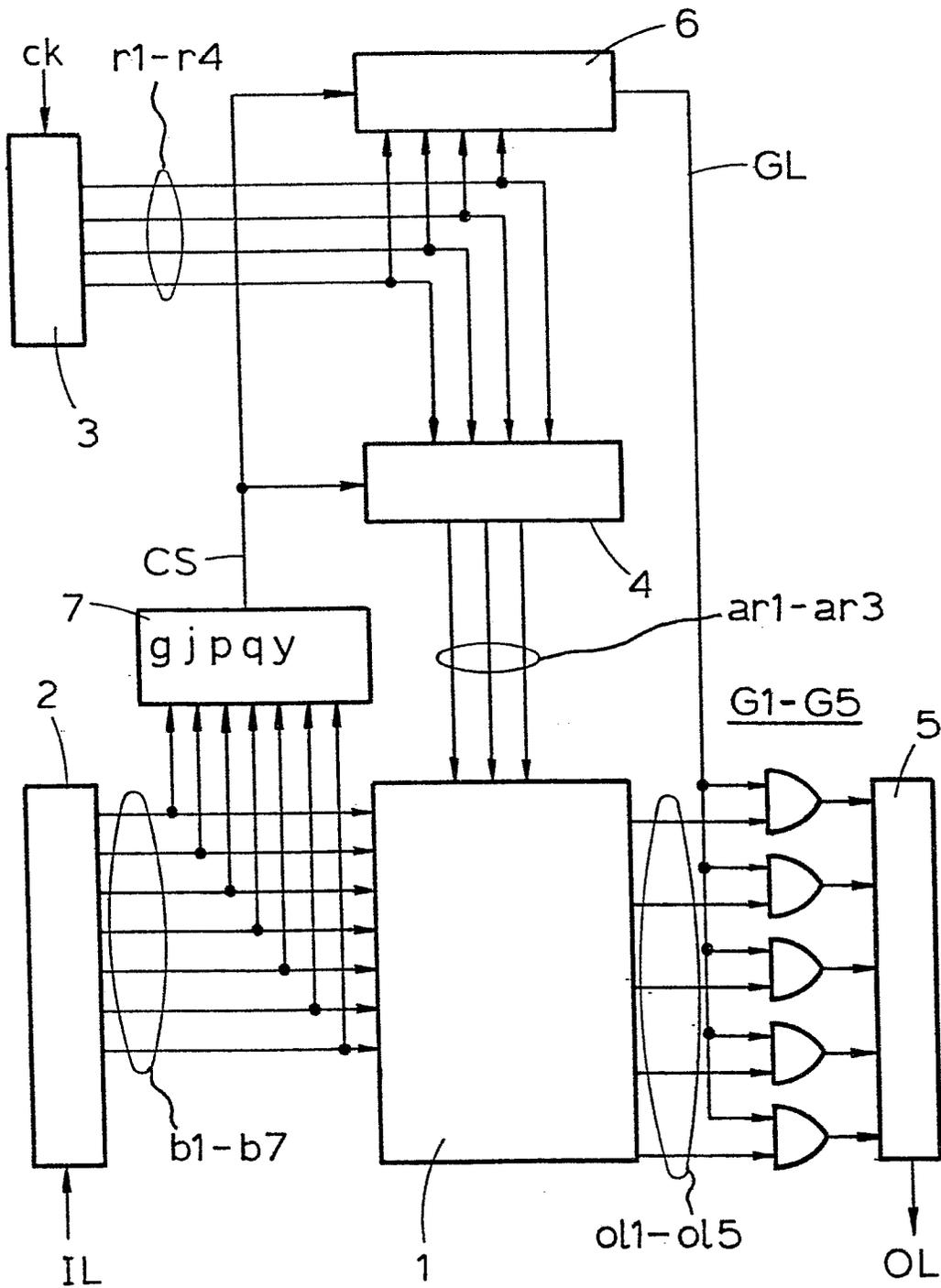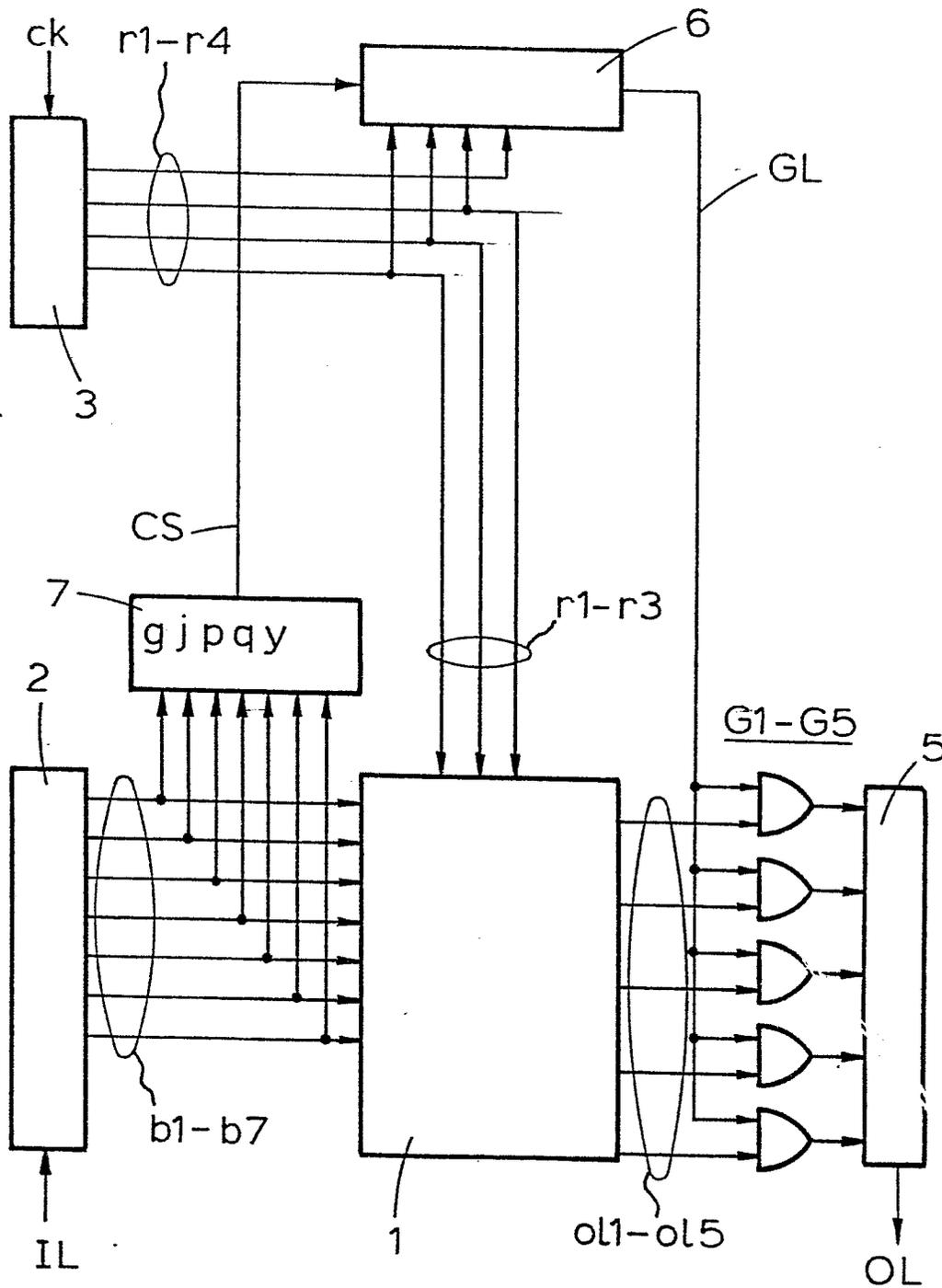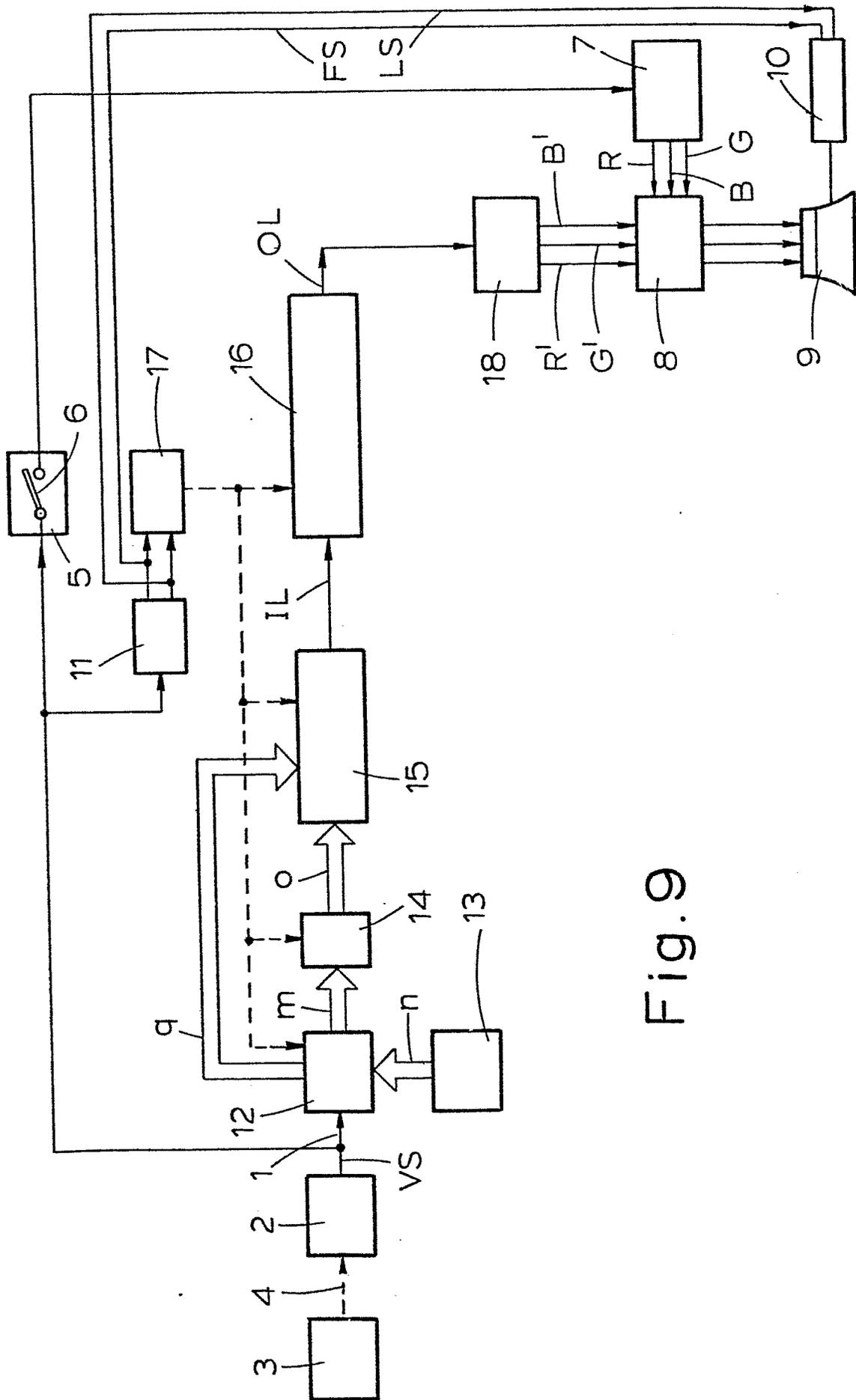
DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim
P	US - A - 4 146 877 (E.F. ZIMMER) 27th March 1979 * Figures 1-2; from column 1, line 59 to column 2, line 23; column 3, lines 3-19; from column 4, line 28 to column 5, line 20; from column 5, line 41 to column 6, line 19 * --	1-4
A	WIRELESS WORLD, vol. 82, no.1484, April 1976, London, GB J.F. DANIELS: "Wireless world teletext decoder", pages 64-68. * Figure 1 * ----	1-3

CLASSIFICATION OF THE APPLICATION (Int. Cl. 3)

G 09 G   1/14

TECHNICAL FIELDS SEARCHED (Int.Cl. 3)

G 09 G   1/14
          1/16
          1/18
B 41 J   3/02

CATEGORY OF CITED DOCUMENTS

X: particularly relevant
A: technological background
O: non-written disclosure
P: intermediate document
T: theory or principle underlying the invention
E: conflicting application
D: document cited in the application
L: citation for other reasons

&: member of the same patent family, corresponding document

X The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	01-06-1980	VAN ROOST

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