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- (54) A system of functional units for performing logic functions.
- 57 According to the invention, the LSI testing methods allow the states of combinational logic networks to be captured in either a group of master latches (390) or slave latches (400) of shift registers used for performing scan-in/scan-out operations on test data (test patterns, result patterns), but not both.

If on a particular test the states are captured in the master latches, then each master latch state is subsequently shifted to the corresponding slave latch by the application of a shift clock, as known from the art.

If instead the states are captured in the slave latches the slave latches can be immediately shifted out for inspection.

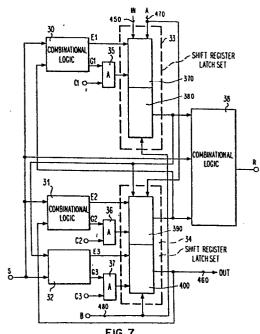


FIG. 7

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EUROPEAN SEARCH REPORT

Application number EP 80 10 3967

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int. Cl.)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	A FEMALON (III. O.)
	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 22, no. 2, July 1979 New York, US BERGLUND et al. "Effective use of level sensitive scan design", pages 730-734.	1,4	G 06 F 11/26
	* Page 730, lines 1-6; figures 1,4; page 734, lines 5-30 *		
AD	<u>US - A - 3 783 254</u> (IBM) * Column 10, lines 48-67; column 11, lines 1-20; column 13, lines 12-67; column 14, lines 11-22; figures 7,9,12, 13 *	1,3	TECHNICAL FIELDS SEARCHED (Int. CI.3)
			CATEGORY OF CITED DOCUMENTS X: particularly relevant
			A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention
		,	E: conflicting application D: document cited in the application L: citation for other reasons
X	The present search report has been drawn up for all claims		&: member of the same patent family, corresponding document
Place of s	Pate of completion of the search 21-05-1981	Examiner	DHEERE