(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 039 178**
B1

(12) # EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification: **11.09.85**

(51) Int. Cl.⁴: **G 05 F 3/20**

(21) Application number: **81301679.7**

(22) Date of filing: **15.04.81**

(54) **Integrated circuit for generating a reference voltage.**

(30) Priority: **18.04.80 JP 51399/80**

(43) Date of publication of application:
04.11.81 Bulletin 81/44

(45) Publication of the grant of the patent:
11.09.85 Bulletin 85/37

(84) Designated Contracting States:
DE FR GB NL

(56) References cited:
FR-A-2 281 603
US-A-3 794 861
US-A-3 886 435

IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-9, December 1974, A.P. BROKAW: "A *simple three-terminal IC bandgap reference*", pages 388-393

(73) Proprietor: **FUJITSU LIMITED**
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211 (JP)

(72) Inventor: **Tsuchiya, Chikara**
26-5, Honmachi 2-chome
Shibuya-ku Tokyo 151 (JP)

(74) Representative: **Abbott, Leonard Charles et al**
GILL JENNINGS & EVERY 53-64 Chancery Lane
London WC2A 1HN (GB)

Courier Press, Leamington Spa, England.

EP 0 039 178 B1

Description

The present invention relates to a circuit for generating a reference voltage, and more specifically to an integrated circuit for generating a reference voltage which is in agreement with a band gap of a semiconductor material that forms the transistor and which assumes a predetermined value irrespective of the temperature.

The reference voltage must, usually, assume a constant value independently of the temperature. This requirement can be satisfied by using a band-gap reference circuit. As represented, for example, by an integrated circuit LM 117 manufactured by National Semiconductor Co., the band-gap reference circuit consists of a first transistor and a second transistor of which the bases are connected and which are served with an equal current from a current mirror circuit, the area of the emitter of the second transistor being N times greater than that of the first transistor. Further, a first resistor is connected to the emitter of the second transistor, and a connection point between the other end of the first resistor and the emitter of the first transistor is grounded via a second resistor. The collector voltage of the first transistor, on the other hand, is fed back to the power supply of the current mirror circuit via a feedback amplifier, and the output voltage is taken out from the base potential of the first and second transistors.

In such a conventional circuit for generating the reference voltage, the potential of the power supply for supplying a current to the current mirror circuit must be higher than the collector potential of the first transistor. When the reference voltage is 1.2 volts, the potential of the power supply of the current mirror circuit must be greater than 2.1 volts at room temperature. The potential of the power supply of the current mirror circuit is supplied from the power supply of the feedback amplifier. Therefore, the feedback amplifier requires a higher power-supply voltage. Requirement of such a high power-supply voltage is not desirable for integrated circuits, and it is an object of the present invention to provide a reference voltage generator circuit which operates on a small power-supply voltage.

The present invention consists in a circuit for generating a reference voltage, comprising: a first transistor and a second transistor of which the bases are connected together, the area of the emitter region of the first transistor being smaller than the area of the emitter region of the second transistor, the emitter of the first transistor being connected to ground, and the emitter of the second transistor being connected to ground via a first resistor; a current supply means which supplies equal currents to the collectors of the first and second transistors; and characterised by a second resistor which is connected between an output terminal and a connection point of the interconnected bases of the first and second transistors; and a current generator circuit which is connected between the connection point of the commonly connected bases and ground to produce a current which is proportional to the emitter current of the first transistor or the second transistor, such that a constant voltage is generated at the output terminal.

In order that the invention may be better understood examples of circuits embodying the present invention will now be described with reference to the accompanying drawings, in which:—

Fig. 1 is a block diagram of a conventional bandgap reference circuit;

Fig. 2 is a diagram which illustrates temperature characteristics of the band-gap reference circuit;

Fig. 3 is a block diagram illustrating a basic embodiment of a circuit for generating a reference voltage according to the present invention;

Fig. 4 is a circuit diagram of an embodiment of the block diagram of Fig. 3;

Fig. 5 is a block diagram illustrating another embodiment of the circuit for generating a reference voltage according to the present invention;

Fig. 6 is a circuit diagram of an embodiment of the block diagram of Fig. 5;

Fig. 7 is a circuit diagram of another embodiment of the circuit for generating a reference voltage of the present invention;

Fig. 8 is a circuit diagram of a further embodiment according to the present invention; and

Figs. 9A and 9B are circuit diagrams illustrating important portions of still further embodiments according to the present invention.

Fig. 1 shows a conventional band-gap reference circuit in which the feature resides in a pair of npn transistors Q_1 and Q_2 that produce a current proportional to the absolute temperature, and a resistor R_1. The transistors Q_1, Q_2 of which the bases are interconnected are served with equal currents from a current mirror circuit 1 consisting of pnp transistors Q_3 to Q_5, and wherein the area of the emitter of the transistor Q_2 is N times greater than that of the transistor Q_1. One end of a first resistor R_1 is connected to the emitter of the transistor Q_2, and another end of the resistor R_1 and the emitter of the transistor Q_1 are grounded via a second resistor R_2. Therefore, the base potential of the transistors Q_1, Q_2, i.e., a reference voltage V_B at the output terminal B is given by,

$$V_B = V_{BE1} + I_2 R_2 \qquad (1)$$

where V_{BE1} denotes a voltage across the base and emitter of the transistor Q_1, and I_2 denotes a current which flows through the resistor R_2.

If emitter currents of the transistors Q_1 and Q_2 are each denoted by I_E, there is the relation $I_2 = 2I_E$.

Since the transistors Q_1, Q_2 have different emitter areas, the voltage V_{BE2} across the base and emitter of the transistor Q_2 is different from the voltage V_{BE1} across the base and emitter of the transistor Q_1. Namely,

$$V_{BE1}=V_T I_n \frac{I_E}{I_S} \quad (2)$$

$$V_{BE2}=V_T I_n \frac{I_E}{N \cdot I_S} \quad (3)$$

where, $V_T=\frac{kT}{q}$

where k denotes Boltzmann's constant, T denotes the absolute temperature, q denotes the electric charge of an electron, N denotes a ratio of emitter areas, and I_S denotes a saturated current.

In the connection mode of Fig. 1,

$$V_{BE1}=V_{BE2}+I_E \cdot R_1 \quad (4)$$

If relations (2) and (3) are inserted into the above relation, there is obtained the relation,

$$I_E \cdot R_1=V_{R1}=V_T I_n N \quad (5)$$

By using the above relation (5), the relation (1) can be rewritten as follows:

$$V_B=V_{BE1}+2I_E \cdot R_2$$

$$=V_{BE1}+2V_{R1}\frac{R_2}{R_1}$$

$$=V_{BE1}+2 \cdot \frac{R_2}{R_1} V_T I_n N \quad (6)$$

The temperature dependency, therefore, is as shown in Fig. 2. Namely, V_{BE1} which is the first term on the right side of the relation (6) decreases with the increase in the temperature T, and

$$2 \cdot \frac{R_2}{R_1} \cdot V_T I_n N$$

which is the second term increases with the rise in the temperature T. Therefore, of the changing ratios are equalized by adjusting R_2/R_1, the two values are cancelled by each other, and the reference voltage V_B remains constant (compensated for the temperature). This constant value is nearly equal to a band-gap voltage (1.2 volts in the case of a silicon semiconductor) of a semiconductor material which forms transistors Q_1, Q_2.

Here, if a voltage across the collector and emitter which does not saturate the transistor is denoted by V_S the potential V_A at a point A which supplies a current to the current mirror circuit CM must assume a value which is greater than a potential $V_B-V_{BE1}+V_S$ at the collector (point C) of the transistor Q_1 by a quantity of two stages of V_{BE} of the transistors Q_3, Q_5, i.e.,

$$V_A \geqq V_B+V_{BE}+V_S \quad (7)$$

Practical values at room temperature are $V_B=1.2$ V, $V_{BE}=0.7$ V, and $V_S=0.2$ V. Therefore, the relation $V_A \geqq 2.1$ V must hold true. The voltage V_A is supplied from the power-supply voltage V_{CC} of the feedback amplifier 2. Therefore, requirement of a high voltage V_A means that the power-supply voltage V_{CC} must be high. Symbols R_3 and R_4 denote resistors of the output stage, which feed base currents to the transistors Q_1 and Q_2.

Fig. 3 is a circuit diagram illustrating a first embodiment of the present invention, in which the same portions are denoted by the same symbols. What makes the circuit of Fig. 3 different from the circuit of Fig. 1 is that the second resistor R_2 is connected between the output terminal B and a point D where bases of the transistors Q_1, Q_2 are connected; this resistor is denoted by R_{12}. Further, a transistor (or a diode) Q_6 is connected between the point D where the bases are connected and ground, so that the electric current I_2 will flow through the second resistor R_{12} in proportion to the absolute temperature. The transistor Q_6 forms a current mirror circuit together with the transistor Q_1. It is therefore possible to pass an electric current which is proportional to the ratio of emitter areas of the two transistors. In other words, it is possible to adjust the current flowing through the resistor R_{12} to become equal to the current I_2 of Fig. 1. Consequently the above-mentioned relation (1) holds true even with the circuit of Fig. 3. Therefore, the temperature characteristics of V_{BE1} of the transistor Q_1 are compensated by the temperature characteristics of voltage drop I_2R_{12} across the resistor R_{12}, and the reference voltage V_B(=1.2 V) is maintained constant as shown in Fig. 2. Further, since the emitter of the transistor Q_1 can be grounded, the potential at the point C can be lowered to V_S, and the potential V_A at the point A can be lowered to,

$$V_A \geqq 2V_{BE}+V_S \quad (8)$$

If the aforementioned numerical figures are inserted $V_A \geqq 1.6$ V; i.e., the power-supply voltage V_{CC} can be lowered by 0.5 V as compared with the case of the relation (7). As is well known, the power supply of the integrated circuits has a small voltage, and is often established by storage cells. Therefore, the decrease of the power-supply voltage by 0.5 volt gives such a great effect that the number of storage cells can be reduced, for example, from three to two.

The resistor R_4 works to reduce the potential difference (1.6—1.2) V between V_A and V_B. The resistor R_4, however, may be replaced by a diode or a transistor. Fig. 4 illustrates an embodiment of a circuit based upon the fundamental setup of Fig. 3, in which symbols Q_8, Q_9 denote transistors which constitute an amplifier 2a, and C_1 denotes a capacitor for compensating the phase. Further, a

resistor R_S connected between the power supply V_{CC} and the point A has a high resistance and works to start the operation. The emitter area of the transistor Q_2 is set to be, for example, 5 times (×5) that of the transistor Q_1. In the embodiment of Fig. 4, a potential difference of about 0.7 V is maintained between V_A and V_B by a diode D_1.

Fig. 5 illustrates a modified embodiment of the fundamental setup of Fig. 3. What makes the circuit of Fig. 5 different from the circuit of Fig. 3 is that a series circuit comprising the transistor Q_2 and the resistor R_1 is connected in series with the collector of the transistor Q_3, the collector of the transistor Q_1 is connected in series with the base of the transistor Q_3, and the feedback amplifier 2b is fed back to the potential V_A from the collector of the transistor Q_2. In this case, the input phase and the output phase of the amplifier are reversed relative to each other. The principle of operation, functions and effects are quite the same as those in the case of Fig. 3. Fig. 6 illustrates an embodiment of the setup of Fig. 5, wherein a transistor Q_{10} works as a feedback amplifier, and its output phase and the input phase are reversed relative to each other.

Fig. 7 illustrates a modified embodiment of Fig. 4, in which a transistor Q_7 is used in place of the resistor R_4 that is employed in Fig. 3, and transistors Q_8 and Q_9 form an amplifier. This circuit features a large output current since the transistor Q_7 is connected in a manner of emitter follower. Fig. 8 illustrates a further modified embodiment of Fig. 4. Namely, the circuit of Fig. 8 does not have the transistor Q_3 and the diode D_1 that are used in the circuit of Fig. 4, and requires a further decreased power-supply voltage V_{CC}.

Figs. 9A and 9B illustrate important portions of the embodiment of Fig. 3 when the offset compensation is effected. The reference voltage generator circuit of this type is constructed in the form of a semiconductor integrated circuit, and an offset voltage (usually of the order of several millivolts) is generated in the voltages V_{BE} of the transistors Q_1, Q_6. Symbols R_{E1} and R_{E2} refer to small resistances which are inserted on the emitter side to cancel the offset voltage. These resistances generate voltages which are sufficient to cancel the offset voltages.

According to the present invention as mentioned in the foregoing, the power-supply voltage of a band-gap reference circuit can be lowered, and the number of storage cells can be reduced from, for example, three to two. Or, even when the same number of storage cells are used, for example, even when two storage cells are used, the circuit can be operated maintaining sufficient margin.

Claims

1. A circuit for generating a reference voltage, comprising: a first transistor (Q_1) and a second transistor (Q_2) of which the bases are connected together, the area of the emitter region of the first transistor being smaller than the area of the emitter region of the second transistor, the emitter of the first transistor being connected to ground, and the emitter of the second transistor being connected to ground via a first resistor (R_1); a current supply means (1) which supplies equal currents to the collectors of the first and second transistors; and characterised by a second resistor (R_{12}) which is connected between an output terminal (V_B) and a connection point of the interconnected bases of the first and second transistors; and a current generator circuit (Q_6) which is connected between the connection point of the commonly connected bases and ground to produce a current which is proportional to the emitter current of the first transistor (Q_1) or the second transistor (Q_2), such that a constant voltage is generated at the output terminal.

2. A circuit for generating a reference voltage according to claim 1, wherein the current supply means (1) comprises a current mirror circuit that is connected between the collectors of the first and second transistors (Q_1, Q_2) and a first power supply (V_A), and a feedback amplifier (2a) which is driven by a second power supply (V_{cc}) having a voltage higher than that of said first power supply and which is connected from the collector of the first transistor (Q_1) or the second transistor (Q_2) to the first power supply (V_A).

3. A circuit for generating a reference voltage according to claim 2, wherein the feedback amplifier (2a) is a positive-phase-sequence amplifier which is connected between the collector of the first transistor and the first power supply.

4. A circuit for generating a reference voltage according to claim 2, wherein the positive-phase-sequence amplifier (2a) comprises a third transistor (Q_9) of which the base is connected to the collector of the first transistor and of which the emitter is connected to ground, a fourth transistor (Q_8) of which the base is connected to the collector of the third transistor, of which the emitter is connected to the second power supply and of which the collector is connected to the first power supply, and a third resistor (R_S) connected between the first power supply and the second power supply.

5. A circuit for generating a reference voltage according to claim 4, wherein the circuit further has a sixth transistor (Q_7) of which the base is connected to the first power supply, of which the collector is connected to the second power supply, and of which the emitter is connected to the output terminal.

6. A circuit for generating a reference voltage according to claim 2, wherein the feed-back amplifier (2b) is a negative-phase-sequence amplifier which is connected between the collector of the second transistor and the first power supply.

7. A circuit for generating a reference voltage according to claim 6, wherein the negative-phase-sequence amplifier comprises a fifth transistor (Q_{10}) of which the base is connected to the collector of the second transistor (Q_2), of

which the emitter is connected to ground, and of which the collector is connected to the first power supply, and a third resistor (R_S) which is connected between the first power supply and the second power supply.

8. A circuit for generating a reference voltage according to any one of claims 1 to 7, wherein a resistor for offset compensation is inserted between the emitter of the first transistor (Q_1) and ground.

9. A circuit for generating a reference voltage according to any one of claims 1 to 7, wherein a resistor (R_{E1}) for offset compensation is inserted between ground and the junction of the emitter of the first transistor and the first resistor.

10. A circuit for generating a reference voltage, comprising: a first transistor (Q_1) and a second transistor (Q_2) of which the bases are connected together, the area of the emitter region of the second transistor being greater than that of the first transistor, the emitter of the first transistor being grounded and a first resistor (R_1) being connected between the emitter of the second transistor and ground; and characterised by a second resistor (R_{12}) connected between the base of the first transistor and an output terminal (V_B); a third transistor (Q_5) and a fourth transistor (Q_4) of which the collectors are connected to the collectors of the first and second transistors, respectively, of which the emitters are connected to the output terminal (V_B), of which the bases are connected together, and the base and collector of the fourth transistor (Q_4) are connected to each other; a voltage generator circuit connected between ground and the interconnected bases of the first and second transistors; a fifth tansistor (Q_9) of which the base is connected to the collector of the first transistor and of which the emitter is grounded; a capacitor (C_1) connected between the base of the fifth transistor and ground; a sixth transistor (Q_8) of which the base is connected to the collector of said fifth transistor, of which the emitter is connected to a power supply, and of which the collector is connected to the output terminal; and a third resistor (R_s) which is connected between said power supply and said output terminal.

Patentansprüche

1. Schaltung zur Erzeugung einer Referenzspannung mit: einem ersten Transistor (Q_1) und einem zweiten Transistor (Q_2), deren Basen miteinander verbunden sind, wobei das Gebiet des Emitterbereichs des ersten Transistors kleiner als das Gebiet des Emitterbereichs des zweiten Transistors, der Emitter des ersten Transistors mit Erde verbunden und der Emitter des zweiten Transistors über einen ersten Widerstand (R_1) mit Erde verbunden ist; einer Stromversorgungseinrichtung (1), welche gleiche Ströme zu den Kollektoren des ersten und des zweiten Transistors liefert; und gekennzeichnet durch einen zweiten Widerstand (R_{12}), welcher zwischen einem Ausgangsanschluß (V_B) und einem Verbindungspunkt der miteinander verbundenen Basen des ersten und zweiten Transistors angeschlossen ist; und eine Stromgeneratorschaltung (Q_6), welche zwischen dem Verbindungspunkt der miteinander verbundenen Basen und Erde angeschlossen ist, um einen Strom zu erzeugen, der proportional zu dem Emitterstrom dem ersten Transistors (Q_1) oder des zweiten Transistors (Q_2) ist, so daß an dem Ausgangsanschluß eine konstante Spannung erzeugt wird.

2. Schaltung zur Erzeugung einer Referenzspannung nach Anspruch 1, bei welcher die Stromversorgungseinrichtung (1) eine Stromspiegelschaltung umfaßt, die zwischen den Kollektoren des ersten und des zweiten Transistors (Q_1, Q_2) und einer ersten Energieversorgung (V_A) angeschlossen ist, und einen Rückkopplungsverstärker (2a), welcher von einer zweiten Energieversorgung (V_{cc}) betrieben wird, deren Spannung höher als diejenige der genannten ersten Energieversorgung ist, und der zwischen den Kollektor des ersten Transistors (Q_1) oder des zweiten Transistors (Q_2) und der ersten Energieversorgung (V_A) angeschlossen ist.

3. Schaltung zur Erzeugung einer Referenzspannung nach Anspruch 2, bei welcher der Rückkopplungsverstärker (2a) ein mitläufiger Verstärker ist, der zwischen dem Kollektor des ersten Transistors und der ersten Energieversorgung angeschlossen ist.

4. Schaltung zur Erzeugung einer Referenzspannung nach Anspruch 2, bei welcher der mitläufige Verstärker (2a) einen dritten Transistor (Q_9) umfaßt, dessen Basis mit dem Kollektor des ersten Transistors und dessen Emitter mit Erde verbunden ist, einen vierten Transistor (Q_8), dessen Basis mit dem Kollektor des dritten Transistors verbunden ist, dessen Emitter mit der zweiten Energieversorgung und dessen Kollektor mit der ersten Energievorsorgung verbunden ist, und einen dritten Widerstand (R_S), der zwischen der ersten Energieversorgung und der zweiten Energieversorgung angeschlossen ist.

5. Schaltung zur Erzeugung einer Referenzspannung nach Anspruch 4, bei welcher die Schaltung ferner einen sechsten Transistor (Q_7) umfaßt, dessen Basis mit der ersten Energieversorgung, dessen Kollektor mit der zweiten Energieversorgung und dessen Emitter mit dem Ausgangsanschluß verbunden ist.

6. Schaltung zur Erzeugung einer Referenzspannung nach Anspruch 2, bei welcher der Rückkopplungsverstärker (2b) ein Gegenkopplungsverstärker ist, der zwischen dem Kollektor des zweiten Transistors und der ersten Energieversorgung angeschlossen ist.

7. Schaltung zur Erzeugung einer Referenzspannung nach Anspruch 6, bei welcher der Gegenkopplungsverstärker einen funften Transistor (Q_{10}) umfaßt, dessen Basis mit dem Kollektor des zweiten Transistors (Q_2), dessen Emitter mit Erde und dessen Kollektor mit der ersten Energieversorgung verbunden ist, und einen dritten Widerstand (R_S), der zwischen der ersten

Energieversorgung und der zweiten Energieversorgung angeschlossen ist.

8. Schaltung zur Erzeugung einer Referenzspannung nach irgendeinem der Ansprüche 1 bis 7, bei welcher ein Widerstand zur Abweichungskompensation zwischen dem Emitter des ersten Transistors (Q_1) und Erde eingefügt ist.

9. Schaltung zur Erzeugung einer Referenzspannung nach einem der Ansprüche 1 bis 7, bei welcher ein Widerstand (R_{E1}) zur Abweichungskompensation zwischen Erde und dem Verbindungspunkt des Emitters des ersten Transistors und des ersten Widerstands eingefügt ist.

10. Schaltung zur Erzeugung einer Referenzspannung mit: einem ersten Transistors (Q_1) und einem zweiten Transistor (Q_2), deren Basen miteinander verbunden sind, wobei das Gebiet des Emitterbereichs des zweiten Transistors größer als das des ersten Transistors ist und der Emitter des ersten Transistors geerdet und ein erster Widerstand (R_1) zwischen dem Emitter des zweiten Transistors und Erde geschaltet ist; und gekennzeichnet durch einen zweiten Widerstand (R_{12}), der zwischen der Basis des ersten Transistors und einem Ausgangsanschluß (V_B) angeschlossen ist; einen dritten Transistor (Q_5) und einen vierten Transistor (Q_4), deren Kollektoren mit den Kollektoren des ersten bzw. zweiten Transistors verbunden sind, deren Emitter mit dem Ausgangsanschluß (V_B) verbunden sind und deren Basen miteinander verbunden sind, wobei die Basis und der Kollektor des vierten Transistors (Q_4) miteinander verbunden sind; eine Spannungsgeneratorschaltung, die zwischen Erde und den miteinander verbundenen Basen des ersten und zweiten Transistors angeschlossen ist, einen fünften Transistor (Q_9), dessen Basis mit dem Kollektor des ersten Transistors verbunden und dessen Emitter geerdet ist; einen Kondensator (C_1), der zwischen der Basis des fünften Transistors und Erde angeschlossen ist; einen sechsten Transistor (Q_8), dessen Basis mit dem Kollektor des genannten fünften Transistors verbunden ist, dessen Emitter mit einer Energieversorgung verbunden ist und dessen Kollektor mit dem Ausgangsanschluß verbunden ist; und einen dritten Widerstand (R_S), der zwischen der genannten Energieversorgung und dem genannten Ausgangsanschluß angeschlossen ist.

Revendications

1. Circuit pour la génération d'une tension de référence, comprenant; un premier transistor (Q_1) et un second transistor (Q_2) dont les bases sont connectées ensemble, la surface de la région d'émetteur du premier transistor étant inférieure à la surface de la région d'émetteur du second transistor, l'émetteur du premier transistor étant connecté à la masse, et l'émetteur du second transistor étant connecté à la masse par l'intermédiaire d'une première résistance (R_1); un moyen d'alimentation en courant (1) qui fournit des courants égaux aux collecteurs des premier et second transistors; et caractérisé par une seconde résistance (R_{12}) qui est connectée entre une borne de sortie (V_B) et un point de connexion des bases interconnectées des premier et second transistors; et un circuit générateur de courant (Q_6) qui est connecté entre le point de connexion des bases connectées en commun et la masse pour produire un courant qui est proportionnel au courant d'émetteur du premier transistor (Q_1) ou du second transistor (Q_2), de sorte qu'une tension constante est engendrée à la borne de sortie.

2. Circuit pour la génération d'une tension de référence selon la revendication 1, caractérisé en ce que le moyen d'alimentation en courant (1) est constitué par un circuit à courant en rapport géométrique qui est connecté entre les collecteurs des premier et second transistors (Q_1, Q_2) et une première alimentation (V_A); et un amplificateur à réaction (2a) qui est commandé par une seconde alimentation (V_{CC}) ayant une tension supérieure à celle de la première alimentation et qui est connectée par le collecteur du premier transistor (Q_1) ou du second transistor (Q_2) à la première alimentation (V_A).

3. Circuit pour la génération d'une tension de référence selon la revendication 2, caractérisé en ce que l'amplificateur à réaction (2a) est un amplificateur fonctionnant sur la composante positive de la phase qui est connecté entre le collecteur du premier transistor et la première alimentation.

4. Circuit pour la génération d'une tension de référence selon la revendication 2, caractérisé en ce que l'amplificateur fonctionnant sur la composante positive de la phase (2a) comprend un troisième transistor (Q_9) dont la base est connectée au collecteur du premier transistor et dont l'émetteur est connecté à la masse, un quatrième transistor (Q_8) dont la base est connectée au collecteur du troisième transistor, dont l'émetteur est connecté à la seconde alimentation et dont le collecteur est connecté à la première alimentation, et une troisième résistance (R_S) connectée entre la première alimentation et la seconde alimentation.

5. Circuit pour la génération d'une tension de référence selon la revendication 4, caractérisé en ce que le circuit comprend en outre un sixième transistor (Q_7) dont la base est connectée à la première alimentation, dont le collecteur est connecté à la seconde alimentation, et dont l'émetteur est connecté à la borne de sortie.

6. Circuit pour la génération d'une tension de référence selon la revendication 2, caractérisé en ce que l'amplificateur à réaction (2b) est un amplificateur fonctionnant sur la composante négative de la phase qui est connecté entre le collecteur du second transistor et la première alimentation.

7. Circuit pour la génération d'une tension de référence selon la revendication 6, caractérisé en ce que l'amplificateur fonctionnant sur la composante négative de la phase comprend un cinquième transistor (Q_{10}) dont la base est connectée au collecteur du second transistor (Q_2),

dont l'émetteur est connecté à la masse, et dont le collecteur est connecté à la première alimentation, et une troisième résistance (R_S) qui est connectée entre la première alimentation et la seconde alimentation.

8. Circuit pour la génération d'une tension de référence selon l'une quelconque des revendications 1 à 7, caractérisé en ce qu'une résistance servant à la compensation d'un décalage est insérée entre l'émetteur du premier transistor (Q_1) et la masse.

9. Circuit pour la génération d'une tension de référence selon l'une quelconque des revendications 1 à 7, caractérisé en ce qu'une résistance (R_{E1}) servant à la compensation d'un décalage est insérée entre la masse et la jonction de l'émetteur du premier transistor et de la première résistance.

10. Circuit pour la génération d'une tension de référence, comprenant: un premier transistor (Q_1) et un second transistor (Q_2) dont les bases sont connectées ensemble, la surface de la région d'émetteur du second transistor étant supérieure à celle du premier transistor, et l'émetteur du premier transistor étant relié à la masse et une première résistance (R_1) étant connectée entre l'émetteur du second transistor et la masse; et caractérisé par une seconde résistance (R_{12}) connectée entre la base du premier transistor et une borne de sortie (V_B); un troisième transistor (Q_5) et un quatrième transistor (Q_4) dont les collecteurs sont connectés aux collecteurs des premier et second transistors, respectivement, dont les émetteurs sont connectés à la borne de sortie (V_B), dont les bases sont connectées ensemble, et dont la base et le collecteur du quatrième transistor (Q_4) sont connectés ensemble; un circuit générateur de tension connecté entre la masse et les bases interconnectées des premier et second transistors; un cinquième transistor (Q_9) dont la base est connectée au collecteur du premier transistor et dont l'émetteur est relié à la masse; un condensateur (C_1) connecté entre la base du cinquième transistor et la masse; un sixième transistor (Q_8) dont la base est connectée au collecteur du cinquième transistor, dont l'émetteur est connecté à une alimentation, et dont le collecteur est connectée à la borne de sortie; et une troisième résistance (R_S) qui est connectée entre ladite alimentation et la borne de sortie.

Fig. 1

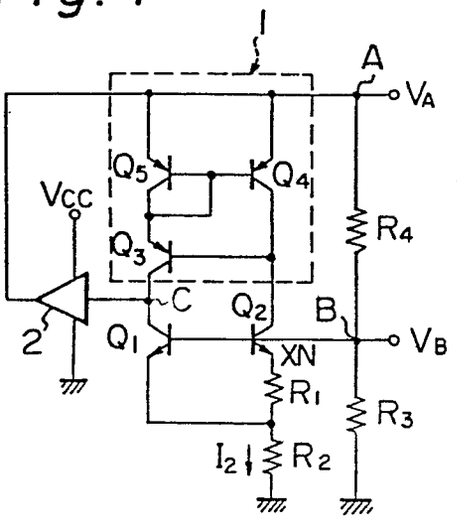

Fig. 2

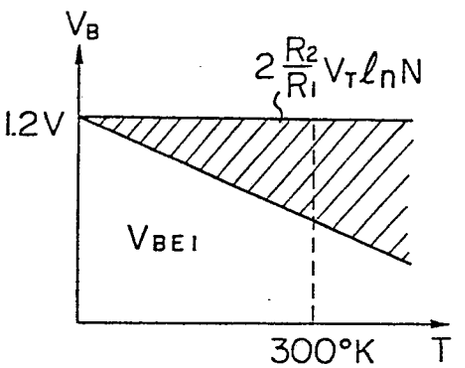

Fig. 3

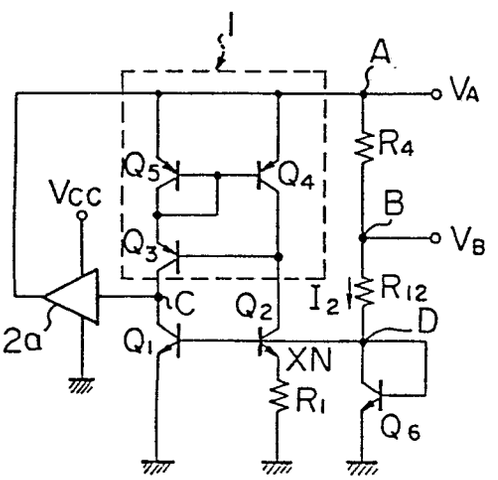

Fig. 4

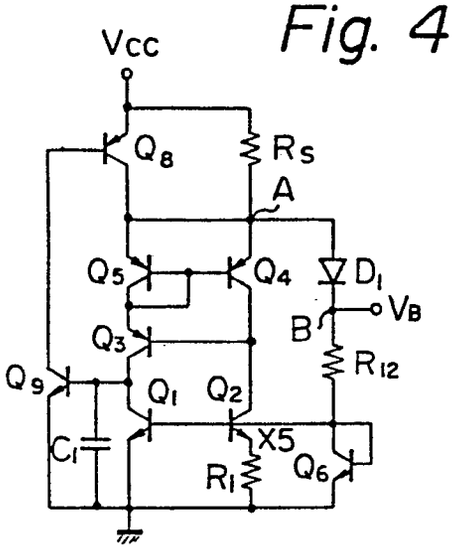

Fig. 5

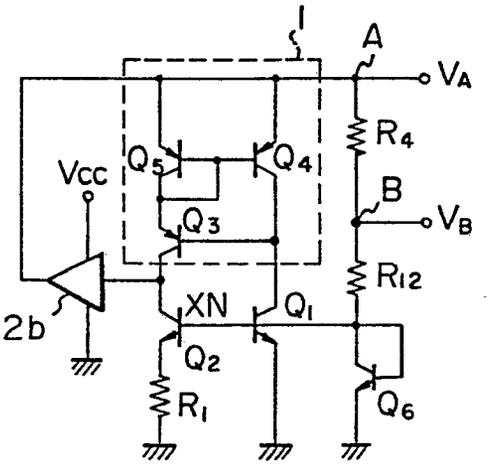

Fig. 6

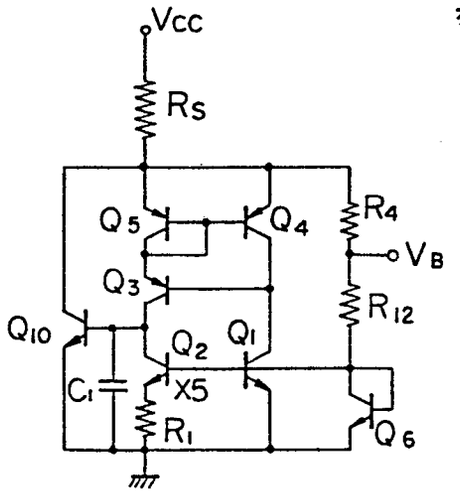

Fig. 7

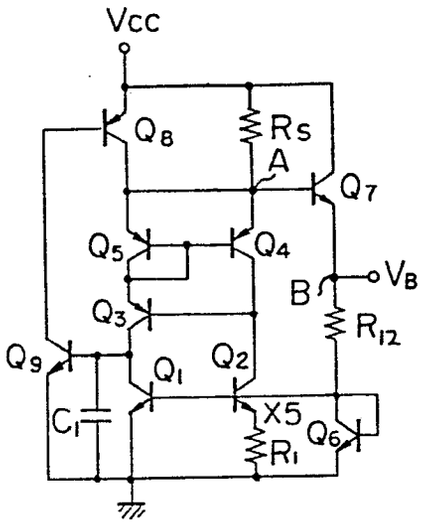

Fig. 8

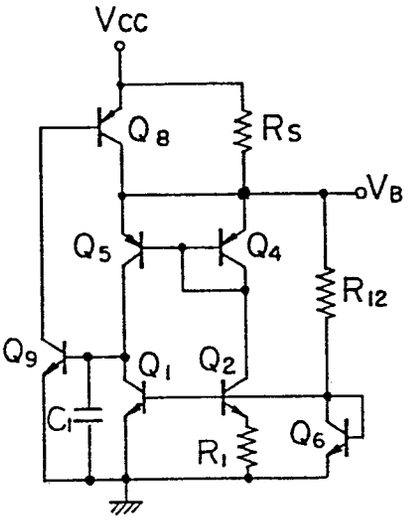

Fig. 9A

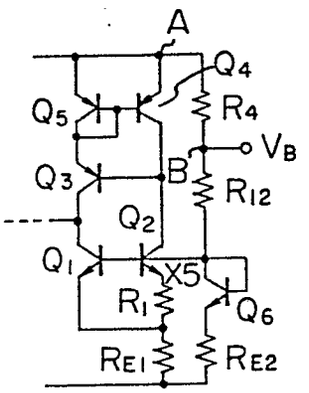

Fig. 9B