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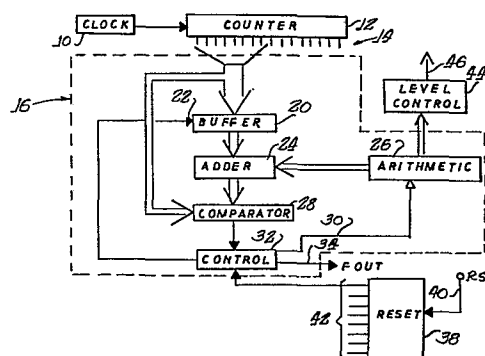
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54 Programmable tone generator.

57 A programmable tone generator for an electronic musical instrument generates a pulse train output (F out) in which in each cycle the starting time and duration of each pulse is controlled, thereby to determine the harmonic content of the electronic waves that are converted to audio sound. A binary counter (12) serves as a time base for encoding each period of a tone signal waveform into plural outputs (14) in the form of a binary code. A plurality of programmable tone generation circuits (16) are coupled with selected counter outputs (14) to comprise plural tone signal branches (16), each providing a tone signal at a selected fundamental frequency and having selected harmonic content. Each tone signal branch (16) includes a programmable variable code generator (26) and determines the initial content of the output waveform, subsequently either maintaining or changing the fundamental frequency and harmonic content thereof.



Electrical generation of suitable tone signals in electronic musical instruments has been accomplished in the past by many different arrangements. In recent years, the prevalent practice has been to provide oscillators for separately generating tone signals corresponding to the semi-tones of the top octave of the instrument or above, and providing each oscillator with a chain of divide-by-two circuits to produce the corresponding frequencies (lower order harmonics) in lower octaves of the instrument. This approach of course requires individual tuning of twelve oscillators.

Recent developments in integrated circuit technology have made possible the use of a single high frequency oscillator driving parallel divider circuits each providing a suitable divider ratio to produce one of the twelve frequencies of the top octave of the instrument. These divider chains are then followed by divide-by-two circuits as in the previous example to produce the corresponding frequencies in lower octaves of the instrument. Such circuits are advantageous in requiring tuning of but a single oscillator. However, these circuits have presented problems in obtaining accurate division ratios and suitable waveform symmetry that are difficult and costly to solve.

In both of the foregoing systems, the use of conventional divider circuits results in generation of square waves (i.e., 50% duty cycle rectangular waves), thus limiting the harmonic structure of the tone signal at the outputs of such generators to the harmonic spec-

trum of a square wave. Thus, to obtain other desired musical sounds, it is necessary to provide other circuitry, which is often quite cumbersome and expensive, to modify, combine, reshape and/or filter these waveforms as necessary to produce the desired musical sounds. For example, some systems utilize analog wave-shaping techniques to produce harmonically rich waveforms, and then selectively filter these waveforms to approximate the desired harmonic structure of the output waveform. Generally speaking, such analog circuits are subject to problems in maintaining accurate and noise free signals during analog signal processing. Moreover, such analog circuits have generally been cumbersome and expensive, due to the great redundancy of circuits generally required to produce the number of voices required even for a relatively simple instrument.

Accordingly, it is a general object of the present invention to provide a new and improved tone generating method and apparatus for an electronic musical instrument which is capable of producing a tone signal output at a desired fundamental frequency having a desired harmonic content.

A more specific object of the present invention is to provide tone generating method and apparatus for an electronic musical instrument which is programmable for initially determining and thereafter for selectively maintaining or changing the fundamental frequency and harmonic content of the tone signal output thereof.

A related object is to provide a tone generating method

and apparatus of the type described which is entirely digital in form, replacing all analog elements of other conventional tone generation methods and apparatus, and which provides a digitally derived signal output which may be applied directly to conventional analog sound reproduction elements.

Briefly, and in accordance with the foregoing objects, a method for tone signal generation according to one aspect of the present invention comprises producing a clock signal at a predetermined frequency, producing an advancing binary encoded count on a plurality of outputs in response to said clock signal, and digitally processing the count at selected ones of said outputs to produce a series of pulse output signals, said digital processing including controlling in a predetermined fashion the width of each said pulse signal produced and the spacings therebetween, thereby producing a composite tone signal of predetermined fundamental frequency and harmonic content.

A tone signal generator according to another aspect of the invention comprises a clock pulse generator, counter means having an input coupled to said clock pulse generator and having output means, at least one digital signal processing circuit coupled to said output means and having a tone signal output which is a composite signal comprising a series of digital signal segments and a programmable variable number source coupled to supply predetermined digital numbers to said digital processing circuit and cooperating therewith to individually control the duration of each of said digital signal segments, thereby constructing said composite signal at a predetermined fundamental frequency and having predetermined harmonic content.

The present invention will be more readily understood upon reference to the following detailed description of the illustrated embodiment together with the accompanying drawings, wherein:

FIGURE 1 illustrates, in block diagrammatic form, the novel tone generating circuit of the present invention;

FIG. 2 is a waveform diagram illustrating one form of output signal of the circuit of FIG. 1;

FIG. 3, FIG. 4 and FIG. 5 are circuit schematics illustrating portions of the block diagram of FIG. 1 in additional detail;

FIG. 6 illustrates an addition to the circuit of FIG. 1, in accordance with a further aspect of the present invention;

FIGS. 7 and 8 are circuit schematics illustrating further additions to the circuits of the preceding figures, in accordance with further aspects of the invention; and

FIG. 9 is a circuit schematic, partially in block form, illustrating an alternate form of a tone generating system in accordance with the principles of the present invention.

In FIG. 1, a novel tone signal generation system in accordance with the present invention is illustrated

in block diagrammatic form. Advantageously, the circuit of this invention is capable of generating a composite output signal in the form of a series of pulse signals or a pulse train whose individual sections or segments are controllably varied in width or time duration as well as in amplitude. Accordingly, this composite tone signal output exhibits a desired harmonic content or spectrum. As a further advantage, the circuits of the invention are all in digital logic form, capable of incorporation on a large scale integrated circuit (LSI) chip, utilizing conventional manufacturing techniques, thus enhancing the cost effectiveness as well as the reliability of the system of the present invention.

Initially, FIG. 1 illustrates a clock or high frequency oscillator 10 which presents a suitable high frequency pulse train to a multi-stage binary counter 12, which preferably comprises an eight-bit synchronous binary counter. Accordingly, the counter 12 presents eight bits or binary outputs designated generally 14. In the illustrated embodiment, these counter outputs 14 are utilized to drive eight substantially identical digital processing circuits 16. In order to facilitate the description only one such digital processing circuit 16 is illustrated. Each such digital processing circuit 16 utilizes the eight counter outputs 14.

Each circuit 16 produces a pulse train comprising a series of pulse signals, sections or segments, which may take, as one example, the form illustrated in FIG. 2. This series generally designated 18, of pulse signals or segments 18a, 18b, etc., includes in the illustrated embodiment, six such signals, sections or segments 18a, 18b, etc., which might be called pulses

and spaces. In the illustrated embodiment, the period of the pulse train is variable with a minimum of six and maximum of 512 counts from the clock 10 via the counter 12. As will be seen later, both the width and the amplitude of each of these sections may be varied in accordance with novel aspects of the present invention, thus the designation of "pulse" and "space" of the signal train or series 18 illustrated in FIG. 2 may not be strictly accurate in all cases, whereby the terms "section" or "segment" are frequently utilized hereinbelow. It will also be recognized that the specific example heretofore given is for purposes of illustration only, and is not to be construed as limiting the invention in any fashion.

Referring again to FIG. 1, the digital processing circuit 16 includes a buffer circuit 20 which receives the associated eight output lines 14 of the counter circuit 12. In the preferred embodiment, this buffer circuit 20 comprises a latch, which is controlled at an input 22 thereof for latching or holding the count from the first outputs of the counter 12. The control signal at the input 22 and the time sequence in which it latches the ongoing count from the counter 12 will be described later. The buffer or latch 20 feeds the eight-bit binary signal which has been latched from the counter 12 to an eight-bit adder circuit 24. This adder circuit 24 receives a second eight-bit binary encoded signal from an arithmetic unit 26. The adder 24 functions to sum or add the two eight-bit binary encoded signals at its respective inputs and to produce this sum as an eight-bit binary encoded output feeding one compared input of a comparator circuit 28. The comparator circuit receives as a second compared input, an eight-bit binary encoded signal direc-

tly from the same eight outputs 14 of the counter circuit 12 which feed the buffer 20. The comparator 28 compares these two eight-bit binary encoded input signals and produces a control output signal indicating whether or not these two signals are identical. This output control signal feeds a control circuit 32 which responds by providing suitable control signals both for the arithmetic unit 26 (via a line 30) and for the control input 22 of the latch or buffer 20 as will be described in additional detail later herein. The control circuit 32 also produces a resultant or composite tone signal output (F out) on a line 34.

A suitable reset circuit 38, as shown in FIG. 5 and described later, feeds all the eight like digital processing circuits 16, therefore being illustrated outside of the dashed line. This reset circuit receives a reset signal (RST) at an input line 40, and feeds the reset signal in a predetermined sequence to each of eight output lines, designated generally 42, for resetting each of the eight control circuits 32 of the digital processing circuit 16.

In accordance with a further novel aspect of the invention, a pulse height or level control circuit 44 may be utilized to achieve individual control of the level or height of each of the signal sections, e.g., 18a, 18b, etc., as illustrated in FIG. 2. This circuit 44 receives further outputs of the arithmetic circuit 26 and produces pulse height or level controls signal at an output 46.

It will be constructive to now briefly consider the operation of the present invention with reference to the block diagram of FIG. 1. The arithmetic unit 26

generally comprises a programmable, variable number or code source which outputs a control number or code to the adder 24. The code source stores an initial binary encoded number as an initial control output for each section of the signal to be produced. With reference to the example given in FIG. 2, a separate such initial number or code would therefore be stored in the arithmetic circuit 26 for each segment or section 18a, 18b, etc. This signal corresponds to the actual number of clock pulses to be counted by the counter 12 for that output signal section. In accordance with an important feature of the invention, these numbers are separately programmable in the arithmetic circuit 26 for each of the digital processing circuits 16, and therefore can be utilized to produce as many different tone signals as there are digital processing circuits 16 in the instrument.

After a desired number of cycles of production or period of time of the pulse series (e.g., series 18 of FIG. 2) in accordance with the initial control side, which number is also programmed into the arithmetic circuit 26, the binary encoded control numbers output by arithmetic unit 26 may be altered, for modifying the next number of cycles accordingly. This alteration is also programmed into each unit 26. It should be recognized in this connection that by cycle is meant a given group or series of digital signals or pulses, the example of FIG. 2 illustrating a cycle or series 18 comprising six such segments or sections. The arithmetic circuit 26 may further be programmed for modifying the binary encoded control number output a given number of times, whereupon a stable state is reached at which the circuit 26 continues to generate a fixed binary encoded signal output, again dependent

upon the programming thereof.

Referring now to FIG. 3, the arithmetic unit 26 is illustrated in circuit schematic form. A read only memory (ROM) portion of the circuit comprises two integrated circuit ROM's 50 and 52, which in the illustrated embodiment each comprises an integrated circuit ROM of the type generally designated MM5202A. In the embodiment illustrated in FIG. 3, the ROM 50 is utilized to store six eight-bit words while the ROM 52 is utilized to store up to six two-bit words. Thus, the ROM space utilized in the embodiment illustrated in FIG. 3 comprises six, ten-bit words. The eight bits of each word contained in ROM 50 comprise the binary encoded number or code which determines the duration or width of a respective section of the tone signal output, e.g., the widths of sections 18a, 18b, etc., of the waveform 18 of FIG. 2. The two binary encoded output bits of each word which are stored in the ROM 52 are controls or "flags", utilized, respectively, to indicate whether the section width or duration should be modified in succeeding cycles of the output waveform, and whether it should be increased or decreased.

The ROM's 50 and 52 are addressed by a counter 54 which receives its clock input from the output line 30 of the control circuit 32. This signal and its derivation will be explained in detail hereinafter. Suffice it to say that this signal on the line 30 goes low (i.e., logic "0") at the end of each section of the signal output (e.g., sections 18a, 18b, etc., of the waveform 18 of FIG. 2). The counter circuit 54 is preferably of the type generally designated 74LS93 and is decoded via a suitable logic circuit including

an AND gate 56 and an OR gate 58, to count from zero through five. Three similar counter circuits 60, 62 and 64 are interconnected with the counter 54 and each other, to comprise a counter chain, which provides a clock pulse to a seven-bit counter comprising a pair of further similar counter circuits 66 and 68. In the illustrated embodiment, the counters 60, 62, 64, 66 and 68 are all integrated circuits of the type generally designated 74LS93. The counters 62 and 64 together comprise a programmable counter for preselecting the number of counts therefrom necessary to provide each clock to the counter 66. This programming or preselection is accomplished by providing a suitable jumper between a selected output of counters 62 and 64 and one input of a two-input AND gate 69 which feeds the clock input of the counter 66. The other input of the AND gate 69 is fed from the output of a six-input NAND gate 71, which is utilized to provide a maximum count lockout. The inputs to the NAND gate 71 are also programmed by being selectively jumpered with the outputs of the counters 66, 68, thereby programming the maximum count for lockout. This process also allows the number of pulse pattern changes available for each such circuit 16 to be pre-programmed into the circuit. The invention is not limited, however, to such a counter chain, since other circuits may be utilized to perform this function. For example, an asynchronous oscillator circuit (not shown) might be arranged to provide an adjustable period for controlling these pulse pattern changes.

It will be appreciated from the foregoing that each of the circuits 16 may be individually programmed to achieve the desired pattern of output pulses. Advantageously, the novel yet simple expedient of separately

programming the respective ROM's 50 and 52, as well as the counters 62, 64, 66 and 68 is all that is required. In all other respects, the remaining portions of the arithmetic unit circuit 26, and all other components, are identical for each digital processing circuit 16.

In operation, the six-bit output of the counters 66 and 68 are utilized to provide a number, programmed as described above, which is either added to or subtracted from the eight-bit ROM number at the output of the ROM 50. This addition or subtraction is carried out by a pair of four-bit adders 70, 72, which receive one set of inputs to be added from the ROM 50 directly, and receives the other set of inputs to be added from the six-bit counters 66, 68 via suitable intervening logic. The adders 70 and 72 output an eight-bit signal comprising the sum of these two signals on eight output lines designated generally 74 (and separately designated 74-1, 74-2, 74-3, 74-4, 74-5, 74-6, 74-7, 74-8).

The decision as to when and how to modify the eight-bit output of the ROM in the adders 70, 72 is also programmed into ROM 52. As mentioned briefly above, one bit output ROM 52 determines whether or not the count from the counters 66, 68 will be fed through to the adders 70, 72, to combine with the output of ROM 50. In the illustrated embodiment, this is output 76 of ROM 52 and is connected via a suitable buffer 78 to one input of each of a plurality of two-input AND gates designated generally 80, the other input of each of these AND gates 80 being joined with a respective output of a group of exclusive OR gates 84.

The remaining bit output of the ROM 52 controls whether the six-bit signal from the counter 66, 68, once allowed in accordance with the state of the bit output 76, will be added or subtracted, at the adders 70 and 72, to the eight-bit signal from ROM 50. This control bit is output 82 and feeds one input of each of a plurality of two-input exclusive OR gates designated generally 84, via a suitable buffer 86. The other inputs of these exclusive OR gates 84 are fed from the respective outputs of the previously described counters 66 and 68. From the foregoing it will be seen that when the bit output 76 of ROM 52 is high, the six-bit signal from counters 66 and 68 will be allowed at the adders 70 and 72 and conversely, when the bit 76 is low, these same signals will be inhibited. When the bits 76 and 82 of ROM 52 are both high, the six-bit output of the counter 66 and 68 will be subtracted from the eight-bit output of ROM 52 by the adders 70 and 72, while if bit 82 is low, the six-bit number will be added to the eight-bit number. When the bit 76 is low, all zeros will be presented at those inputs of the adder 70 and 72 normally receiving the six-bit output of counter 66 and 68, whereby the eight-bit output of ROM will be reproduced unaltered at the output 74. The foregoing may of course be achieved as desired by programming the bits 76 and 82 accordingly. In the illustrated embodiment, the circuit of FIG. 3 effects at most a one-bit change in the output signal 74 per segment, per cycle of the tone signal output, it being remembered that one cycle in the illustrated embodiment comprises six segments or sections, with reference to FIG. 2.

Referring now to FIG. 4, the remaining elements of the digital processing circuit 16 are illustrated,

together with the counter 12 and an associated clock 90. The clock 90, in the case of the first of the processing circuits 16, is the clock or external oscillator 10. This oscillator 10 as previously mentioned, outputs a square wave pulse train at a fixed frequency, which in the illustrated embodiment, is on the order of 1.7 megahertz. The counter 12, in the illustrated embodiment, comprises two, four-bit synchronous counter circuits 91, 92 and interconnected to form an eight-bit synchronous counter. The outputs of the synchronous counter feed the illustrated first signal processing circuit 16 comprise the four output bits (F1, F2, F3, F4) of the counter circuit 91 and the four bits (F5, F6, F7, F8) of the counter circuit 92. In the illustrated embodiment, the counter circuits 91 and 92 comprise integrated circuits of the type generally designated 74LS161.

The buffer 20 comprises a pair of four-bit latch circuits 95 and 96, which have their input terminals joined with the respective outputs of the counters 91 and 92. The load control input line 22 of the latches is fed from the control circuit 32, as mentioned previously. The output lines of the latches 95 and 96 also comprise four bits each and feed respective input terminals (A) of two four-bit adders 97 and 98, which form the adder circuit 24 of the block diagram of FIG. 1. These adders 97, 98 receive at their other inputs (B) the output lines 74 from the adders 70, 72 of the arithmetic circuit 26 of FIG. 3 as designated by the use of the like reference numerals 71-1 through 71-8. The adder circuits 97 and 98 preferably comprise integrated circuits of the type generally designated 74LS83, while the latches 95 and 96 preferably comprise integrated circuits

of the type generally designated 74LS95.

The summed outputs (A+B) of the adders 97 and 98 comprise four-bit outputs which feed corresponding four-bit input terminals (A) of a pair of four-bit comparators 99 and 100, which comprise the comparator 28 of the block diagram of FIG. 1. The other compared inputs (B) to the comparators 99 and 100 are the four-bit counter outputs of the counters 91 and 92, respectively. The compare output (A=B) of comparator 100 is fed as an input to comparator 99 whose compare output (A=B) forms the input to control circuit 32.

The control circuit 32 comprises a pair of flip-flops 101 and 102 and an AND gate 104. The comparator 99 output line (A=B) feeds the clear input of flip-flop 101, whose clock input is fed directly from the clock 90. The $\bar{Q}$ output of flip-flop 101 comprises the output line 30 for this circuit 32, which is the same control line feeding the clock input of the counter 54 of FIG. 3, and the clock input for flip-flop 102 whose clear input is driven from the first reset line 42 of the block diagram of FIG. 1. The $\bar{Q}$ output of flip-flop 102 forms one input to the AND gate 104 whose other input is tied to the same reset line 42. The output of AND gate 104 forms the tone signal output (F out) on line 34 of the digital processing circuit 16.

With reference to FIG. 5, the Reset circuit 38 of the block diagram of FIG. 1 is illustrated in detail, whereby the derivation of the reset signal on lines 42 will now be described in detail. The reset circuit 38 includes a demultiplexer circuit comprising a pair of three-line-to-eight-line demultiplexers 110

and 112. In the illustrated embodiment, the demultiplexers 110 and 112 are integrated circuits of the type generally designated 74LS138. An externally generated, multiplexed reset signal (RST) feeds the input line 40 to the circuit, which becomes a first enable signal of the demultiplexer 110. Select inputs of the demultiplexers 110 and 112 are fed in common from three lines designated generally 114 which are provided with suitable external timing signals, in synchronization with the multiplexing of the reset signal (RST) at the line 40. The unselected outputs of demultiplexers 110 and 112 remain high, while selected outputs go low.

The eight outputs of demultiplexers 110 and 112 each drive the input of one of sixteen inverters designated generally 116. The inverters 116 associated with the outputs of the demultiplexer 110 each feed the clock (C) input of one of a corresponding plurality of flip-flops designated 118. The inverters 116 associated with the outputs of the demultiplexer 112 each feed one input of one of a corresponding plurality of three-input NAND gates designated generally 120. The second input of each of the NAND gates 120 is fed directly from a respective output of the demultiplexer 110, while the third inputs thereof are all tied in common to a control signal line 122. This control signal on line 122 comprises a sample pulse occurring during the last quarter of each multiplexing clock cycle (i.e., the cycle in which the multiplex clock control signals are given over the lines 114). It will be understood that these multiplex signals and control lines are for use with an electronic musical instrument which utilizes multiplexing and demultiplexing circuits, and is provided with common control signals

therefor to assure proper synchronization between the operations of the various related multiplexed and/or demultiplexed circuits. Such multiplexing and demultiplexing components form no part of the present invention, however, and therefore need not be described in detail.

The outputs of the NAND gates 120 feed respective reset (R) inputs of the flip-flops 118. The Q outputs of the flip-flops 118 form the respective reset lines 42 for the eight circuits 16. In the illustrated embodiment, the lines 114 present a binary encoded count which advances at a 30 KHz rate.

Referring now to FIG. 6, the pulse height or level control circuit 44 is illustrated. This circuit 44 comprises three multiplexer circuits 130, 132 and 134, which in the illustrated embodiment are all of the type generally designated 74151. These multiplexers have respective output select inputs driven in common from the three control lines designated generally 114, which are the same lines 114 associated with the circuit of FIG. 5. It will be recognized that these three lines present three bits of multiplexing and demultiplexing information, suitable for handling the eight data processing circuits 16 of the illustrated embodiment. The multiplexed inputs of multiplexers 130, 132 and 134 are provided in serial fashion from the respective ROM 52 in each of the data processing circuits 16. In order to accommodate the pulse height adjusting feature, the utilization of these ROM's 52 is increased by three bits, thereby providing for programming of eight possible amplitude levels. These three additional bits are generally designated 138, only one such ROM 52 and its bit outputs 138 being

illustrated to facilitate clarity in the drawing.

Referring again briefly to FIG. 3, a further optional feature comprises external selection of pulse patterns. To this end, a pair of terminals 140, 142 are joined with respective additional address inputs of each of the ROM's 50 and 52. These additional address lines are wired in common to the ROM's 50, 52 for each of the eight digital processing circuits 16. The lines 140, 142 directly join external selection means such as a suitable switch, or the like, for selecting additional words programmed into the ROM's 50, 52 responsive to these two address inputs.

Reference is now invited to FIG. 7 and FIG. 8, wherein additional control circuits, which may be associated with each data processing circuit 16 of the block diagram of FIG. 1, are illustrated. The ROM's 50 and 52 are shown in FIG. 7 as a decoder and a matrix array associated with the counter 54 of FIG. 3. It will be remembered that each ROM 50, 52 may be programmed with six, eight-bit words for each processing circuit 16. Accordingly, the matrix array of FIG. 7 illustrates six, sixteen-bit words, representing the contents of both ROM's 50 and 52 for one processing circuit 16. The ROM's 50 and 52 are provided with a three-line-to-six-line decoder circuit 150, which receives the count from counter 54 and decodes into six lines for selectively addressing one of the six words of the ROM 50, 52.

As described above, the first eight bits, here designated generally 152, provide "transition time" or signal segment width information to the adder 70, 72 of FIG. 3. The next two bits 76 and 82 are the same as

like numbered bits of ROM 52 in FIG. 3, providing the "change or maintain" information and the "add or subtract" information to the other circuits of FIG. 3. The next three bits are the bits 138 containing pulse height or level information, as described above with reference to FIG. 6. The remaining three bits, designated generally 154, may be selectively utilized to program other suitable information for the tone signal segments associated with these six words of ROM's 50 and 52.

A digital logic control circuit is provided for utilizing the bits 138 and 154 in conjunction with a mode and enable control circuit illustrated in FIG. 8. The logic control circuit of FIG. 7 comprises an array of six two-input AND gates designated generally 156 each having one input tied to a respective one of the ROM bits or output lines 138 and 154. The second inputs of the last three AND gates 156, as viewed from the left to right in FIG. 7, are fed from the output of an inverter 155, while the second inputs of the remaining three AND gates 156 are fed the opposite sense signal taken at the input of inverter 155. The outputs of the first three AND gates 156 are fed to one input of each of three, two-input OR gates designated generally 158, which receive their second inputs from the respective outputs of the remaining three AND gates 156.

Referring now to FIG. 8, outputs 157, 159 and 161 of the three OR gates 158 of FIG. 7 feed one input each of three OR gates designated generally 160. These three OR gates 160 feed the three inputs of a three-bit digital-to-analog converter 162, thereby converting to analog form the digitally encoded pulse height or

level signals carried in the ROM's 50, 52. The remaining inputs of the three OR gates 160 are fed in common from a control input 164. The mode and enable control circuit of FIG. 8 receives a second control input on a line 166, which feeds one input of a further two-input OR gate 168, whose opposite input is fed by the control line 30 from the flip-flop 101 of FIG. 4. The control input 164 also feeds an inverter 170 which in turn feeds one input of a two-input AND gate 172, whose other input is fed directly from the control input 166. The output 174 of AND gate 172 feeds the input of the inverter 155 of FIG. 7. The output of OR gate 168 feeds a reference input of the three input D-to-A converter 162.

In operation, the control inputs 164 and 166 are connected with control switches or other suitable control signal sources for receiving logic "1" or "0" signals to cause the circuits of FIGS. 7 and 8 to control the output pulses or tone signal segments in accordance with three possible modes of operation. With both inputs 164 and 166 at logic "0", the foregoing circuits will allow variation in segment width of all segments, e.g., 18a, 18b, etc., of FIG. 2, and in level or amplitude of alternate segments, e.g., segments 18a, 18c, and 18e of FIG. 2. With input 166 at logic 0 and input 164 at logic 1, segment width of each segment of the signal, e.g., segments 18a, 18b, etc. of FIG. 2, is variable. With input 166 at logic 1 and input 164 at logic 0, both width and level or amplitude of each segment of the output tone signal is variable.

Reference is now invited to FIG. 9, which shows a system incorporating eight separate notes or tone signals generated in accordance with the present invention

on one LSI circuit chip. The circuit of FIG. 9 makes use of eight of each of the components thus far described with reference to FIGS. 3, 4, 7 and 8, which are here each illustrated in block diagrammatic form. Several additional suitable control circuit elements are included to facilitate the incorporation of these eight similar circuits in one integrated circuit package.

These additional components comprise a pair of flip-flops 200 and 210, the flip-flop 200 receiving its D input from a "pulse out" signal terminal 202. This pulse out signal terminal 202 and the signal provided thereat form no part of the present invention and need not be described herein in detail. Suffice it to say, that a pulse signal will be developed at the pulse out terminal 202 in response to each actuation of a key on a keyboard of the associated electronic musical instrument. The Q output of the flip-flop 200 feeds the clock (CK) input of flip-flop 210, whose Q output in turn feeds the reset terminals of each of eight counter circuits, designated generally 212. These counter circuits 212 are each a counter chain similar to that comprising counters 54, 60, 62, 64, 66 and 68, illustrated in FIG. 3. Each counter 212 is associated with an arithmetic circuit and ROM's designated generally 214, each of which is similar to the remainder of the circuit illustrated in FIG. 3. The arithmetic circuits and ROM's 214 in turn each feed a transition circuit designated generally 216, each of which is the same as the circuit of FIG. 4, excluding the counters 80, 82, 84 and 86. These counters are replaced in the embodiment of FIG. 9 by a single eight-bit counter 218. The eight-bit counter 218 also drives the clock input of the flip-flop 200 and the reset

input of the flip-flop 210.

An additional circuit in the embodiment of FIG. 9 comprises a frequency and phase detector 220, which has one input fed from the eight-bit counter 218 and a second input fed by a frequency signal (F in) from the electronic musical instrument via a suitable buffer 222. The outputs of the frequency detector may be connected to suitable external circuit elements (e.g., filters) for use as desired, at terminals designated generally 224. The input to the eight-bit counter 218 is from a suitable external oscillator (e.g., a VCO) at a terminal 226. The period transition circuits 216 and additional bits of ROM information from the circuits 214 feed respective mode select and enable circuits, designated generally 228. These circuits 228 are each the same as circuits illustrated in FIG. 7 and FIG. 8. The interconnections of these circuits 228 with their associated period transition circuits 216 and ROM's in block 214 are the same as those described with reference to FIGS. 7 and 8. A separate D-to-A converter 162 is provided for each note or tone signal output, and each has its output, designated generally 230 tied to a suitable circuit for envelope control, such as FET's designated generally 232.

A suitable envelope control signal is provided at the gate electrode of each FET 232 from an external source 234. Accordingly, the envelope output signal appears at the opposite terminal of FET 232 at the circuit point designated 236. In the illustrated embodiment, the envelope control signals are applied to the outputs of the tone generation circuits in groups of three, three and two, viewed from top to bottom. Other enveloping arrangements may be utilized, the foregoing

forming no part of the invention but serving merely to give an example of a circuit embodying the present invention and including enveloping control.

While preferred embodiments of the invention have been illustrated and described herein, the invention is not limited thereto. On the contrary, various modifications, changes and alternatives may occur to those skilled in the art, and the invention includes such changes, modifications and alternatives insofar as they fall within the spirit and scope of the appended claims.

CLAIMS

1. A programmable tone generator comprising a digital signal processing circuit having an output tone signal which is a composite signal comprising a series of digital signal segments and a programmable variable number source coupled to supply predetermined digital numbers to said digital processing circuit and cooperating therewith to individually control the duration of each of said digital signal segments, thereby constructing said composite signal at a predetermined fundamental frequency and having predetermined harmonic content and characterized in that the programmable variable number source (26) comprises a first programmable number source (50) and a second programmable number source (62, 64) cooperating in circuit with said first programmable number source (50) to provide the predetermined digital numbers supplied to said digital processing circuit.

2. A programmable tone generator according to claim 1 wherein the first programmable number source (50) comprises a ROM (50).

3. A programmable tone generator according to claim 1 wherein said second programmable number source (62, 64) comprises a programmable counter circuit (62, 64).

4. A programmable tone generator according to claim 1 including a plurality of like digital processing circuits (16) and a plurality of independently programmable variable number sources (26) each coupled to one of said digital processing circuits (16).

5. A tone signal generator according to claim 2 wherein said first programmable number source (50) is addressed

by a counter (54) which defines the number of said signal segments in each cycle, each cycle comprising a like number of consecutive segments.

6. A programmable tone generator according to claim 1 further characterized in the provisions of a third programmable number source (52) for providing a control signal indicative of a desired amplitude for each digital signal segment.

7. A programmable tone generator according to claim 5 wherein said further programmable number source comprises a ROM (52).

8. A tone signal generator according to claim 6 wherein said third programmable number source (52) also controls the maintaining or changing of the width of signal segments at corresponding positions in successive ones of said cycles thereby selectively maintaining or changing the harmonic content of the tone signal output of the associated tone signal branch.

9. A programmable tone generator according to claim 1 and further comprising a clock (10) for producing a series of pulses at a predetermined frequency, a counter (12) having an input coupled to said clock (10) and a plurality of outputs (14), at least one tone signal branch (16) connected to selected ones of said outputs (14) and comprising said digital signal processing circuits (16) and producing a cyclical tone signal output, each cycle thereof comprising a predetermined plurality of contiguous signal segments and further characterized in that the first programmable number source (50) is coupled with said tone signal branch (16) and cooperates with said counter (12)

for controlling in a predetermined fashion the time duration of each said signal segment in a basic cycle of said cyclical tone signal output and second programmable number source (62, 64) cooperates with said first programmable number source (50) for controlling in a predetermined fashion the time duration of each said signal segment in each cycle of said cyclical tone signal output, thereby constructing the composite output tone signal of a predetermined fundamental frequency and of predetermined harmonic content from said tone signal branch.

10. A tone signal generator according to claim 9 wherein said clock (10) comprises a digital electronic clock circuit, wherein said counter (12) comprises a digital electronic N-bit binary counter circuit, and wherein each signal processing circuit (16) includes a latch circuit (20) and an adder circuit (24), said adder circuit (24) receiving one set of inputs from the latch circuit (20) and another set of inputs from said programmable variable number source (26), and a comparator (28) connected in circuit for comparing the output of the adder circuit (24) with the output of the counter (12), and for controlling operation of the latch circuit (20) in accordance with said comparison, and a control circuit (32) driven by the output of the comparator (28) and providing the output tone signal.

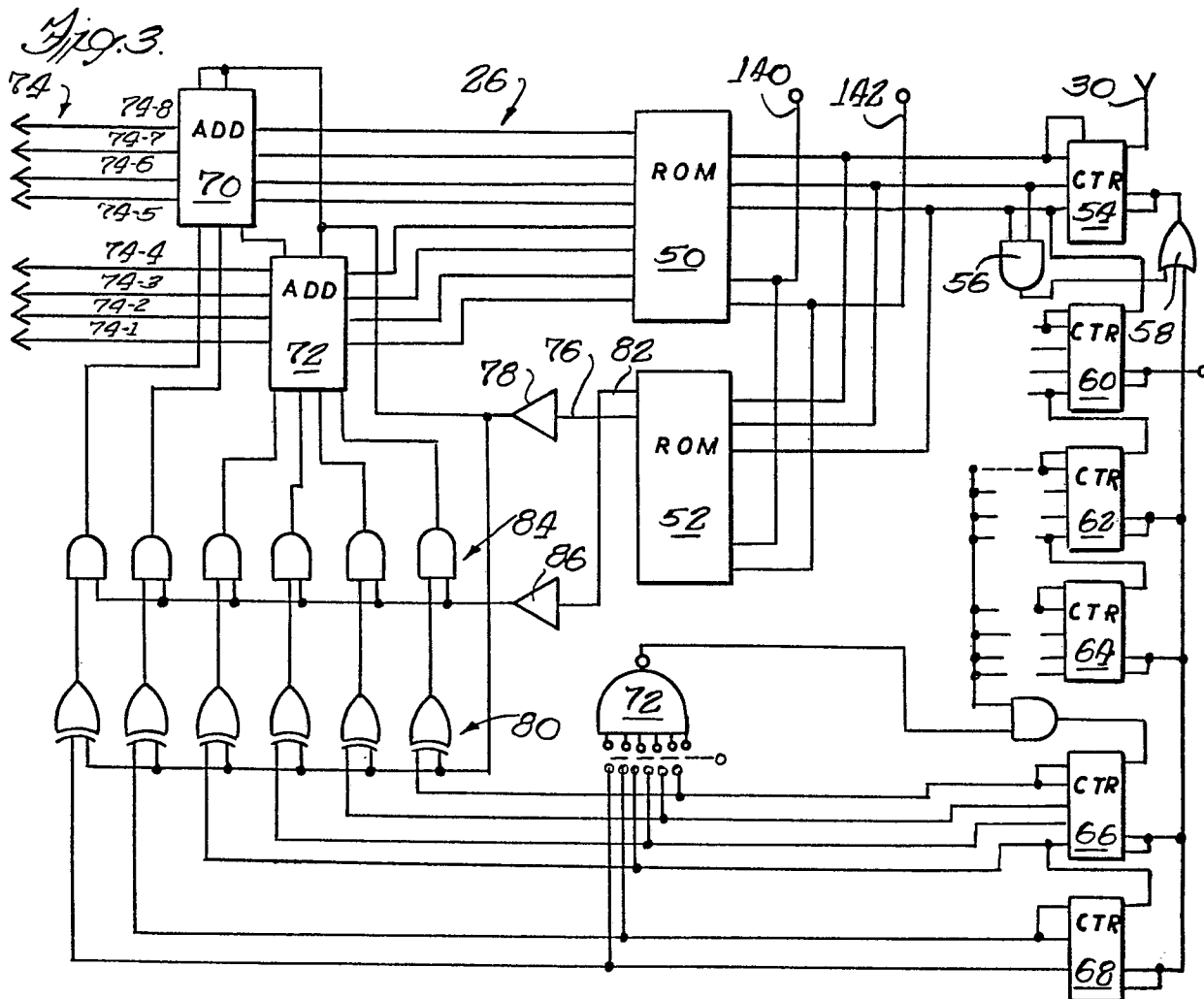
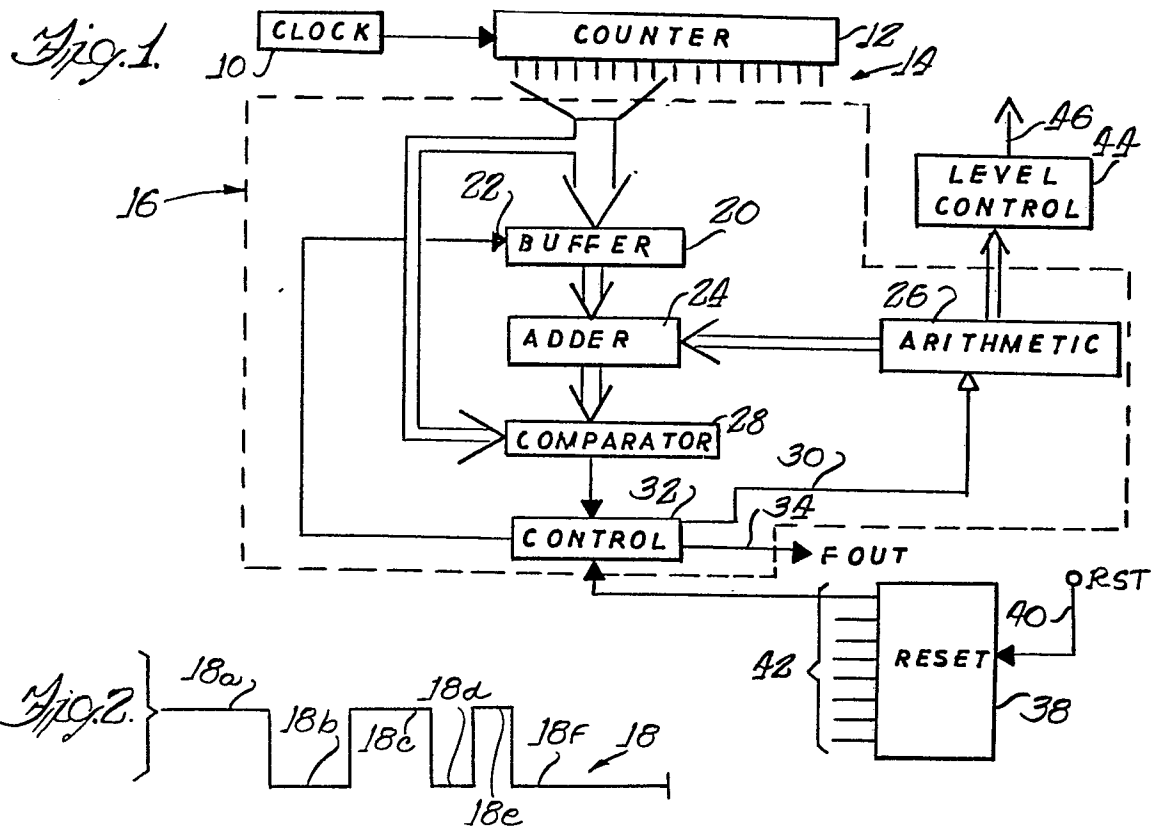


Fig. 4.

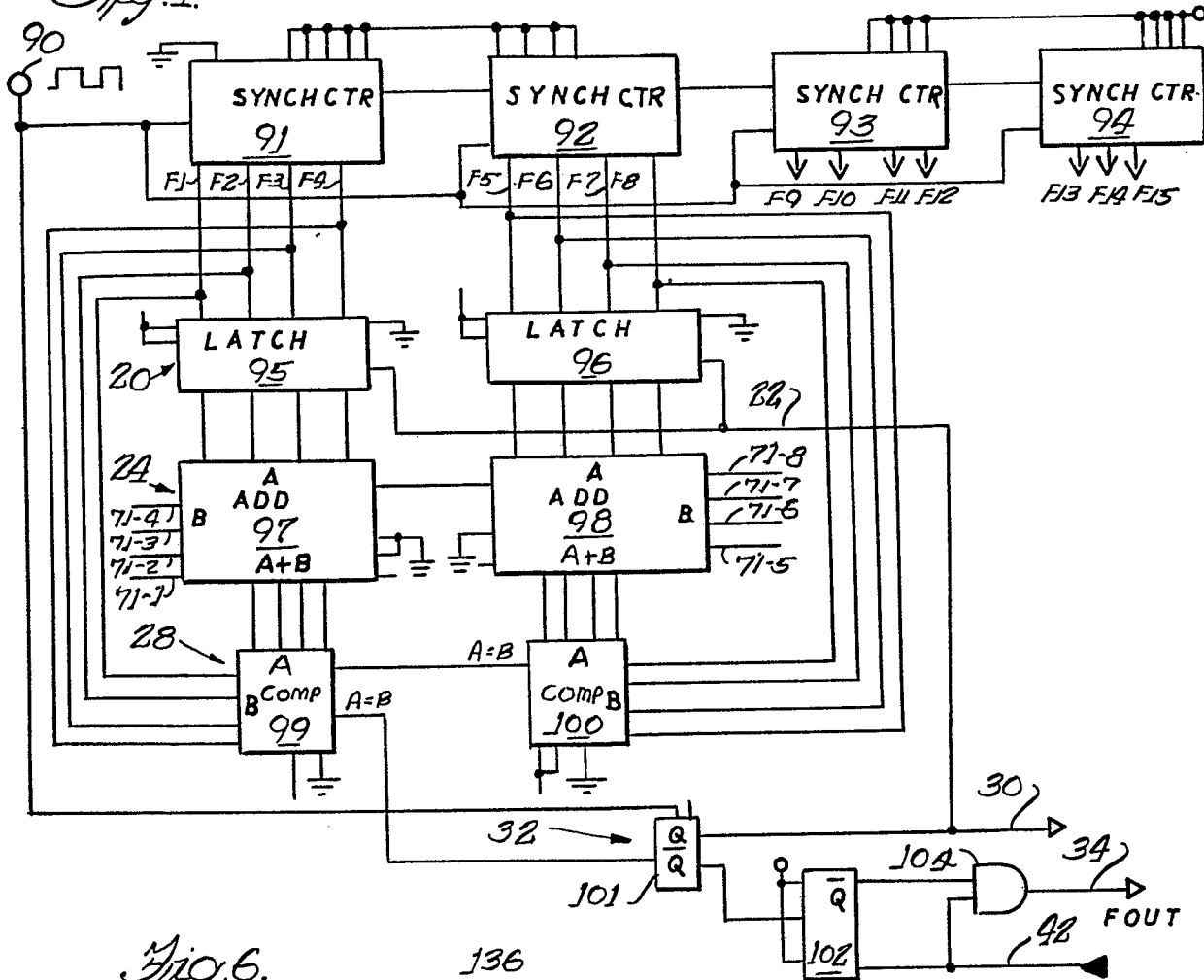


Fig. 6.

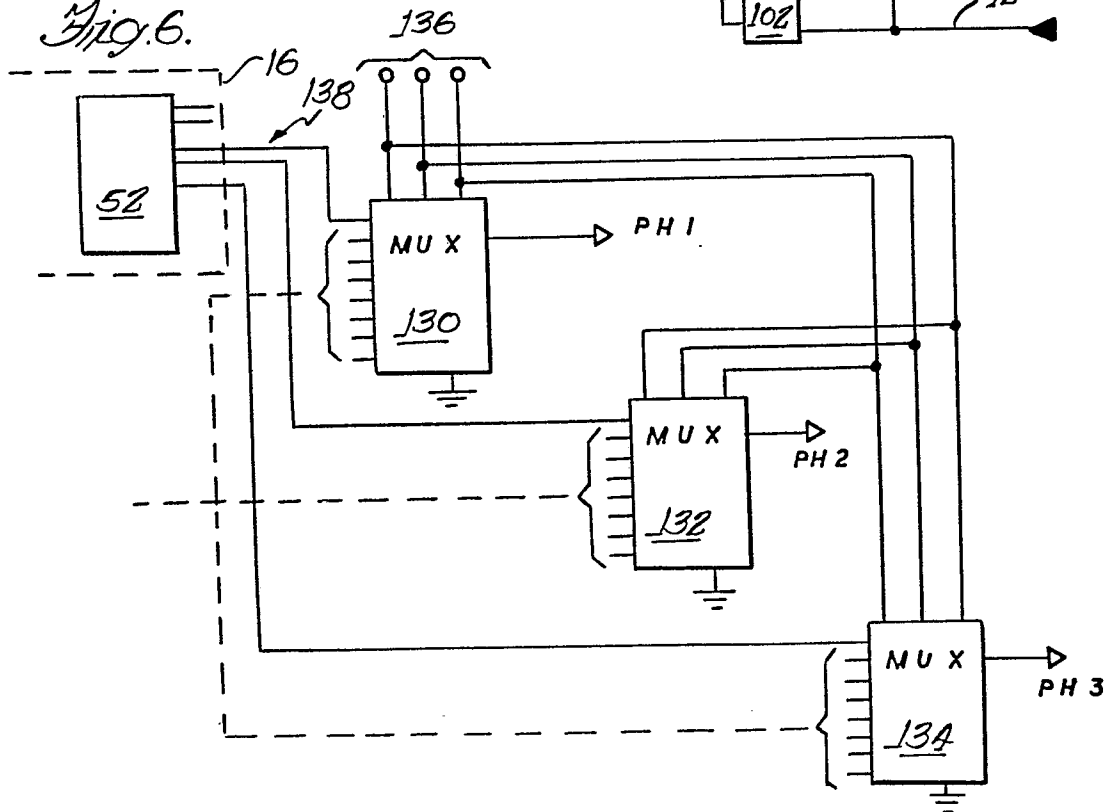
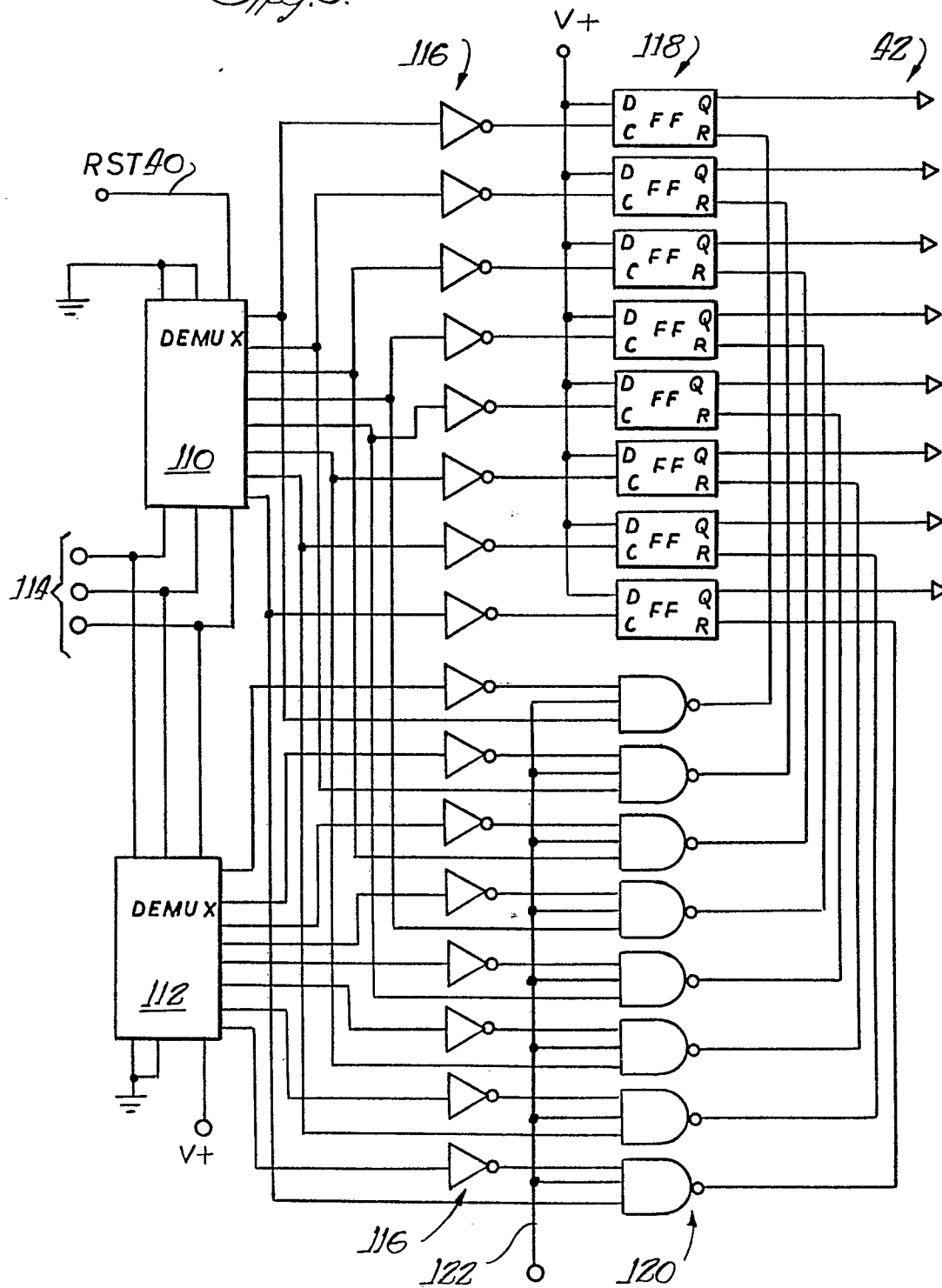
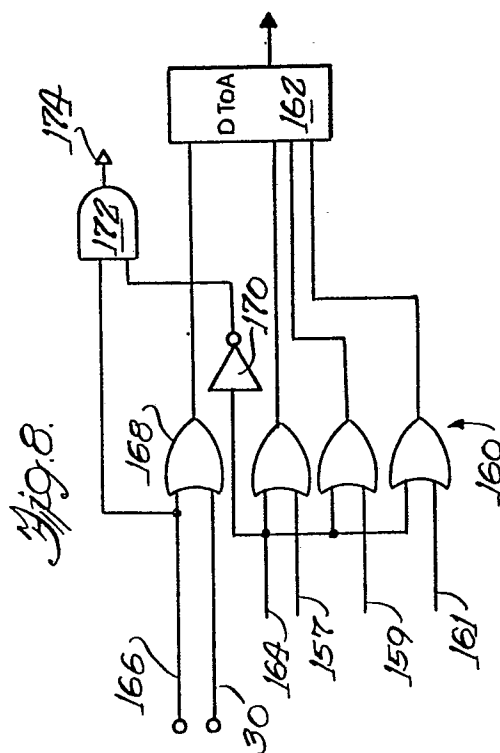
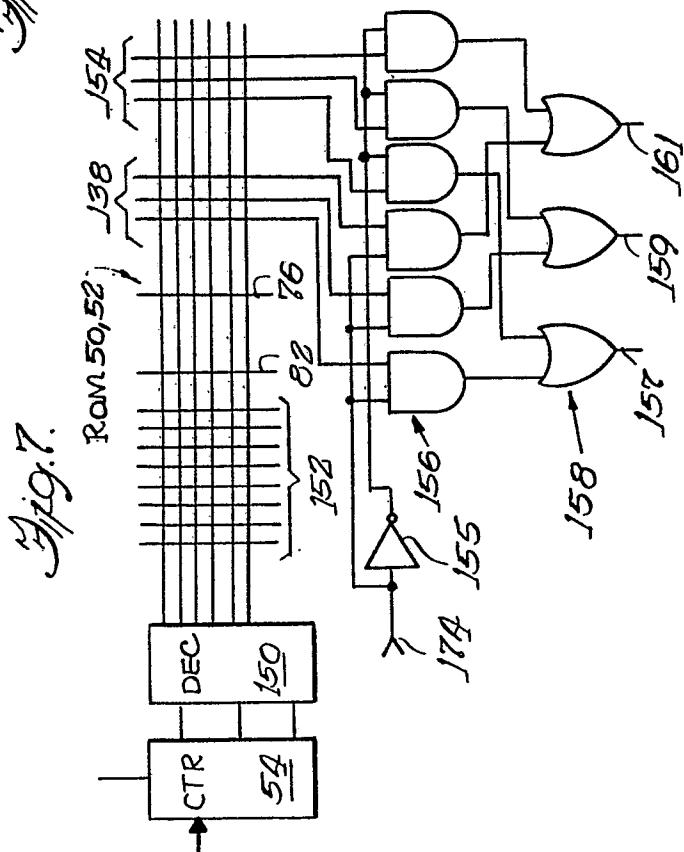
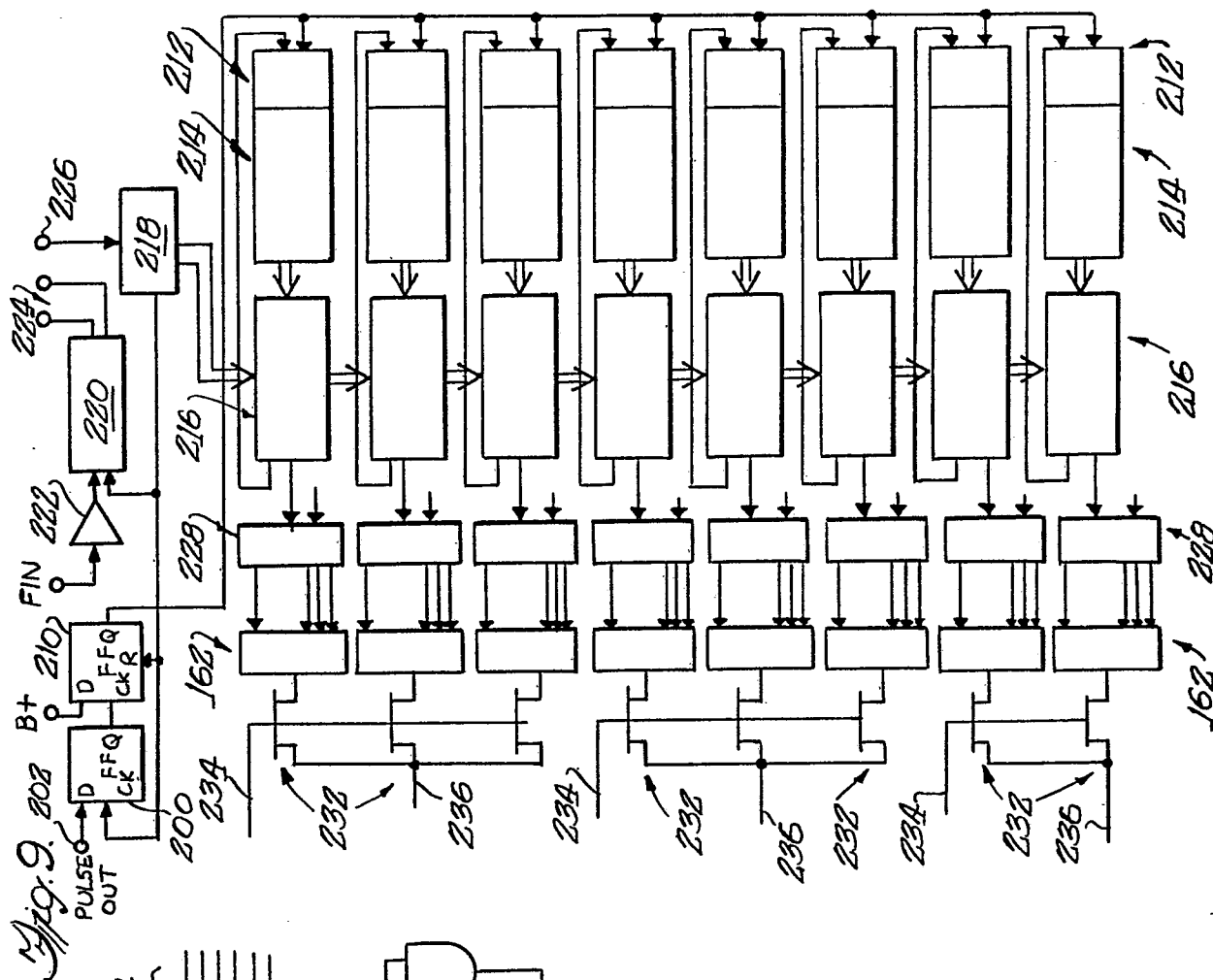


Fig. 5.







European Patent
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EUROPEAN SEARCH REPORT

0042019
Application number

EP 80 30 1980.1

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
	US - A - 4 137 810 (WHEELWRIGHT et al.) * fig. 5; column 6, lines 40 to 46; column 7, lines 23 to 33; fig. 6; column 7, lines 34 to 59; fig. 3;	1,2	G 10 H 7/00
	fig. 6; column 7, lines 47 to 59;	4	G 10 H 5/06
	fig. 2, 5 and 6 *	5	G 10 H 1/06
	--	9,10	
	GB - A - 2 013 945 (WURLITZER CO.) * abstract; fig. 2; fig. 3, position 40; page 2, lines 13 to 21; fig. 3, fig. 3 *	1,2	TECHNICAL FIELDS SEARCHED (Int. Cl. ³)
	--	4,9,10	
		5	
A	DE - A - 2 029 582 (LICENTIA) * claims 1, 2, 5; fig. 1, 3; page 6, line 33 to page 7, line 3 *		G 10 H 1/00
	--		G 10 H 5/00
			G 10 H 7/00
A	US - A - 4 055 103 (MACHANIAN) -----		
			CATEGORY OF CITED DOCUMENTS
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			&: member of the same patent family, corresponding document
X The present search report has been drawn up for all claims Place of search Berlin Date of completion of the search 20-02-1981 Examiner ARENDET			