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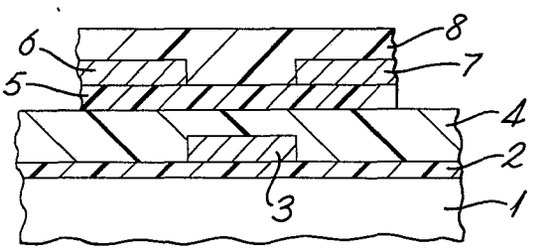
(54) **Annealing process for a thin-film semiconductor device.**

(57) A thin film semiconductor device, for example a transistor, is fabricated by depositing layers of materials of appropriate electrical characteristics on an insulating substrate (1). To manufacture a transistor, firstly an insulating base layer (2) is applied which is then followed by a gate electrode (3), an insulation layer (4) and a semiconductor layer (5). Source and drain electrodes (6) and (7) are then applied and finally a protective layer (8) encapsulates the device. In order to improve the life of the device it is annealed firstly in a reducing atmosphere and then in an oxidising atmosphere.



EP 0 051 940 A1

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METHODS OF MANUFACTURING SEMICONDUCTOR DEVICES

This invention relates to methods of manufacturing semiconductor devices. It has application in the manufacture of thin film transistors as well as other semiconductor devices.

A thin film transistor (or TFT) is a thin equivalent of a MOSFET (a metal-oxide-silicon field-effect transistor). It is a high input impedance non-linear device which is useful in switching applications. As with conventional field-effect transistors it has source, drain and gate electrodes. For an n-type enhancement device with a positive voltage applied to the gate there is a low impedance between the source and drain (the 'on' state). With the gate voltage zero there is a high impedance between the source and drain.

It has been suggested that such a device would be useful to switch flat panel matrix displays where each crossover point of the matrix constitutes a picture point in the display. Such displays may employ liquid crystal, electroluminescent, or electrochromic elements. These various types of display would be more effective if a TFT were to be associated with each picture point as an active switch device for the element. Since the area of deposition is only limited by masking, an array of TFTs can be provided over the same dimensions as a display panel and can be integrated with the panel.

For use as a switch in a matrix display a TFT should be stable when operated over long periods of time, should have a sufficiently low impedance when turned 'on' to allow charging of each picture point during the permitted address time, should have a sufficiently high impedance in the 'off' state to prevent decay of the charge to each picture point before the same element is readdressed, and should have a sufficiently large ratio of 'on' current to 'off' current. The problems associated with stability are firstly that there is a slow logarithmic decay of drain current when the device is operated under steady gate bias and secondly there is an ill-defined irreversible decay caused by the atmosphere

or by the overlaying layers of the picture elements. In practice the required value of 'on' currents can be readily obtained but it is difficult to achieve a sufficiently low value of 'off' current.

It is an object of the present invention to provide a semiconductor device which is adequately stable and has a low value of 'off' current.

According to the invention a method of fabricating a thin film semiconductor device comprises the steps of depositing layers of materials of appropriate electrical characteristics on an insulating substrate to form such a device, said layers including a semiconductor layer and an insulating layer protecting the semiconductor layer, and annealing the device so formed in an oxidising atmosphere.

Preferably the annealing is carried out firstly in a reducing atmosphere and then in the oxidising atmosphere.

In carrying out the invention the protective insulating layer should have low electrical loss and not be porous and it should not react with the semiconductor layer in a manner which would degrade the required electrical properties. A suitable material for such an insulating layer is silica.

In order that the invention may be more fully understood reference will now be made to the accompanying drawings in which Figure 1 and Figure 2 illustrate in cross-section alternative embodiments of TFTs manufactured in accordance with the invention.

Referring now to Figure 1 a TFT is fabricated by sequential deposition through metal stencil masks of appropriate materials. An insulating substrate 1 of any suitable material, for example aluminosilicate glass has deposited on it a base coat 2 of silica of thickness 100 nm by sputtering. This base coat 2 acts as a smoothing layer and prevents diffusion of contaminants from the substrate.

A gate electrode 3 formed of aluminium of thickness 50 nm is then evaporated through an appropriate mask. An insulator layer 4 of silica of thickness 100 nm is then sputtered followed by the evaporation of a semiconductor layer 5 of cadmium sulphide to a thickness of 40 nm. A source contact and a drain contact of chromium are then evaporated onto the surface of the semiconductor layer 5 through metal masks to a thickness of 50 nm and are backed up by evaporating aluminium layers of 120 nm thickness to form source electrode 6 and drain electrode 7. Finally a silica layer 8 of encapsulant is then sputtered over the top surface of the device to a thickness of 100 nm.

The sputtering operations are carried out by rf sputtering in a 95% argon-5% oxygen mixture and the evaporation operations are carried out by resistive heating.

Figure 2 shows an alternative construction of a TFT having a substrate 1 and base coat 2 similar to the substrate and base coat of Figure 1. In the construction of Figure 2 a source electrode 16 and a drain electrode 17 are deposited directly on base coat 2 and a semiconductor layer 15 is deposited between these electrodes. The source and drain electrodes and the semiconductor layer are then covered by an insulating layer 14 of silica which is deposited by sputtering. Finally a gate electrode 13 is deposited on to the surface of semiconductor layer 15 through metal masks.

In the construction of Figure 2 it will be seen that insulating layer 14 acts to protect semiconductor layer 15 in a similar manner to the encapsulant layer 8 in the construction of Figure 1.

While only one TFT is shown in both Figure 1 and Figure 2 it will be appreciated that any number of TFTs can be fabricated simultaneously to cover an area corresponding to a display panel.

The fabricated device or array of devices is then subject to an annealing process. In this process the array is annealed for one hour in a reducing atmosphere. Such an atmosphere may comprise a mixture of hydrogen and an inert gas. The purpose of

the inert gas is to reduce the concentration of hydrogen to below an explosive level. A suitable mixture is 10% hydrogen and 90% nitrogen and the annealing takes place at a temperature of 380°C. This annealing step is then followed by a second annealing step in which the array is annealed for three hours in an atmosphere of pure oxygen at 380°C.

The thicknesses of the layers quoted above are by way of example only and may be varied as considered suitable. The annealing times can be varied depending on the thickness of the semiconducting and encapsulating layer and for thicker layers a longer time is required. The time of anneal can be shortened by raising the temperature.

It is believed that the effect of the initial annealing in a reducing atmosphere is to remove damage caused by the sputtering process and promote diffusion. The effect of the subsequent annealing in an oxidising atmosphere is to reduce the carrier concentration of the semiconductor layer. It may be possible in certain circumstances to dispense with the initial step of annealing in a reducing atmosphere and rely on the annealing in an oxidising atmosphere. In such cases it may be desirable to increase the annealing time to in excess of 9 hours.

TFTs made in accordance with the above steps have been shown to have decay rates of less than 2.5% per decade corresponding to a 20% change in drain current in six years of continuous operation. Furthermore in accelerated ageing tests the on:off ratio of currents remains substantially constant at about 10^6 with 'off' currents of less than 6×10^{-11} amps.

The method described above can be used for TFTs prepared through stencil masks or by photolithography and etching and applies to all structural configurations. Thus for example in the method described with reference to Figure 1 the metal layers 6 and 7 may be deposited before the semiconductor layer 5. In the method described with reference to Figure 2 semiconductor layer 15 may be deposited before metal layers 16 and 17.

The method can be applied to matrix addressed displays using for example liquid crystal, electroluminescent and electrochromic materials and for electrophoretic and vacuum fluorescent displays.

The method is applicable to other insulators or encapsulants in addition to the silicon dioxide described above. Metals other than aluminium can be used for the gate electrode and the source and drain electrodes can be formed of metals other than chromium and aluminium. The anneal process can be used for insulators or encapsulants deposited by techniques other than sputtering, e.g. electron beam evaporation. The method described above is applicable to other thin film active devices, for example to solar cells.

CLAIMS

1. A method of fabricating a thin film semiconductor device comprising the steps of depositing layers of materials of appropriate electrical characteristics on an insulating substrate to form such a device, said layers including a semiconductor layer and an insulating layer protecting the semiconductor layer, characterised in that the device so formed is annealed in an oxidising atmosphere.

2. The method according to Claim 1 characterised in that the annealing is carried out firstly in a reducing atmosphere and then in an oxidising atmosphere.

3. The method according to Claim 2 characterised in that the reducing atmosphere comprises a mixture of hydrogen and an inert gas.

4. The method according to Claim 2 or Claim 3 characterised in that the reducing atmosphere comprises a mixture of 10% hydrogen and 90% nitrogen.

5. The method according to any one of Claims 2 to 4 characterised in that annealing in a reducing atmosphere takes place at approximately 380^{o}C.

6. The method according to any one of the preceding claims characterised in that the oxidising atmosphere comprises substantially pure oxygen.

7. The method according to any one of the preceding claims characterised in that annealing in the oxidising atmosphere is carried out at a temperature of approximately 380^{o}C.

8. The method according to any one of the preceding claims characterised in that the insulating layer comprises silica.

9. A thin film semiconductor device characterised in that it is fabricated in accordance with the method as claimed in any one of the preceding claims.

10. An array of thin film semiconductor devices characterised in that they are all fabricated on a common substrate in accordance with the method of any one of preceding Claims 1 to 8.

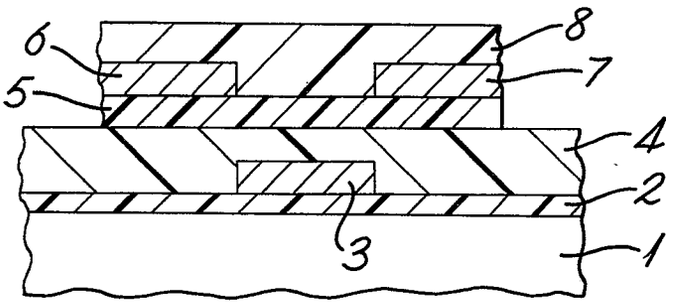

Fig. 1

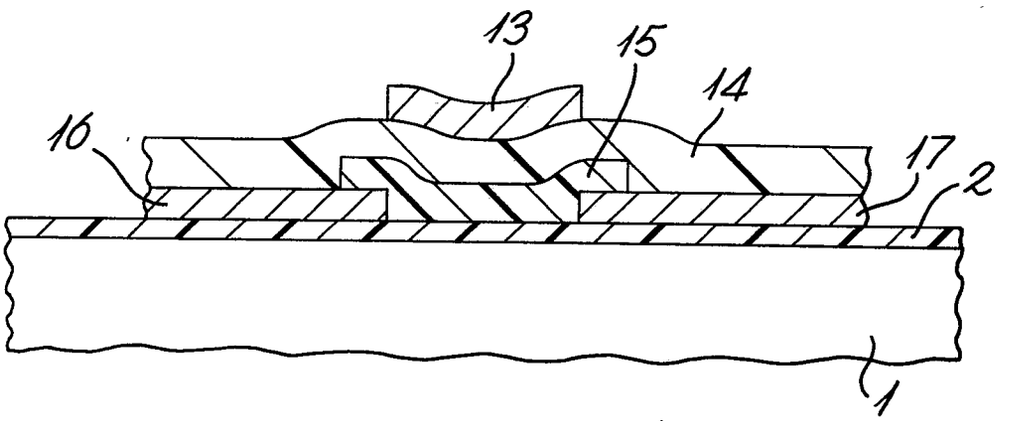

Fig. 2

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EUROPEAN SEARCH REPORT

0051940
Application number

EP 81 30 4945.9

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim
Y	IBM TECHNICAL DISCLOSURE BULLETIN, Vol. 22, No. 1, June 1979 New York P. BURR et al. "Single Step Anneal for Thin Film Transistors" page 353 --	1,7
Y	GB - A - 1 250 509 (PHILIPS) * claims 29, 33; page 10, example IV; page 17, line 114 to page 18, line 60 * --	1,6,8
Y	DE - B2 - 1 923 265 (LICENTIA PATENT-VERWALTUNGS-GMBH) * claim 1 * --	1,6
A	US - A - 3 885 993 (TIHANYI) * claims 1, 2; column 2, lines 16 to 41 * --	2,5
A	FR - A1 - 2 382 097 (RTC LA RADIOTECHNIQUE-COMPELEC) * claims 3, 4 * --	3,4
A	US - A - 4 091 527 (GOODMAN et al.) * claims 5, 8; column 5, line 17 to column 6, line 30 * ----	10

CLASSIFICATION OF THE APPLICATION (Int. Cl. 3)

H 01 L 21/324

TECHNICAL FIELDS SEARCHED (Int.Cl. 3)

H 01 L 21/31
H 01 L 21/324
H 01 L 21/84
H 01 L 29/78

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
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A: technological background
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P: intermediate document
T: theory or principle underlying the invention
E: earlier patent document, but published on, or after the filing date
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L: document cited for other reasons

&: member of the same patent family, corresponding document

X The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Berlin	28-01-1982	GIBBS

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