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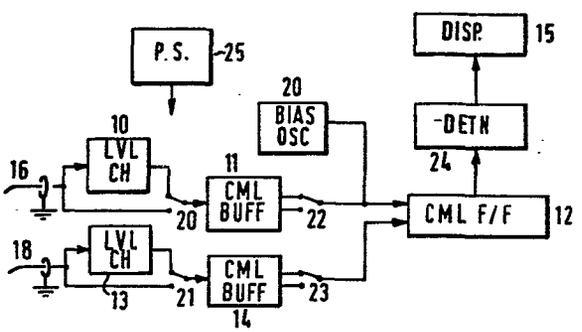
(54) **Test apparatus for signal timing measurement.**

(57) Test apparatus enables the relative timing of two signals picked up by probes 16, 18 to be determined. The two signals are fed, via switchable polarity and level changing circuitry 10, 11, 13,14 to a simple flip-flop 12, which comprises two cross-coupled transistors plus two input transistors. With both inputs at 0, the flip-flop is in an abnormal state with both cross-coupled flip-flops in the same state. The first input signal to go to 1 causes the flip-flop to enter a corresponding one of its two normal states (the cross-coupled flip-flops in opposite states). Detection circuitry 24 and display means 15 signal this state.

A low frequency bias oscillator 20 shifts the sloping transitions of one signal up and down relative to the other, changing their relative timing. For a part of each slow cycle dependent on the relative timings of the two signals, their effective timings at the flip-flop will be reversed. Hence the mean output from 24 will be dependent on the time difference between the two signals.



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TEST APPARATUS FOR SIGNAL TIMING MEASUREMENT

The present invention relates to test apparatus for measuring the time difference between two signals, paticularly signals which are cycled repeatedly.

Such apparatus is frequently required in the development and monitoring of digital electronic circuitry. The primary need is often merely to determine which of two signals is the first to undergo a transition, but it is often desirable also to be able to measure the time interval between the two signals.

A variety of techniques are known for achieving this. For example, a clock oscillator and counter can be used, with gating circuitry which opens a gate to allow clock pulses into the counter when the first signal changes and closes the gate to freeze the count in the counter when the second signal changes. Another known technique is to use an oscilloscope, either a single trace oscilloscope with the trace triggered by one signal and showing the other, or a dual trace oscilloscope.

The known techniques generally involve a substantial amount of complex and expensive equipment. Also, when the time intervals to be measured are very small, in the subnanosecond range, some of the known techniques fail because they cannot cope with such speeds.

The object of the present invention is to provide test apparatus for measuring the time difference between two signals which is both simple and fast.

Accordingly the present invention provides test apparatus for determining the time interval betwwen two signals, characterized by a pair of probes for picking up the two signals, circuitry for adjusting the polarities of levels of the signals, a pair of cross-coupled transistors, forming a simple flip-flop, input circuitry to the flip-flop to apply the signals to the flip-flop so as to cause the flip-flop to change from an initial abnormal state with both transistors in the same state to a normal state with

the two transistors in opposite states, detection circuitry fed from the two transistors to determine the difference between their outputs, and display means fed by the detection circuitry.

Test apparatus embodying the invention will now be described, by way of example, with reference to the drawings in which:

Figure 1 is a block diagram of the apparatus;

Figure 2 is a circuit diagram of a flip-flop in the apparatus; and

Figures 3 to 5 are waveforms which illustrate the operation of the apparatus.

Figure 1 shows the main units of the test apparatus. Two probes 16 and 18 are attached to the two points at which the two signals, whose timings are to be compared, appear. Two switches 20 and 21 select the probe outputs either direct or via level changing circuits 10 and 13, which are TTL to CML level shifters. The switches 20 and 21 feed respective CML buffers 11 and 14, from which either the positive (direct) or negative (inverted, complemented) outputs can be selected by two more switches 22 and 23. The two switches 22 and 23 feed a CML flip-flop circuit 12, which is the key to the signal comparison process. This circuit 12 feeds a detection circuit 24, which in turn feeds a display unit 15 which displays an indication of the timing difference between the two signals.

A bias oscillator 20, which produces a sine wave output of frequency low compared to that of the signals being compared, is coupled to one input to the flip-flop 12. A power supply 25 provides power for the remainder of the circuitry. In some circumstances, the circuitry can obtain its power supplies from the computer being tested instead of having its own independent power supply 25.

Figure 2 shows the CML flip-flop 12 in detail. This comprises two transistors Q2 and Q3, cross-coupled and connected in series with two resistors R1 and R2 respectively

as shown, to form a bistable circuit, together with two input transistors Q1 and Q2 connected across Q2 and Q3 as shown. This circuit is a very simple and primitive form of flip-flop, without any of the elaboration of input circuitry and clocking which is normally included in flip-flops as understood nowadays. We will adopt the convention that logical 1 is high, logical 0 is low. The "normal" or quiescent state of the inputs to the flip-flop is both 0 (low). This means that Q1 and Q4 are both turned off. The flip-flop can be in either of its two "normal" states: either Q2 on and Q3 off, or Q2 off and Q3 on. A "normal" change of flip-flop state is accomplished by one or other, but not both, of the inputs going momentarily to 1. Say the input to Q1 goes briefly to 1. This turns on Q1, forcing the collector of Q1 and hence the base of Q3 low, and hence turning off Q3 and forcing the base of Q2 high, so turning on Q2. This forces the flip-flop to one of its two normal states, and it remains in that state when the input to Q1 goes back to 0.

However, if both inputs to the flip-flop go to 1 together, the flip-flop is forced into an abnormal state in which Q1 and Q4 are both on and the bases of Q2 and Q3 are both low. If now one or other of the two inputs should go to 0, say the input to Q1, the corresponding input transistor Q1 will turn off, and the flip-flop will change to a normal state in which one of the two transistors Q2 and Q3 (in fact, Q2) will go off and the other (here, Q3) will remain on. This state, of course, will persist if the other input then also goes to 0. Conversely, it is obvious that if both inputs are at 1 and the input to Q4 goes to 0, transistor Q3 will go off and Q2 will stay on, and this state will persist when, later, the input to Q1 also goes to 0.

This is illustrated in Figure 3, where signals Q1b and Q4b are the input signals applied to the bases of Q1 and Q4, and signals Q2c and Q3c are the signals appearing

at the collectors of Q2 and Q3. The input signals are both initially at 1; the full line graphs show what happens when the input to Q1 is the first to fall to 0, and the broken line graphs show what happens when the input to Q4 is the first to drop to 0.

The two inputs to the flip-flop are the two signals picked off by the probes 16 and 18. It is assumed that these two signals are both initially at 1, and it is required to determine which is the first to drop to 0. (If either or both is changing from 0 to 1, the CML buffers 11 and 14 can be used to invert them appropriately.) At time t0, when both have dropped to 0, the state of flip-flop 12 is dependent on which of the two signals was the first to change.

The detection circuit 24 is fed by the collectors of both transistors Q2 and Q3 of flip-flop 12 as shown, and forms the difference between the two voltages. This difference has a polarity dependent on the state of the flip-flop when the flip-flop is in either normal state, as indicated in Figure 3. Hence a positive voltage from circuit 24 indicates that the signal on probe 16 was the first to change, a negative voltage, that the signal on probe 18 was the first to change. The display device 15 indicates the sign of this voltage.

Of course, in a typical situation the system under test will be cycling, and the signals picked up by the probes will return to 1 at some time after t0, probably (but not necessarily) in the same sequence that they went to 0. The flip-flop 12 will then be forced back to the abnormal state, and will return to the normal state as soon as one or other of its input signal goes back to 0. Thus the output from the detection circuit 24 will probably be a pulse signal of one or other polarity.

This bias oscillator 20 provides a sinusoidal bias signal whose frequency is low compared to the cycle frequency of the system under test. This bias signal enables

the time interval between the changes of the two signals being picked up by probes 16 and 18 to be measured, instead of merely the sign of this time interval being determined, as has been described so far.

Considering the input voltages to the flip-flop 12 in more detail, these will in fact change between their 2 levels by sloping rather than vertical waveforms, and the point at which the transistors Q1 and Q4 change between on and off will be some critical voltage level Vc between the two logic levels. Hence the two input voltages V1 and V2 will be somewhat as shown in Figure 4, with the transistors Q1 and Q4 turning off as V1 and V2 cross the critical voltage Vc.

If a bias voltage Vb is added to voltage V1, this will move the waveform V1 vertically up or down, and will therefore change the point at which the combined voltage V1 + Vb crosses the critical voltage Vc. In particular, for a suitable value of Vb as shown in Figure 4, the combined voltage V1 + Vb can be made to cross Vc at the same instant as does V2. For other values of Vb, the crossing point for V1 + Vb will be before or after the crossing point for V2.

This means that if the slope of the singals is known (as will often be the case, since the slope will be determined by known circuit parameters), then the time difference between the two signals is equivalent to a voltage difference. It is therefore possible, by adjusting the bias voltage to the point where the flip-flop 12 takes up both states more or less equally often as the system under test cycles repeatedly, to measure the time difference between the two signals.

Preferably however a slow sine wave bias is used, as already stated. The effect of this is shown in Figure 5. The two signals V1 and V2 are shown cycling repeatedly. As the slow sine wave Vb carries the signal V1 up and down with respect to the critical voltage, so the instant at which the voltage V1 + Vb crosses the critical voltage will

move relative to the instant at which the signal V2 crosses Vc. At some point in the Vb cycle, these two instants will coincide. Up to that point, the output Q2c - Q3c of the flip-flop 12 will consist of a series of positive pulses, as the flip-flop is repeatedly set to the same state on each signal cycle. At this point, the flip-flop will be set to the other state, and its output will therefore be a series of pulses of the opposite polarity, until the bias voltage Vb drops back to the level where the change-over occurred.

The detection circuit 24 will therefore be fed with a signal somewhat as shown in Figure 5. It is evident that by smoothing this signal, a steady voltage can be obtained having a magnitude and polarity which indicate the magnitude and sign of the timing difference between the two signals V1 and V2.

It will be seen from Figure 3 that the length of the output pulse from the flip-flop 12 is the time during which either of the two input signals is at 0. Hence as the relative timing of the two input signals is changed by the bias signal, so the length of the output pulses from the flip-flop 12 will change, increasing somewhat as the timings of the two signals move apart.

CLAIMS

1. Test apparatus for determining the time interval between two signals, characterized by a pair of probes (16,18) for picking up the two signals, circuitry (10, 20,11,22,13,21,14,23) for adjusting the polarities and levels of the signals, a pair of cross-coupled transistors (Q2,Q3) forming a simple flip-flop (12), input circuitry (Q1,Q4) to the flip-flop (12) to apply the signals to the flip-flop so as to cause the flip-flop to change from an initial abnormal state with both transistors (Q2, Q3) in the same state to a normal state with the two transistors in opposite states, detection circuitry (24) fed from the two transistors to determine the difference between their outputs, and display means (15) fed by the detection circuitry (24).
2. Test apparatus according to Claim 1, characterized by bias means (20) for adding a variable bias to one of the signals.
3. Test apparatus according to Claim 2, characterized in that the bias means generate a sinusoidal signal of frequency much lower than the cycle frequency of the two signals.

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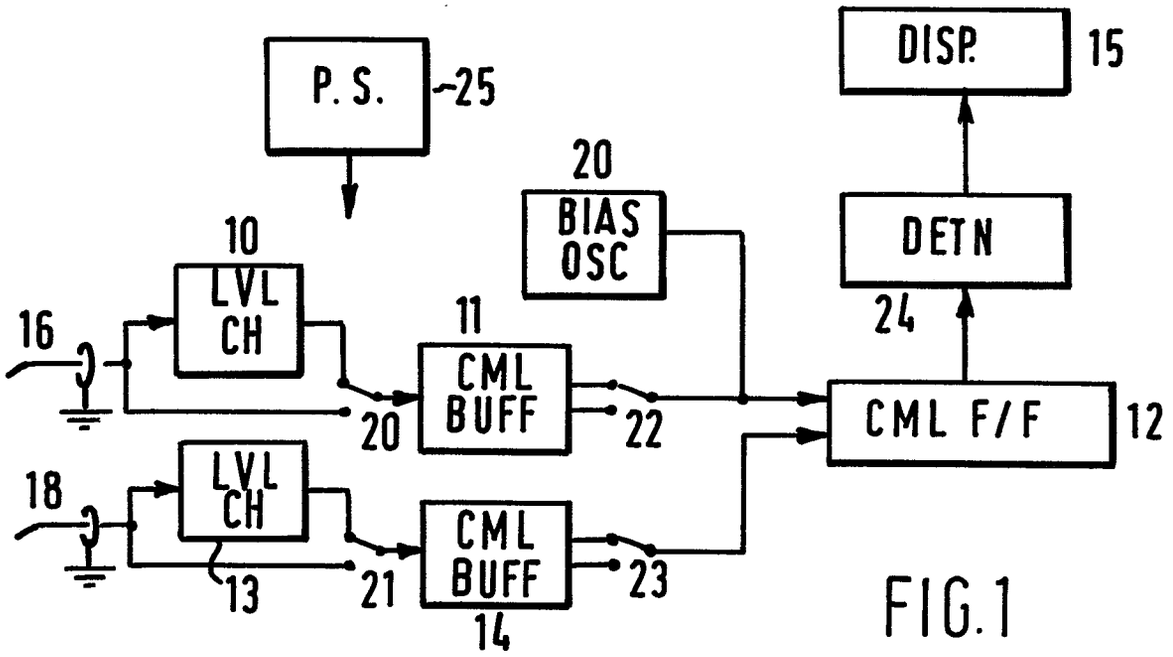

FIG.1

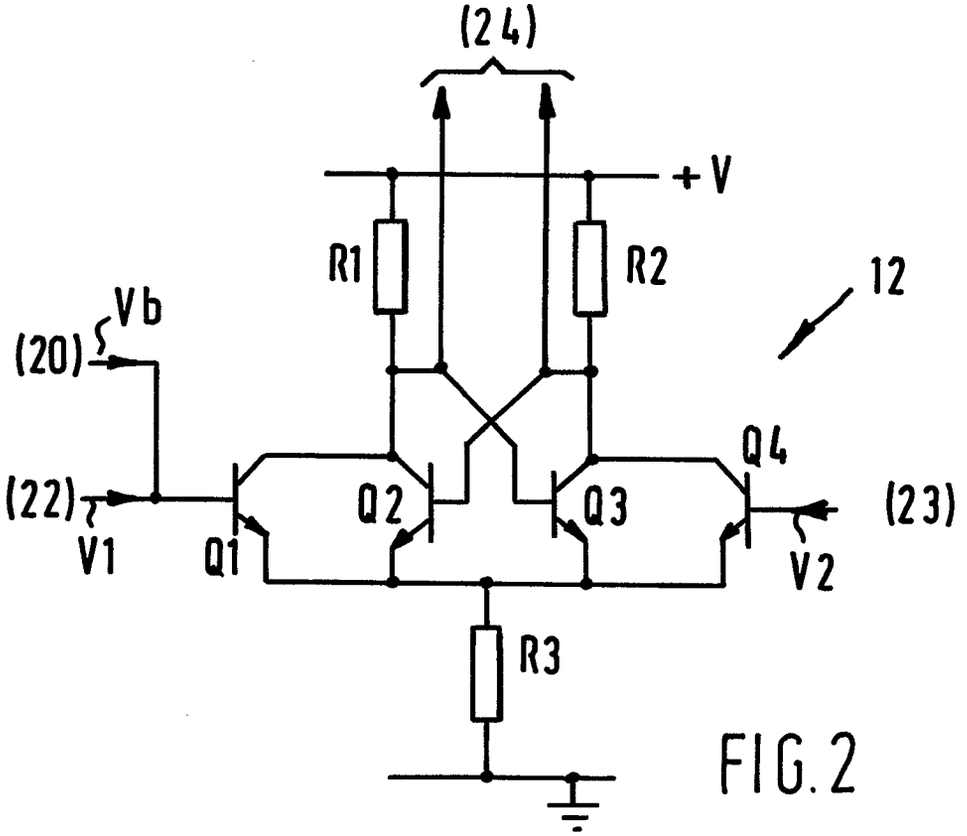

FIG.2

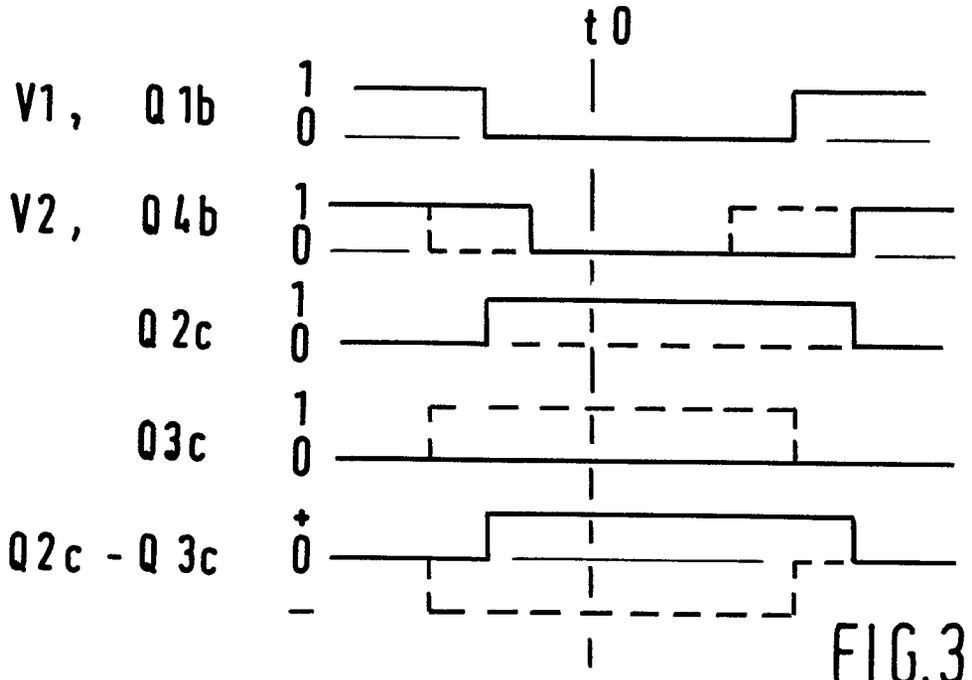

FIG.3

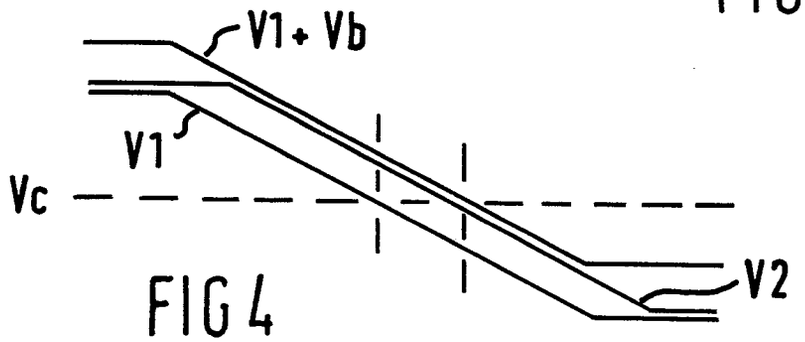

FIG 4

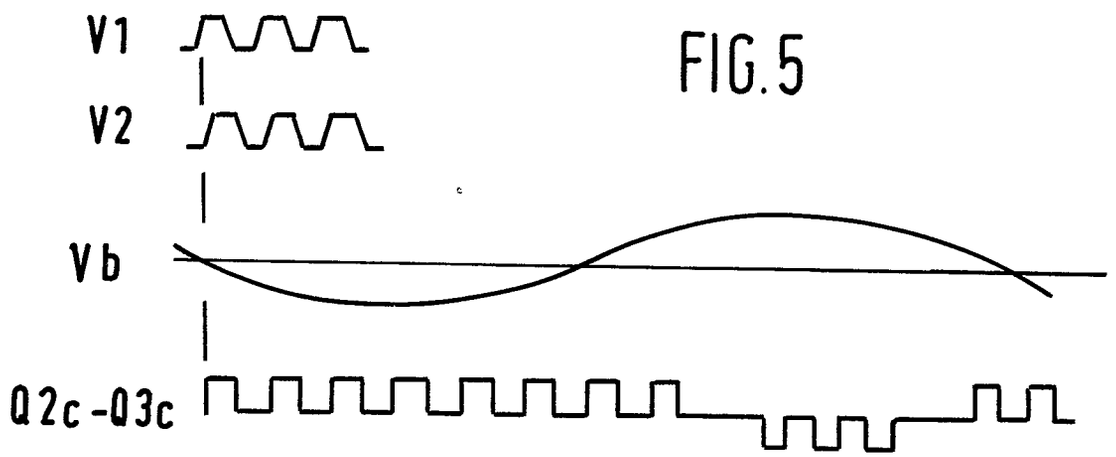

FIG.5

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EUROPEAN SEARCH REPORT

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Application number

EP 81 30 5596

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim
Y	US - A - 3 534 271 (LOEWER) * column 4, lines 4 to 47; figure *	1,2
Y	GB - A - 1 242 855 (HOURIE) * page 1, line 85 to page 3, line 17; figures 1-3 *	1
A	INSTRUMENTS AND EXPERIMENTAL TECHNIQUES, no.1, January/ February 1970, Plenum Publishing Corp. NEW YORK (US) S.S. KUZNETSKII et al.:"Phase-Metering Attachment for a Digital Frequency Meter" pages 156-159 * figures 1,3 *	1
A	US - A - 3 641 443 (ZERBY) * the whole document *	1
A	US - A - 2 962 609 (McDONALD) * the whole document *	2,3
A	US - A - 3 509 381 (MARSHALL et al.) * column 3, line 61 to column 4, line 35 *	1

CLASSIFICATION OF THE APPLICATION (Int. Cl. 3)

G 04 F 10/00
H 03 K 3/288

TECHNICAL FIELDS SEARCHED (Int.Cl. 3)

G 04 F 10/00
H 03 K 3/00

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
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E: earlier patent document, but published on, or after the filing date
D: document cited in the application
L: document cited for other reasons

&: member of the same patent family, corresponding document

X The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	10-03-1982	DEVINE

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