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(54) **Test apparatus for signal timing measurement.**

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Description

The present invention relates to test apparatus for measuring the time difference between two signals, particularly signals which are cycled repeatedly.

Such apparatus is frequently required in the development and monitoring of digital electronic circuitry. The primary need is often merely to determine which of two signals is the first to undergo a transition, but it is often desirable also to be able to measure the time interval between the two signals.

A variety of techniques are known for achieving this, however, they generally involve a substantial amount of complex and expensive equipment. Also, when the time intervals to be measured are very small, in the subnanosecond range, some of the known techniques fail because they cannot cope with such speeds.

From US patent 3,534,271 a circuit is known for measuring the time differential between two pulses employing a flip-flop circuit in conjunction with a transistor bi-switch. The flip-flop is set from the 0 state to the 1 state by one incoming signal and back to the 0 state by another incoming signal. The time which it spends in the 1 state is indicative for the time interval between the two signals. Correct measuring obviously depends on the second signal occurring after the first, and if the sequence of the two signals is not known, this system will require modification. In addition, the accuracy of this circuit is poor if the time interval to be measured is very short, because the second signal is then fed to the flip-flop before the flip-flop has completed its change of state and complicated dynamic interactions will then occur.

From GB patent 1,242,855 a bi-stable trigger circuit is known employing a flip-flop to determine the polarity of an input signal which is applied between the two input points of the flip-flop, the flip-flop being constructed so that it is balanced and having its power supply turned on for the measurement, the flip-flop thereby taking up one or other state in dependence on the input difference as it becomes bistable as a result of the power supply rising.

From US patent 3,641,443 a frequency compensated pulse time discriminator is known to measure the time or phase difference between pulses in two trains of pulses by the use of flip-flop and NAND components. In this system the circuitry is duplicated to allow detection of both possible orders of input, $t1 - t2$ and $t2 - t1$. This makes the system unduly complex.

The object of the present invention is to provide test apparatus for measuring the time difference between two signals which is both simple and fast.

Accordingly, the present invention provides test apparatus for determining the time relationship between two signals, and comprises a pair of probes for picking up the two signals, circuitry for adjusting the polarities and levels of the signals, a cross-coupled transistor pair forming a flip-flop, detection circuitry connected to said flip-flop to determine the difference between the outputs of its two transistors, and display means fed by said detection circuitry and input circuitry to the flip-flop. The apparatus is characterized by said input circuitry comprising two transistors, each with its emitter-collector path connected in parallel with the emitter-collector path of a respective one of the two cross-coupled transistors of the flip-flop, to apply the signals to the cross-coupled transistor pair so as to cause the cross-coupled pair to change from an initial state with both transistors in the same, i.e. abnormal, state to a state with the two transistors in opposite, i.e. normal, state.

Furthermore, it is advantageous to provide bias means for adding a variable bias to one of the signals, preferably, said bias means to generate a sinusoidal signal of a frequency much lower than the cycle frequency of the two signals.

A circuit is known from US patent 2,962,609 to generate a pulse train in which the repetition rate and duty cycle of the pulses can be varied infinitely and independently of each other even though the switches which generate the pulse have finite operate and release times. While this circuit may be of interest as technological background with respect to the generation of the variable bias mentioned above, it is less relevant to the main object of this invention, i.e. test apparatus for measuring time difference between signals, because it is concerned with the opposite problem to the subject apparatus, i.e. generating signals of known time spacing.

Test apparatus embodying the invention will now be described, by way of example, with reference to the drawings in which:

Figure 1 is a block diagram of the test apparatus;

Figure 2 is a circuit diagram of a flip-flop in the test apparatus embodying the inventive input circuitry to the flip-flop transistors; and

Figures 3 to 5 are waveforms which illustrate the operation of the test apparatus.

Figure 1 shows the main units of the test apparatus. Two probes 16 and 18 are attached to the two points at which the two signals, whose timings are to be compared, appear. Two switches 20 and 21 select the probe outputs either direct or via level changing circuits 10 and 13, which are TTL to CML level shifters. The switches 20 and 21 feed respective CML buffers 11 and 14, from which either the positive (direct) or negative (inverted, complemented) outputs can be selected by two more switches 22 and 23. The two switches 22 and 23 feed a CML flip-flop circuit 12, which is the key to the signal comparison process. This circuit 12 feeds a detection circuit 24, which in turn feeds a display unit 15 which displays an indication of the timing difference between the two signals.

A bias oscillator 20, which produces a sine wave output of frequency low compared to that of the signals being compared, is coupled to one input to the flip-flop 12. A power supply 25 provides power for the remainder of the circuitry.

In some circumstances, the circuitry can obtain its power supplies from the computer being tested instead of having its own independent power supply 25.

Figure 2 shows the CML flip-flop 12 in detail. This comprises two transistors Q2 and Q3, cross-coupled and connected in series with two resistors R1 and R2 respectively as shown, to form a bistable circuit, together with two input transistors Q1 and Q2 connected across Q2 and Q3 as shown. This circuit is a very simple and primitive form of flip-flop, without any of the elaboration of input circuitry and clocking which is normally included in flip-flops as understood nowadays. We will adopt the convention that logical 1 is high, logical 0 is low. The "normal" or quiescent state of the inputs to the flip-flop is both 0 (low). This means that Q1 and Q4 are both turned off. The flip-flop can be either of its two "normal" states: either Q2 on and Q3 off, or Q2 off and Q3 on. A "normal" change of flip-flop state is accomplished by one or other, but not both, of the inputs going momentarily to 1. Say the input to Q1 goes briefly to 1. This turns on Q1, forcing the collector of Q1 and hence the base of Q3 low, and hence turning off Q3 and forcing the base of Q2 high, so turning on Q2. This forces the flip-flop to one of its two normal states, and it remains in that state when the input to Q1 goes back to 0.

However, if both inputs to the flip-flop go to 1 together, the flip-flop is forced into an abnormal state in which Q1 and Q4 are both on and the bases of Q2 and Q3 are both low. If now one or two other of the two inputs should go to 0, say the input to Q1, the corresponding input transistor Q1 will turn off, and the flip-flop will change to a normal state in which one of the two transistors Q2 and Q3 (in fact, Q2) will go off and the other (here, Q3) will remain on. This state, of course, will persist if the other input then also goes to 0. Conversely, it is obvious that if both inputs are at 1 and the input to Q4 goes to 0, transistor Q3 will go off and Q2 will stay on, and this state will persist when, later, the input to Q1 also goes to 0.

This is illustrated in Figure 3, where signals Q1b and Q4b are the input signals applied to the bases of Q1 and Q4, and signals Q2c and Q3c are the signals appearing at the collectors of Q2 and Q3. The input signals are both initially at 1; the full line graphs show what happens when the input to Q1 is the first to fall to 0, and the broken line graphs show what happens when the input to Q4 is the first to drop to 0.

The two inputs to the flip-flop are the two signals picked off by the probes 16 and 18. It is assumed that these two signals are both initially at 1, and it is required to determine which is the first to drop to 0. (If either or both is changing from 0 to 1, the CML buffers 11 and 14 can be used to invert them appropriately.) At time t0, when both have dropped to 0, the state of flip-flop 12 is dependent on which of the two signals was the first to change.

The detection circuit 24 is fed by the collectors of both transistors Q2 and Q3 of flip-flop 12 as shown, and forms the difference between the two voltages. This difference has a polarity dependent on the state of the flip-flop when the flip-flop is in either normal state, as indicated in Figure 3. Hence a positive voltage from circuit 24 indicates that the signal on probe 16 was the first to change, a negative voltage, that the signal on probe 18 was the first to change. The display device 15 indicates the sign of this voltage.

Of course, in a typical situation the system under test will be cycling, and the signals picked up by the probes will return to 1 at some time after t0, probably (but not necessarily) in the same sequence that they went to 0. The flip-flop 12 will then be forced back to the abnormal state, and will return to the normal state as soon as one or other of its input signal goes back to 0. Thus the output from the detection circuit 24 will probably be a pulse signal of one or other polarity.

This bias oscillator 20 provides a sinusoidal bias signal whose frequency is low compared to the cycle frequency of the system under test. This bias signal enables the time interval between the changes of the two signals being picked up by probes 16 and 18 to be measured, instead of merely the sign of this time interval being determined, as has been described so far.

Considering the input voltages to the flip-flop 12 in more detail, these will in fact change between their 2 levels by sloping rather than vertical waveforms, and the point at which the transistors Q1 and Q4 change between on and off will be some critical voltage level Vc between the two logic levels. Hence the two input voltages V1 and V2 will be somewhat as shown in Figure 4, with the transistors Q1 and Q4 turning off as V1 and V2 cross the critical voltage Vc.

If a bias voltage Vb is added to voltage V1, this will move the waveform V1 vertically up or down, and will therefore change the point at which the combined voltage V1 + Vb crosses the critical voltage Vc. In particular, for a suitable value of Vb as shown in Figure 4, the combined voltage V1 + Vb can be made to cross Vc at the same instant as does V2. For other values of Vb, the crossing point for V1 + Vb will be before or after the crossing point for V2.

This means that if the slope of the signals is known (as will often be the case, since the slope will be determined by known circuit parameters), then the time difference between the two signals is equivalent to a voltage difference. It is therefore possible, by adjusting the bias voltage to the point where the flip-flop 12 takes up both states more or less equally often as the system under test cycles repeatedly, to measure the time difference between the two signals.

Preferably however a slow sine wave bias is used, as already stated. The effect of this is shown in Figure 5. The two signals V1 and V2 are shown cycling repeatedly. As the slow sine wave Vb carries the signal V1 up and down with respect to the critical voltage, so the instant at which the voltage V1 + Vb crosses the critical voltage will move relative to the instant at which the signal V2

crosses Vc. At some point in the Vb cycle, these two instants will coincide. Up to that point, the output Q2c – Q3c of the flip-flop 12 will consist of a series of positive pulses, as the flip-flop is repeatedly set to the same state on each signal cycle. At this point, the flip-flop will be set to the other state, and its output will therefore be a series of pulses of the opposite polarity, until the bias voltage Vb drops back to the level where the change-over occurred.

The detection circuit 24 will therefore be fed with a signal somewhat as shown in Figure 5. It is evident that by smoothing this signal, a steady voltage can be obtained having a magnitude and polarity which indicate the magnitude and sign of the timing difference between the two signals V1 and V2.

It will be seen from Figure 3 that the length of the output pulse from the flip-flop 12 is the time during which either of the two input signals is at 0. Hence as the relative timing of the two input signals is changed by the bias signal, so the length of the output pulses from the flip-flop 12 will change, increasing somewhat as the timings of the two signals move apart.

Claims

1. Test apparatus for determining the time relationship between two signals, comprising a pair of probes (16, 18) for picking up the two signals, circuitry for adjusting the polarities and levels of the signals (10, 20, 11, 22; 13, 21, 14, 23), a cross-coupled transistor pair forming a flip-flop (12; Q2, Q3), detection circuitry (24) connected to said flip-flop (12) to determine the difference between the outputs of its two transistors, display means (15) fed by said detection circuitry (24), and input circuitry to the flip-flop (12), characterized by said input circuitry comprising two transistors (Q1, Q4), each with its emitter-collector path connected in parallel with the emitter-collector path of a respective one of the two cross-coupled transistors (Q2, Q3) of the flip-flop (12), to apply the signals to the cross-coupled transistor pair so as to cause the cross-coupled pair to change from an initial state with both transistors (Q2, Q3) in the same, i.e. abnormal, state to a state with the two transistors in opposite, i.e. normal, state.

2. Test apparatus according to claim 1, characterized by bias means (20) for adding a variable bias to one of the signals.

3. Test apparatus according to claim 2, characterized in that said bias means generate a sinusoidal signal of a frequency much lower than the cycle frequency of the two signals.

Patentansprüche

1. Testapparat zur Bestimmung des Zeitverhältnisses zwischen zwei Signalen, aufweisend

ein Paar von Sonden (16, 18) zur Aufnahme der beiden Signale, eine Schaltung zur Einstellung bzw. Justierung der Polaritäten und der Niveaus der Signale (10, 20, 11, 22; 13, 21, 14, 23),

ein kreuz-gekoppeltes Transistorpaar, das einen Flip-Flop (12; Q2, Q3) bildet,

eine Detektorschaltung (24), die mit dem Flip-Flop (12) verbunden ist, um die Differenz zwischen den Ausgängen ihrer zwei Transistoren zu bestimmen,

eine Anzeigeeinrichtung (15), die durch die Detektorschaltung (24) gespeist wird, und

eine Eingangsschaltung zum Flip-Flop (12), dadurch gekennzeichnet, daß die Eingangsschaltung zwei Transistoren (Q1, Q4) umfaßt, deren Emitter-Kollektor-Weg jeweils parallel mit dem Emitter-Kollektor-Weg jeweils eines entsprechenden von zwei kreuz-gekoppelten Transistoren (Q2, Q3) des Flip-Flops (12) verbunden ist, um die Signale an das kreuz-gekoppelte Transistorpaar derart anzulegen, daß das kreuz-gekoppelte Paar dazu veranlaßt wird, von einem Initialzustand, wobei beide Transistoren (Q2, Q3) im gleichen, das heißt abnormalen Zustand sind, in einen Zustand hin zu verändern, wobei die beiden Transistoren im entgegengesetzten, das heißt normalen Zustand sind.

2. Testapparat nach Anspruch 1, gekennzeichnet durch Vorspannungseinrichtungen (20), um einem der Signale eine variable Spannung hinzufügen.

3. Testapparat nach Anspruch 2, dadurch gekennzeichnet, daß die Vorspannungseinrichtungen ein Sinussignal erzeugen, dessen Frequenz viel kleiner ist, als die Zyklusfrequenz der beiden Signale.

Revendications

1. Appareil de test pour déterminer la relation dans le temps entre deux signaux, comprenant une paire de sondes (16, 18) pour capter les deux signaux, un circuit pour régler les polarités et les niveaux des signaux (10, 20, 11, 22; 13, 21, 14, 23), une paire de transistors à couplage croisé constituant une bascule (12; Q2, Q3), un circuit de détection (24) connecté à la bascule (12) pour déterminer la différence entre les signaux de sortie de ses deux transistors, un moyen de visualisation (15) alimenté par le circuit de détection (24), et un circuit d'entrée de la bascule (12), caractérisé en ce que le circuit d'entrée comprend deux transistors (Q1, Q4) dont la voie émetteur-collecteur de chacun est connectée en parallèle avec la voie émetteur-collecteur d'un transistor respectif des deux transistors à couplage croisé (Q2, Q3) de la bascule (12), pour appliquer les signaux à la paire de transistors à couplage croisé de manière à ce que la paire à couplage croisé passe d'un état initial où le deux transistors (Q2, Q3) sont dans le même état, c'est-à-dire un état anormal, à un état où les deux transistors sont dans un état opposé, c'est-à-dire un état normal.

2. Appareil de test selon la revendication 1, caractérisé par un moyen de polarisation (20) servant à ajouter une polarisation variable à un des signaux.

3. Appareil de test selon la revendication 2, caractérisé en ce que le moyen de polarisation engendre un signal sinusoïdal d'une fréquence bien inférieure à la fréquence cyclique des deux signaux.

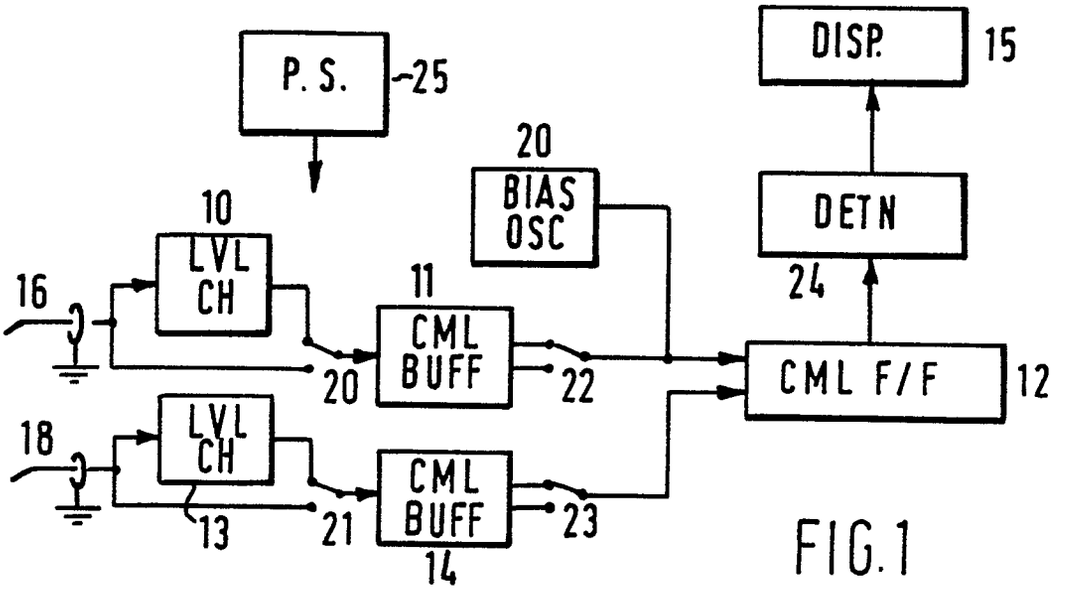
P. S.
25
DISP.
15
20
BIAS OSC
10
LVL CH
DETN
24
16
11
CML BUFF
CML F/F
12
20
22
18
LVL CH
CML BUFF
13
21
23
14

FIG.1

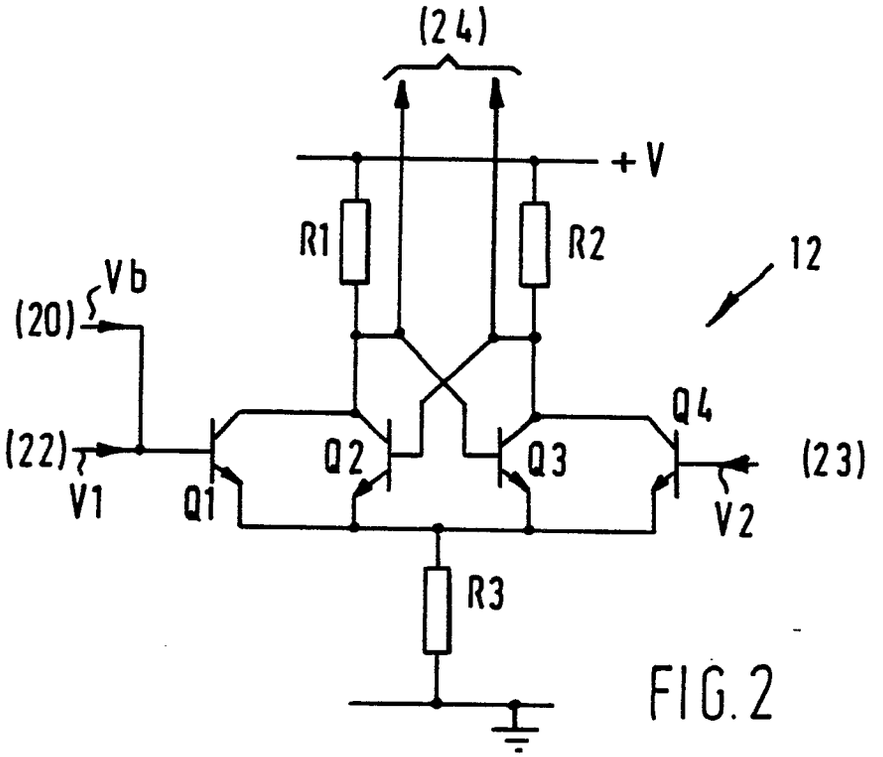
(24)
+V
R1
R2
12
Vb
(20)
Q4
(22)
Q2
Q3
(23)
V1
Q1
V2
R3

FIG.2

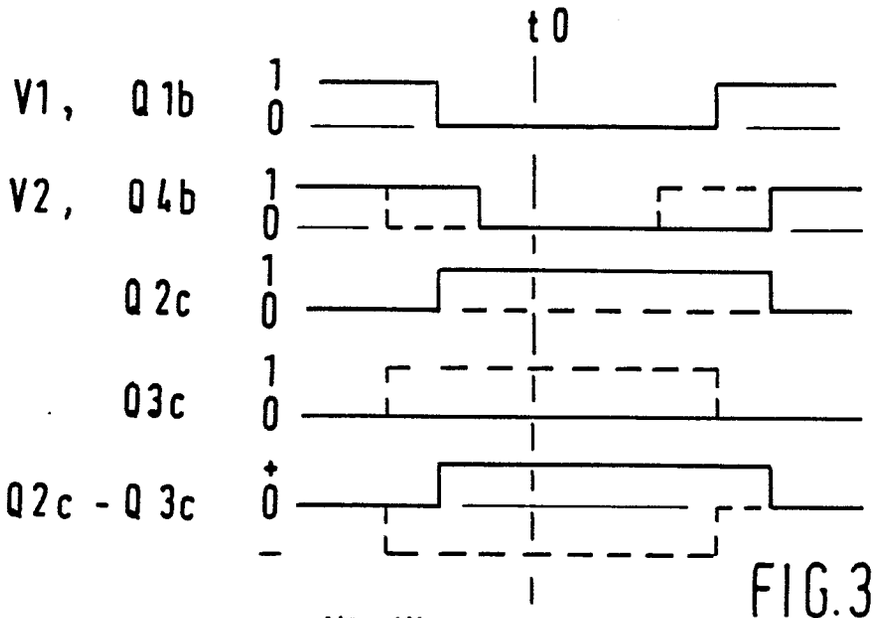

FIG.3

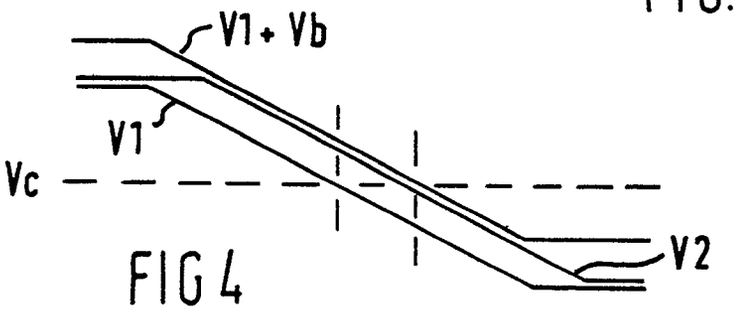

FIG 4

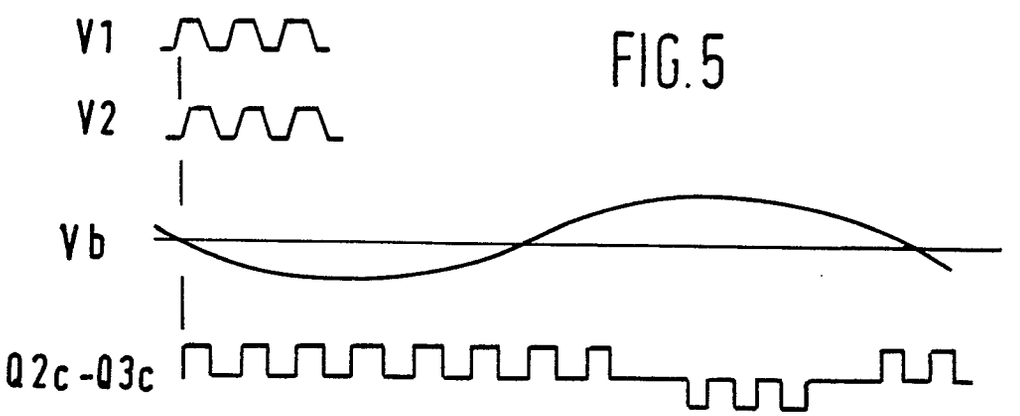

FIG.5