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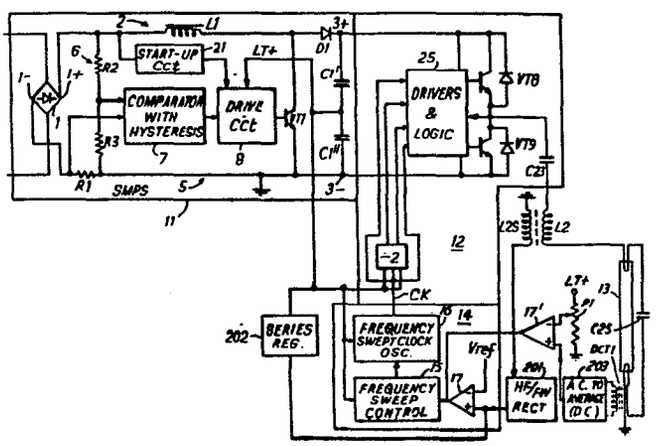
(54) **Lamp driver circuits.**

(57) The invention provides a lamp driver circuit for discharge lamps, in particular fluorescent lamps. An inverter (12) receiving DC provides a high frequency AC output. A resonant circuit includes a capacitor (C25) connected across the lamp (13) and a ballast inductor (L2) in series with them. A control arrangement (15, 16) causes the inverter (12) to operate at a frequency above the resonant frequency of the lamp when initially switched on. It is then caused to sweep down in frequency towards the resonance frequency so that the lamp strikes as a result of the magnified voltage applied to it. After the lamp has struck the frequency drops to a suitable running frequency. If the lamp strikes a circuit (L25, 201, 17) controls the frequency to limit the lamp voltage. Another circuit (DCT1, 203, P1, 17′) controls the lamp frequency for dimming purposes. The circuit when operative at the initial higher frequency provides heating current through the filament before the lamp strikes since the capacitor (C25) shunts the lamp at such frequency.



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Lamp Driver Circuits

The present invention relates to circuits for activating discharge lamps and in particular circuits for activating fluorescent lamps.

To avoid cold-striking such a lamp, the lamp cathode must be heated to emission before a high voltage is applied to strike the arc.

In 50Hz circuits this has generally been achieved by the well known switch-start circuit.

Cold striking is then avoided by arranging that the supply voltage is inadequate to strike the arc with cold cathodes. Instead a gas discharge occurs in a starter switch bulb which heats electrodes therein consisting of two bi-metallic strips. These strips bend toward each other, eventually completing the circuit through the lamp cathodes and causing them to heat. The gas discharge having thus been quenched, the strips cool and the circuit opens. Unless the circuit opens at zero current, a back-emf is produced which will strike the lamp. Once the lamp has struck, the voltage on the starter-switch is too low to break-over the gas so that the switch remains inoperative, otherwise the cycle repeats until the lamp either strikes or complete failure occurs. Such an electro-mechanical device has a limited life and is not suited to inclusion in an electronic

ballast. Electronic starter switches have emerged recently as replacements for the conventional 'glow-starters' but these are thyristor circuits which, at least at present, will not work with the large dv/dt conditions at high frequencies.

The problem of providing correct pre-heating for hot cathode lamps is such that prior workers developing electronic fluorescent ballasts have concluded that it is easier to develop a cold cathode lamp, which it is hoped may be cold started without detriment to life or appearance. However, this involves the introduction of a non-standard lamp and consequent problems of identification and availability.

There are several existing circuits which are 'switchless' in that they do not make use of a starter switch. The best of these is the semi-resonant start (SRS) ballast circuit.

In that circuit series resonance provides pre-heating current through the cathodes and at the same time, a high voltage across the lamp by resonant magnification.

If the system is set up correctly, the arc will not strike until the cathodes are emissive. In practice, to cater for low temperature, reduced mains voltage and worst case lamps, a compromise has to be made which means that a practical circuit will almost certainly cold strike lamps at room temperatures. The switching cycle life of lamps in SRS circuits is thus about half that for switch start circuits.

It is an object of this invention to provide an alternative form of an electronic ballast, for which the above disadvantages are alleviated.

According to the invention, there is provided a lamp driver circuit for a fluorescent circuit comprising

converter means for producing a DC output from a low frequency AC supply,

inverter means for producing a high frequency AC output from the DC output,

an inductor and a capacitor connected in series to receive the AC output, the inductor being arranged to act as an inductive ballast for a fluorescent lamp to be connected across the

capacitor, the inductor and capacitor being chosen to form a resonant circuit, and

control means arranged to cause the inverter to operate at a frequency above the resonant frequency of the resonant circuit when the lamp driver circuit is initially switched on, and then to reduce the frequency of operation towards resonance until the lamp strikes.

The converter means may desirably be arranged to draw power from the low frequency AC supply with unity power factor.

The inverter may also comprise a series arrangement of two switching means, means for defining desired instants at which one switching means is to become non-conductive and the other conductive and vice versa, means for indicating when the switching means actually become non-conducting, and means responsive to the defining and indicating means for causing the other switching means to become conductive only when the said one switching means is non-conductive and vice versa.

For a better understanding of the invention,and to show how it may be carried into effect, reference will now be made, by way of example, to the accompanying drawings in which:

Figure 1 is a schematic block diagram of a circuit for driving a fluorescent lamp,

Figure 2 is a schematic block diagram of a circuit for driving a discharge lamp,

Figure 3 is a circuit diagram of an inverter circuit of Figure 1 or 2,

Figure 4 comprises idealised waveform diagrams illustrating the operation of the inverter circuit of Figure 3,

Figure 5A is a circuit diagram of frequency control and oscillator circuits of the fluorescent lamp circuit of Figure 1 and Figure 5B is a circuit diagram of frequency control and oscillator circuits of the discharge lamp circuit of Figure 2, and

Figure 6 is a detailed circuit diagram of a switched mode power supply of Figure 1 or 2.

Referring to figure 1, a switched mode power supply 11

operates to derive reasonably constant DC from an AC supply, whilst maintaining unity power factor. An inverter 12 receives the DC output of supply 11, and provides high frequency AC to a fluorescent lamp 13, via a DC blocking capacitor C23 and a ballast inductance L2.

A frequency control circuit 14 controls the frequency of the output of the inverter 12. The circuit 14 of Figure 1 is arranged to sweep the frequency of the output during ignition of the lamp 13.

As shown in Figure 1, a capacitor C25 is connected across the lamp 13, and the output of the inverter is connected to the lamp via the ballast inductance L2 and the DC blocking capacitor C23. Capacitor C25 and inductance L2 are chosen to form a resonant circuit which resonates, in this example, at less than 28KHz.

At initial switching on of the circuit of Figure 1 the frequency control circuit is to set to operate the inverter at a frequency much higher than the resonant frequency, for example 50KHz. At this high frequency, the capacitor shunts the lamp 13 and the filaments of it are heated.

The frequency control reduces the frequency toward resonance, magnifying the voltage across the lamp 13 until it strikes. When the lamp strikes the capacitor C25 is shunted by the lamp, damping the resonance. The sweep of frequency then continues down until it stops at a preset lower operating frequency, in this example 28KHz, consistent with the required current.

Although in this example the resonance frequency is less than the running frequency it may be advantageous for resonance to be higher than the running frequency as long as it is at a lower frequency than that at which the lamp is expected to strike.

If the lamp fails to strike the frequency is controlled to limit the maximum voltage and current applied to the lamp to keep the circuit safe.

Thus the frequency control circuit ensures the lamp

filaments are heated before the lamp strikes, to help increase lamp life, and the lamp is protected from large voltages and currents.

The sweep of frequency, in this example from 50KHz towards 28KHz, is caused by sweep control circuit 15 which controls the frequency of oscillation of a clock 16 which defines the operating frequency of the inverter.

The circuit 14 also controls the mean operating frequency of the inverter to limit the maximum pre-strike voltage supplied to the lamp. For this purpose, the circuit 14 comprises a comparator 17 which compares a reference voltage with a voltage representing the actual lamp voltage If the voltage representing the actual lamp voltage exceeds the reference the frequency of the inverter is increased, the action of the sweep control 15 being at least partly overridden, to maintain the frequency away from resonance. Thus if the lamp does not strike, the lamp voltage is held at the maximum safe level (defined by the reference voltage) indefinitely.

If the lamp does strike however, the fall in the actual lamp voltage turns off the comparator 17 and the frequency sweep continues down to 28KHz.

The voltage representing the actual lamp voltage is derived from a secondary winding L2S of a transformer of which inductance L2 forms the primary, by a full wave rectifier 201.

The rectifier 201 is also connected to a series regulator circuit 202 which supplies smoothed DC (LT +) to operate the oscillator 16, sweep control 15, & driver circuit 8 of the switched mode power supply 11, and all active circuits of the circuit of Figure 1 which require a low tension supply LT +. In this way it is ensured that if the lamp 13 fails or is not connected in the circuit, the circuit ceases to operate because the low tension supply is ultimately derived in dependence upon power flow to the lamp.

Figure 1 also includes an arrangement for dimming lamp 13 by increasing the source frequency. A differential current transformer DCT1 monitors the lamp circuit and produces a

voltage representative thereof in a AC to average circuit 203. It is then compared with a voltage reference obtained from a dimming control potentiometer P1 in an error amplifier (comparator) 17'. The output of 17' is added to that of 17 to control the frequency similarly but to the different and opposing purpose of dimming. It will be appreciated that this method of dimming is insensitive to changes in supply voltage. Further the increase in cathode heating current as the supply frequency increases is also an aid to successful dimming to low levels.

The circuit of Figure 2 is similar to that of Figure 1 except that it includes a discharge lamp 18 instead of a fluorescent lamp, and the operating frequency of the inverter is swept continuously to prevent acoustic resonance of the arc in the lamp 18: Acoustic resonance is the name given to conditions in which the arc moves in an uncontrolled manner, and is highly undesirable. By continuously sweeping the frequency of operation of the inverter such resonance is avoided.

In the circuit of Figure 2 a triangular frequency modulating waveform is derived from the full wave rectified and attenuated supply by a limiter 20 and an integrator 19. The waveform is applied to the sweep control 15 to sweep the operating frequency between + and - 10KHz of normal frequency with a repetition rate of 100Hz.

It is possible to use a resonant starting circuit for discharge lamps, as described with reference to Figure 1 for fluorescent lamps. However in Figure 2, a known pulse ignition circuit 35 actuated by a start-up circuit 21 is used to initiate the discharge lamp 18.

This leaves comparator 17 free for use in controlling lamp power by altering inverter frequency. Due to the nature of high pressure discharge lamps there is no direct relationship between lamp current and lamp power, therefore sensing lamp current alone is of no use. A simpler method (the one employed) is to control the mean d.c. to the inverter power stage as sensed by for example a resistor RS and integrating

network 33. Since the inverter supply voltage is already pre-regulated by the switched mode power supply 11, then regulating the supply current to the inverter thus is regulating the power supplied to the inverter and hence to the lamp. This regulation is brought about by comparing in circuit 15 the signal representing the inverter current with the reference value and applying the resultant comparison signal to the FET2. This varies the inverter frequency and the reactance of L2 in addition to the variation due to the continuous sweep of limiter 20 and integrator 19 and thus supplying the lamp with the correct magnitude of current to sustain the desired power. At start up such a circuit would be in saturation operating the inverter at the lowest frequency and hence the lamp at the highest current thus causing a fast run-up of the lamp to its operating power.

The inverter 12 of Figure 1 or 2 comprises two switching transistors VT8 and VT9 connected in series, and controlled by a driver and logic circuit 25. It is essential that both transistors are never simultaneously conductive. Each transistor is, however, subject to charge storage effects whereby charge stored in it when it is conductive continues to flow for a short time after the base voltage controlling its conduction has changed to turn it off. The circuit 25 is arranged to ensure that the transistors VT8 and VT9 are never both simultaneously conductive despite the variable frequency of operation of the inverter.

Figure 3 shows the inverter 12 and its driver and logic circuit 25 in more detail. The example shown in Figure 3 has two fluorescent lamps 13 connected in parallel (although two discharge lamps could be used) and two load inductors L2 and L2' connected in parallel.

The two load inductors are coupled via the DC blocking Capacitor C23 to the centre tap of a series arrangment of the two switching transistors VT8, and VT9 connected across the output of the switched mode power supply 11. The collector-emitter paths of the transistors VT8 and VT9 are

shunted by diodes D20 and D21 and the bases of the transistors are connected to the secondary transformers T2 and T3 across which resistors R52 and R53 are connected.

The primary of the transformer T2 is connected in series with a driver transistor VT6 and the primary of transformer T3 is connected in series with a driver transistor VT7. The two series arrangements of primaries and transistors are in turn connected in parallel between ground and a point X which is connected to the low tension supply via a resistor R48. Preferably connection is by a circuit, not shown, which does not connect the supply when the lamp has not started.

The bases of the driver transistors VT6 and VT7 are connected by coupling circuits 26 and 27 to logic circuits 29 and 30 which control their conduction. The circuits 26 and 27 convert the logic gate outputs into a form suitable for transistor base drive.

The logic circuits 29 and 30 are arranged to ensure that transistors VT8 and VT9 are never both conductive at the same time despite the charge storage effects and their variable frequency of operation. The circuits have a clock input for receiving a clock signal CK defining nominal switching times for the transistors VT8 and VT9, and a further input coupled to the centre tap of the transistors VT8, VT9 via a coupling circuit 28 to receive a signal VCT indicative of whether or not transistor VT8 or VT9 is non-conductive. The circuits 29 and 30 have outputs T and B connected to the bases of the transistors VT6 and VT7.

They implement the logic functions

$$T = Q.\ (VCT + CK)$$

$$B = Q.\ (VCT + CK)$$

the form of signals VCT, CK and Q being as shown in idealised form in Figure 4.

Referring to Figure 4, assuming transistor VT8 is conductive (ON) the current through L2 or L2' rises and the voltage across the inductor L2 or L2' is such that the voltage at the centre tap CT is the positive potential of terminal 3+ of

the power supply 11, +400 V say.

When VT8 switches off and assuming VT9 is off, the voltage in inductor L2 or L2' reverses turning on diode D21 and causing the voltage VCT to become zero. Similarly, when VT9 is conductive and turns off, assuming VT8 is off, the voltage VCT becomes +400V when VT9 turns off, because the potential of the inductor L2 or L2' turns on diode D20.

Thus the voltage at the centre tap indicates the state of transistors VT8 and VT9.

The clock signal CK is as shown at CK in Figure 4 and defines the nominal switching times NST of the transistors VT8 and VT9. It is applied to a bistable (JK flip-flop) which derives from it signals Q and Q, of which only Q is shown in Figure 4.

Assuming VT8 is on the voltage VCT is +400V, T is logical '1' and 'B' is '0' and Q is '0'. When Q changes from '0' to '1' indicating that VT8 is to turn off, and VT9 is to turn on, T changes to '0'. However, VT8 continues to be conductive as stored charge flows out of its emitter and so voltage VCT continues to be +400 after T has changed to zero. Only when VT8 finally ceases to conduct does VCT change to zero, and only then does B change from '0' to '1' thus causing VT9 to turn on.

Thus although Q indicates a nominal switching time NST for VT8 to turn on and VT9 to turn off, (or vice versa), VT8 does not turn on until the stored change of VT9 has flowed away and VT9 actually ceases to conduct as indicated by VCT.

It is essential to the operation of the circuit that VT8 and VT9 do actually alternately conduct even for a short time, so the logic circuits 29 and 30 provide short turn on pulses P in response to CK at the end of the desired conduction periods of the transistors VT8 and VT9.

Figure 5A shows in detail the frequency control circuit 15 and the clock circuit 16 of the fluorescent lamp circuit of Figure 1.

The clock circuit 16 comprises a 555 timer 34, the clock period of which is defined by a capacitor C18 and the (variable)

resistance of a field effect transistor FET2 and fixed resistors R41, R42 and R43. The resistance of the FET2 is in turn determined by the voltage across a capacitor C17 connected between the gate and the source 2 of FET2.

The frequency control circuit comprises a comparator which compares a reference voltage defined by a zener diode DZR, with a voltage representing the actual lamp voltage of the lamps 13 and 13'. This actual voltage is derived via the rectifier 201 from the secondaries L2S and 'L2S' of the load inductances of the inverter 12, the voltage on the primaries being related to the lamp voltage.

The output of the comparator is connected to the gate of the FET2.

In the case of Figure 1 where fluorescent lamps are used, at initial switch on, the voltage across capacitor C17 is low, the resistance of FET2 is small, so the clock operates at high frequency. e.g. 50KHz, mainly defined by the time constant R41. C18. The charge on capacitor C17 builds up with time increasing the resistance of FET2 and so reducing the clock frequency until (eventually) minimum frequency is defined by R42. C18.

The effect of the circuit 15 is to modulate the charge on capacitor C17 and thus the clock frequency in dependence upon the voltage of the lamp or lamps.

The Q factor of the series resonant circuit comprising C23, L2 and the lamp cathodes is so high that operation at or near resonance has to be avoided because of the large voltages and currents which result.

The method is to limit the maximum pre-strike lamp voltage by feedback control of the inverter frequency. For simplicity the low tension windings of L2 are used to represent the voltage on L2 primary and this in turn is related to lamp voltage. If the secondary voltage attempts to exceed the reference value of zener diode DZR fed to comparator 17 the frequency of circuit 16 is increased or 'pulled back' against the action of the sweep circuit (C17) so that in the event a lamp does not strike the

lamp voltage is held at the maximum level indefinitely and the circuit remains safe. If the lamp does strike, however, the resulting (large) drop in lamp voltage and hence L2 secondary voltage turns comparator 17 off and sweep is allowed to continue, reducing frequency to the (lower) desired operating point (e.g. 28KHz) defined by R42 C18.

In the case of Figure 2, where a discharge lamp is used, the frequency of the clock is continuously swept with a period of 100Hz. For this purpose, a limiter 20 receives the FWR AC supply waveform and converts it to a bipolar square waveform and integrator 19 converts that to a bipolar triangular waveform, which is applied to the gate of FET2.

As a pulse ignition circuit 35 activated by the start-up circuit 21 is used there is no need for the frequency sweep components C17 and the resistor/diode connected from FET2 gates to 0v of the clock timer 16 of Figure 5A then serves no useful purpose. Thus the circuit 16 of the charge lamp circuit is as shown in Figure 5B.

As already stated, this leaves comparator 17 free for use in controlling lamp power by altering inverter frequency.

The switch mode power supply 11, is shown in more detail in Figure 6, and is described in detail in our co-pending application No. 81 005552 entitled "Switched Mode Power Supply", the contents of which are incorporated into this specification by virtue of this reference thereto.

However, in brief, it comprises a step-up converter formed by inductor L1, diode D1 and switching transistor VT1, fed with full wave rectified AC by a rectifier 1. A comparator 7 with hysteresis compares the input voltage sensed by a potentiometer 6 (R2, R3) with the input current sensed by resistor R1. The comparator 7 causes the transistor VT1 to switch so as to keep the instantaneous value of the input current within a fixed range of the instantaneous value of a proportion of the input voltage. The transistor is controlled by the comparator 7 via a drive circuit 8. The series arrangement of capacitors C1' and C1" connected across the output is chosen to provide a

constant DC output for a given range of load variation, the power supply 11 operating to keep the capacitors charged.

As shown in Figure 6, the supply 11 may also comprise a circuit 10 which senses when the output voltage across capacitors C1' and C1" exceeds a preset limit, and turns off the transistor VT1. It also comprises a circuit 9 which varies the voltage dividing ratio of the potentiometer 6 via an FET, FET1, to keep the output constant despite slow variations in the supply voltage.

As the full LT supply to the active circuits, in particular the drive circuit 8, of the supply 11 is not available until the inverter 12 operates fully, a start-up circuit 21 is provided.

Circuit 21 also forms a relaxation oscillator of period for example 3 sec so that the circuit will 'test' for a lamp in circuit every (3) sec. If no lamp (or no 'healthy' lamp) is in the circuit the input power remains practically zero.

What we claim is:-

1. A lamp driver circuit for a fluorescent lamp comprising

converter means for producing a DC output from a low frequency AC supply,

inverter means for producing a high frequency AC output from the DC output,

an inductor and a capacitor connected in series to receive the AC output, the inductor being arranged to act as an inductive ballast for a fluorescent lamp to be connected across the capacitor, the inductor and capacitor being chosen to form a resonant circuit, and

control means arranged to cause the inverter to operate at a frequency above the resonant frequency of the resonant circuit when the lamp driver circuit is initially switched on, and then to reduce the frequency of operation towards resonance until the lamp strikes.

2. A lamp driver circuit according to Claim 1 in which the control means is arranged to change the frequency further towards resonance after the lamp has struck until a predetermined operating frequency, between the striking frequency and the resonant frequency, is reached.

3. A lamp driver circuit according to either of the preceding claims including means for limiting the voltage applied to the lamp if the lamp fails to strike.

4. A lamp driver circuit according to Claim 3 in which the means for limiting the voltage includes means sensitive to the voltage arranged to cause the control means to control the frequency in response to said voltage.

5. A lamp driver circuit according to Claim 4 in which the means for limiting the voltage includes means comparing a further voltage representing the lamp voltage with a reference voltage and, if the further voltage exceeds the reference, overriding the change of said frequency to maintain the frequency away from resonance.

6. A lamp driver circuit according to any preceding claim including means for controlling the frequency of operation of the lamp to control the power fed thereto.

7. A lamp driver circuit according to Claim 6 including means for monitoring the current in the lamp and comparing a signal representing that current with a variable voltage reference to effect dimming of the lamp in response to variation of said reference.

8. A lamp driver circuit according to Claim 6 arranged to maintain the power fed to the lamp at a substantially constant level.

9. A lamp driver circuit according to any preceding claim in which the inventor includes a series arrangement of two switching means, the circuit further including means for deriving desired instants at which one switching means is to become non-conductive and the other conductive and vice-versa, means for indicating when the switching means actually become non-conductive, and means responsive to the defining and indicating means for causing the other switching means to become conductive only when the onw switching means is non-conductive and vice-versa.

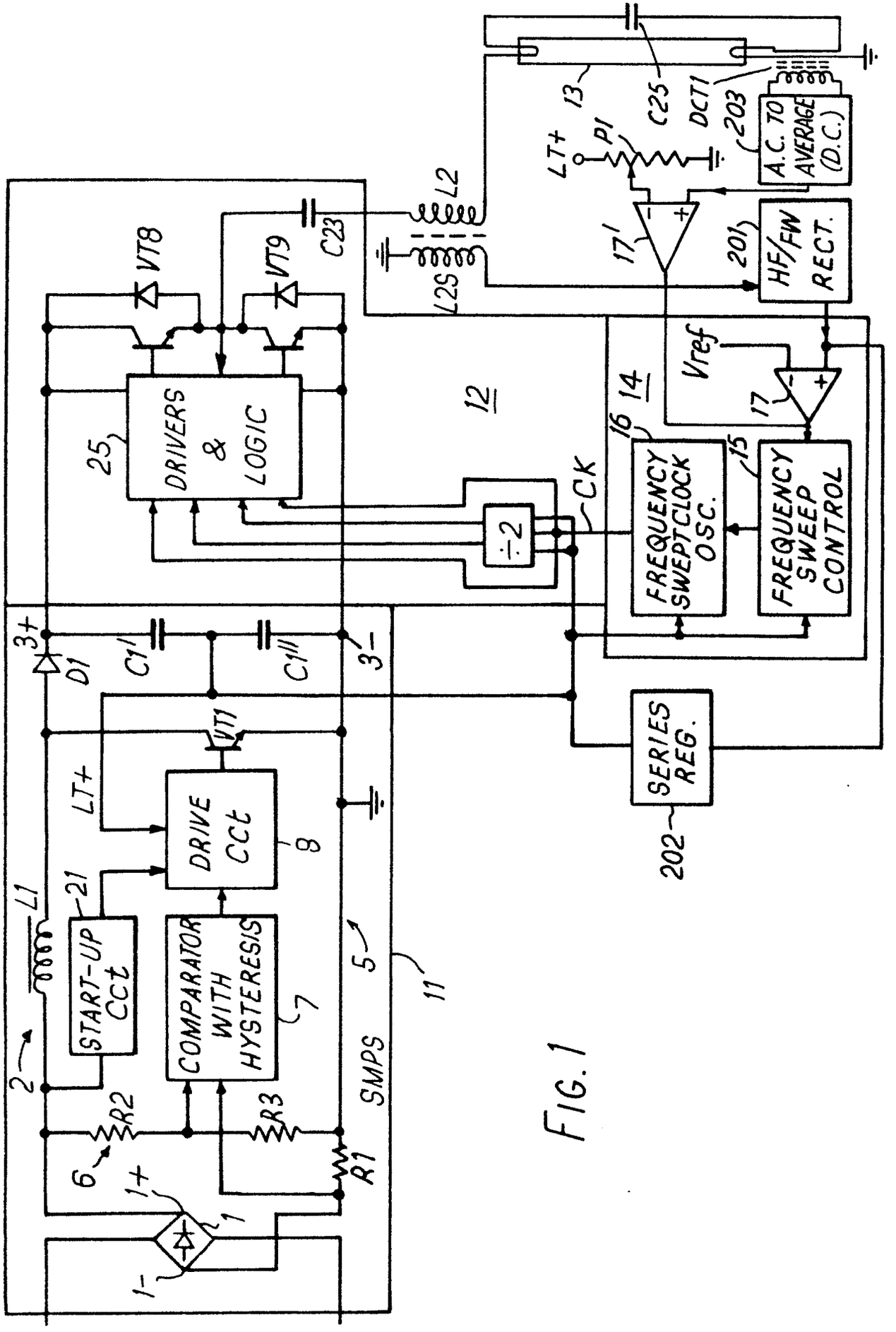
1+
1-
6
R2
R3
R1
2
L1
21
START-UP Cct
COMPARATOR WITH HYSTERESIS
7
DRIVE Cct
8
LT+
VT1
3+
D1
C1'
C1''
3-
5
11
SMPS
12
25
DRIVERS & LOGIC
VT8
VT9
C23
L2
L2S
÷2
CK
16
14
FREQUENCY SWEPTCLOCK OSC.
15
FREQUENCY SWEEP CONTROL
Vref
17
17'
201
HF/FW RECT.
203
A.C. TO AVERAGE (D.C.)
DCT1
C25
13
LT+
P1
202
SERIES REG.

FIG. 1

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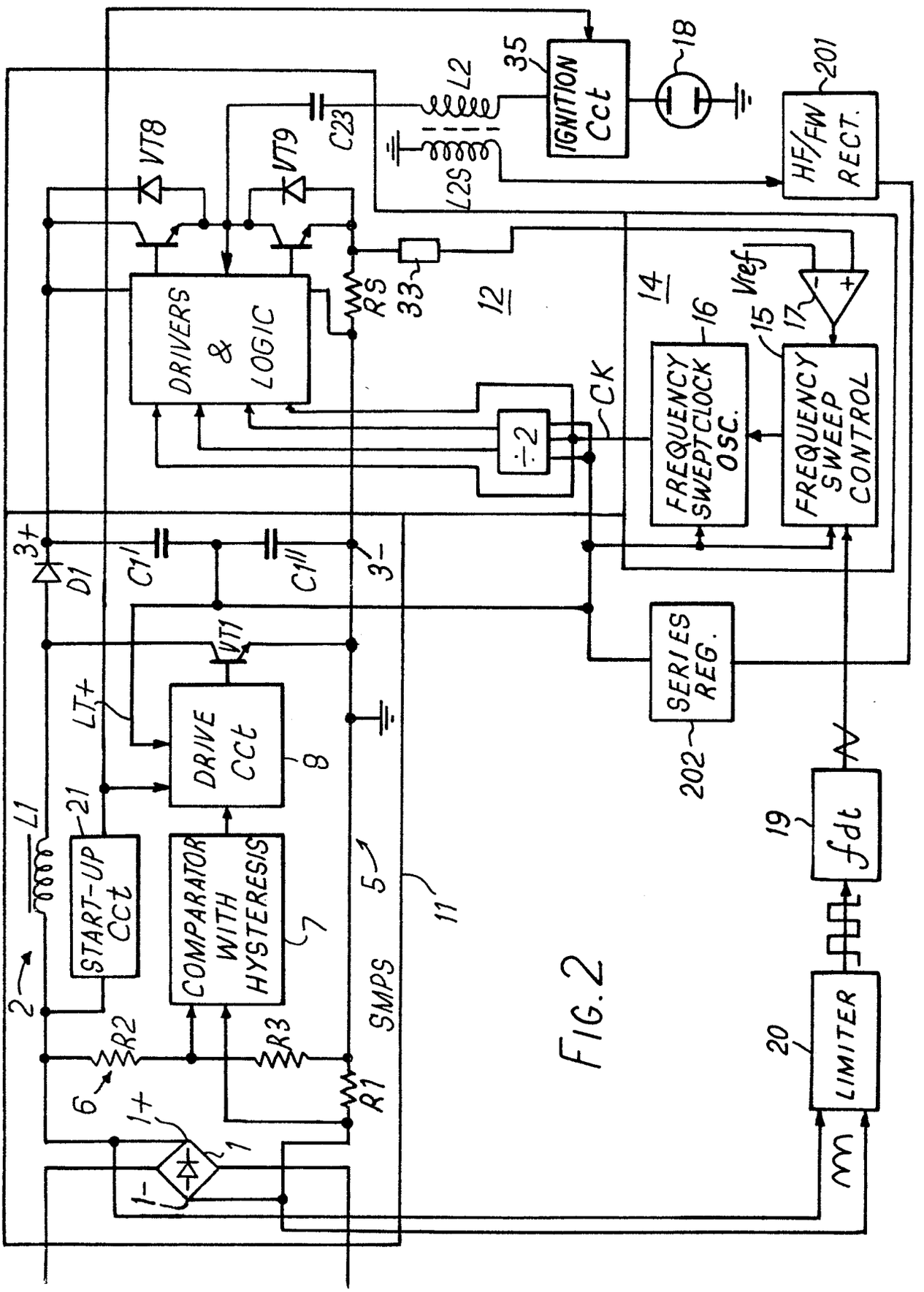

FIG. 2

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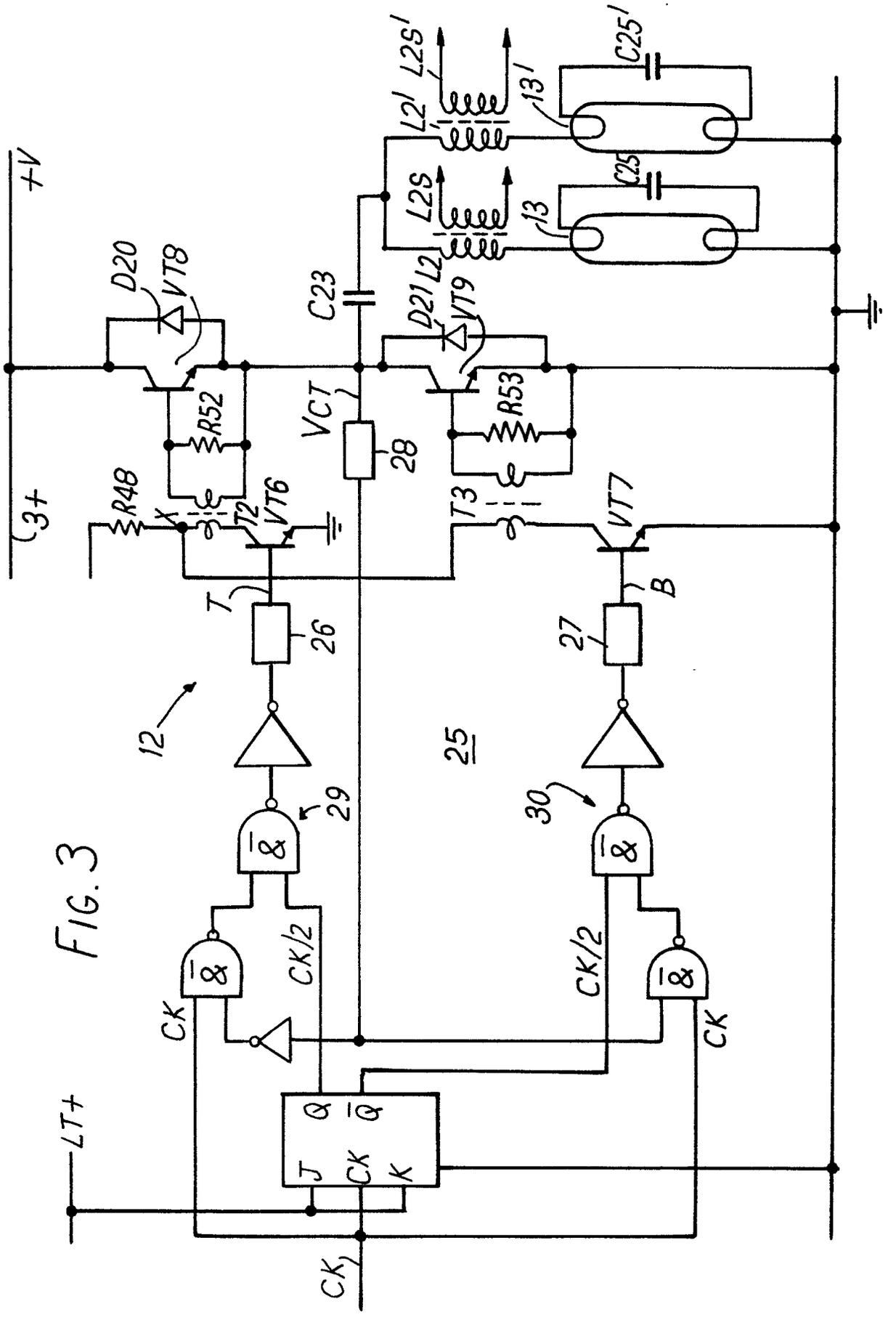

FIG. 3

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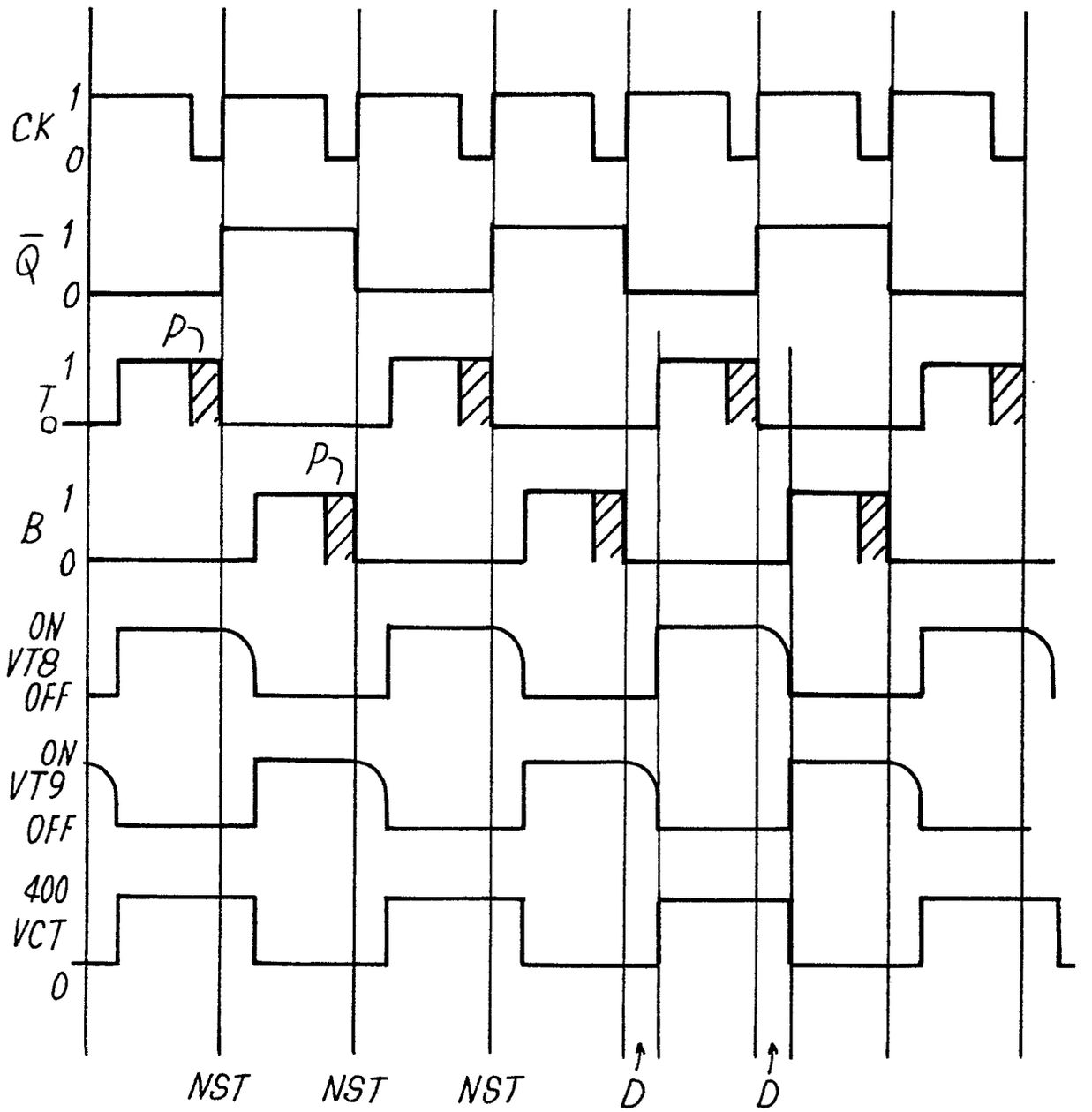
FIG. 4



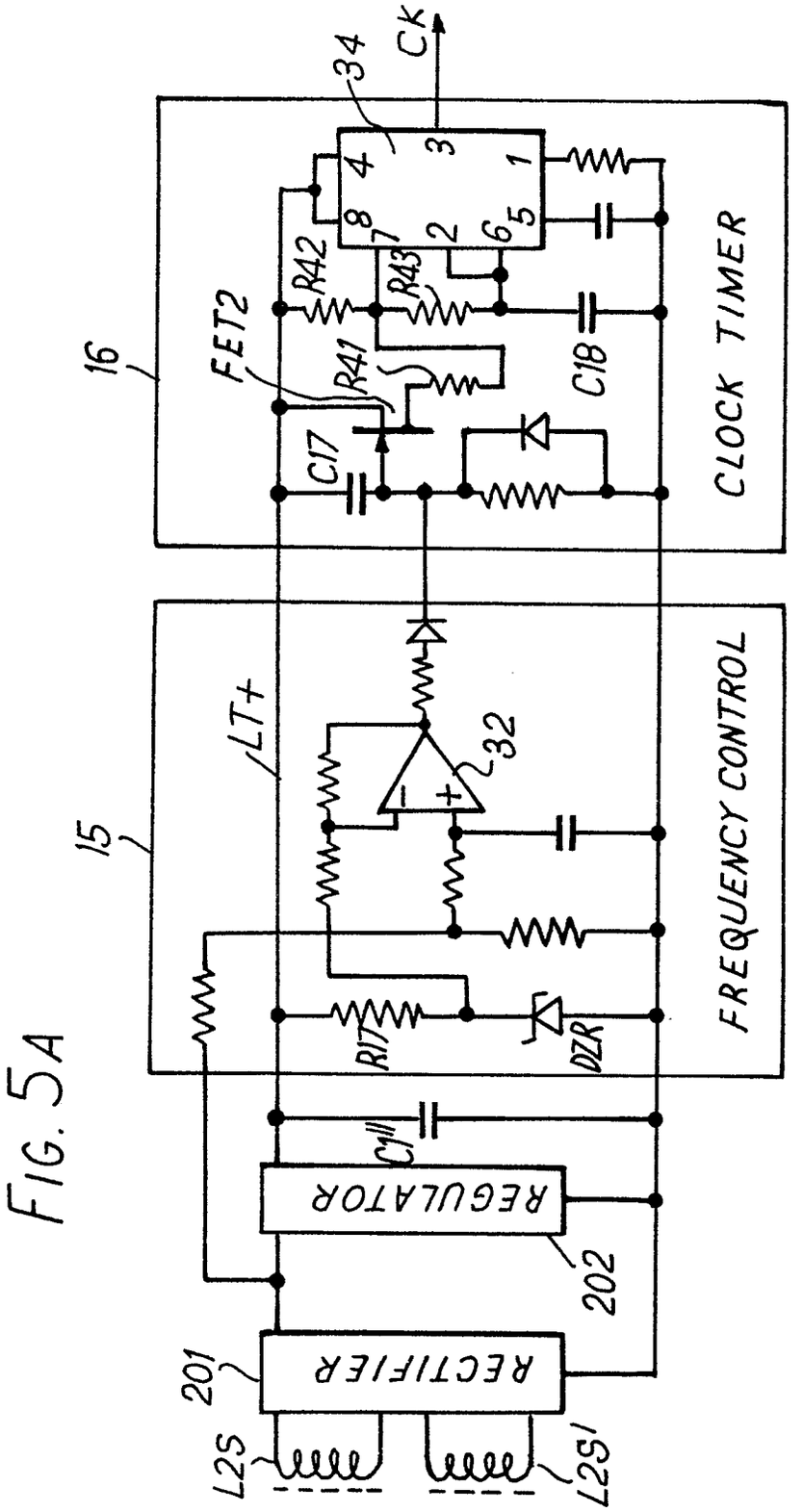
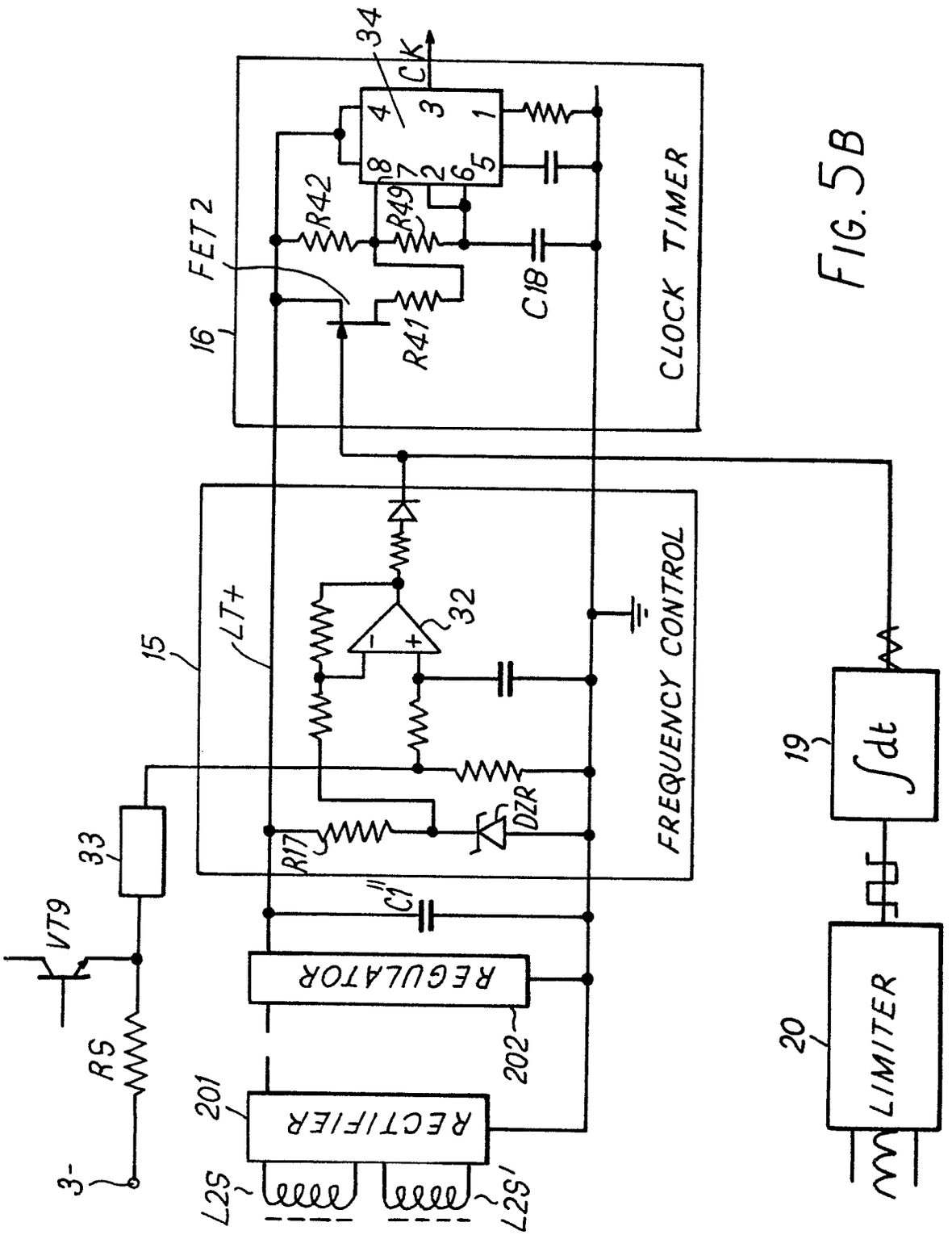

CK
34
3
4
1
8
7
2
6
5
R42
R43
FET2
R41
C18
C17
16
CLOCK TIMER
LT+
32
15
FREQUENCY CONTROL
R17
DZR
C111
REGULATOR
202
201
RECTIFIER
L2S
L2S1

FIG. 5A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LT+
32
FREQUENCY CONTROL
DZR
R17
C1"
33
VT9
RS
3-
REGULATOR
202
201
RECTIFIER
L2S
L2S'
19
∫dt
20
LIMITER

FIG. 5B

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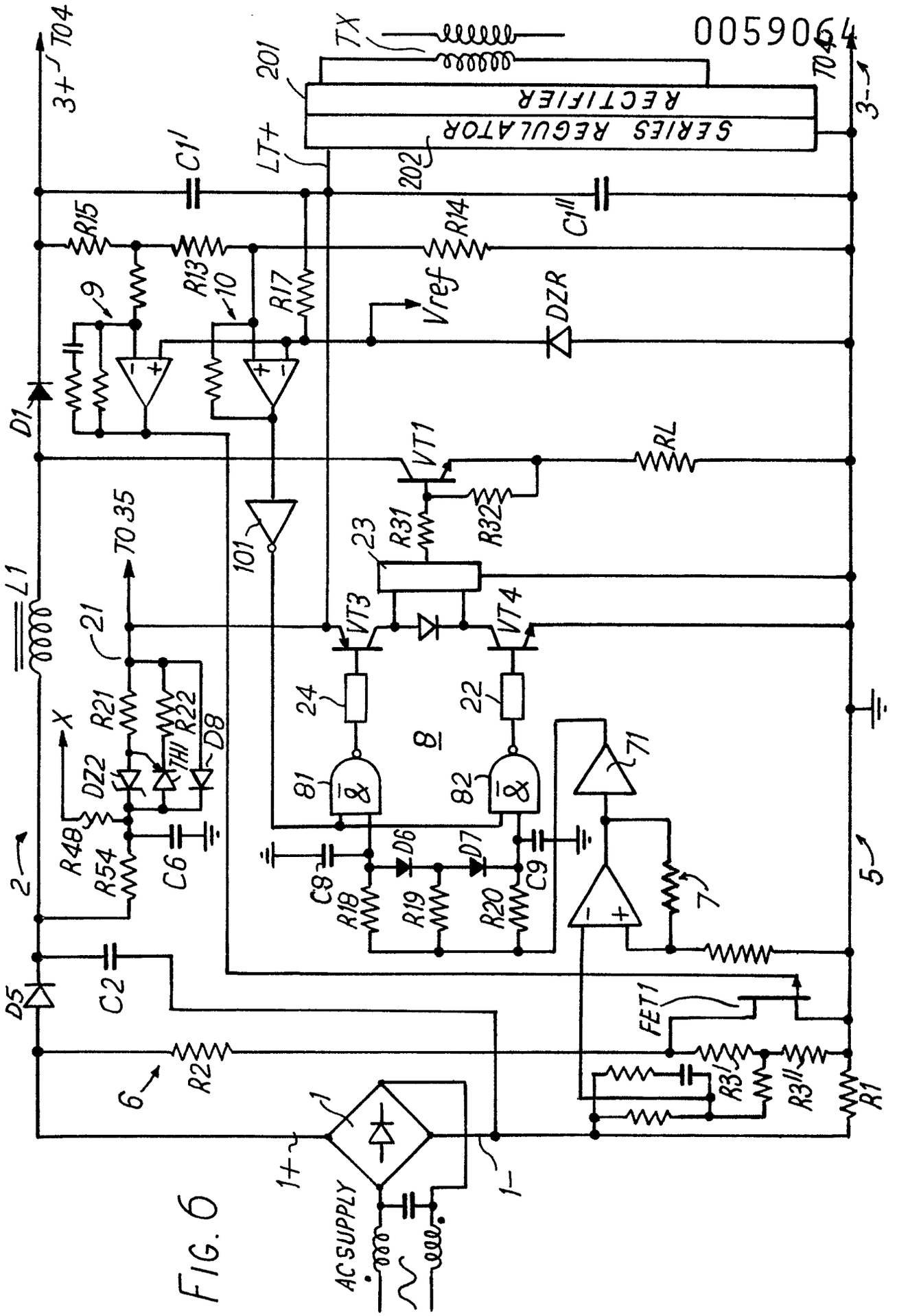

FIG. 6

European Patent Office

EUROPEAN SEARCH REPORT

0059064

Application number

EP 82 30 0787

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
X	EP-A-0 041 589 (BEATRICE FOODS) *Page 4, line 22 to page 13, line 21; figures 1a,1b*	1,2,5, 6	H 05 B 41/392
A	US-A-4 306 177 (ISAO KANEDA) *Abstract; figure 5*	1,2	
A	DE-A-2 721 253 (SIEMENS) *Page 1, claim 1*	1	

TECHNICAL FIELDS SEARCHED (Int. Cl. ³)

H 05 B 41/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	11-06-1982	DUCHEYNE R.C.L.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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D : document cited in the application
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& : member of the same patent family, corresponding document

EPO Form 1503. 03.82