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(54) **Article recognition system and processor controlled system.**

(57) Article, more particularly coin, recognition system including measuring means (L3, L4) producing a measurement signal varying at least in function of the relative position of a coin with respect to the measuring means and the coin material, and coin sensing means (L5) able to produce a control signal upon the rear edge of the coin occupying with respect to the measuring means a predetermined position wherein the coin influences the measuring means, the control signal authorizing the recording in a register (IOC) of the measurement signal then provided by the measuring means. The above system is processor controlled and includes means to prevent it entering a programme loop.

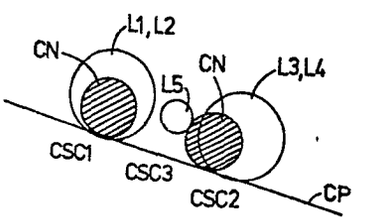

FIG.5

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Article recognition system and processor controlled system

The present invention relates to an article recognition system including measuring means producing a measurement signal varying at least in function of the relative position of said article with respect to said measuring means and of the material of said article.

Such a system and more particularly a coin recognition system is already known from British patent 1 536 904 wherein the recognition is solely based on the material of the coin.

An object of the present invention is to provide a system of the above type wherein the recognition is simultaneously based on the material and the dimensions of the article.

According to the invention this object is achieved due to the fact that the system further includes article sensing means able to produce a control signal upon a part of said article occupying with respect to said measuring means a predetermined position wherein said article influences said measuring means, said control signal authorizing the recording in a register of the measurement signal then provided by said measuring means.

By a suitable choice of the predetermined position, the greater the dimensions of an article the greater is the part of its volume influencing the measuring means at the moment said part

of the article, e.g. the rear edge thereof, occupies said predetermined position, so that the measurement signal then provided by said measuring means is function of the material as well as of the dimensions of the article.

The present invention also relates to a processor controlled system wherein the processor periodically executes clock level programmes interleaved with base level programmes, said system including a timer circuit which periodically applies a request signal for a clock interrupt programme to an interrupt input of said processor which in response to this signal and when operating correctly grants this request by applying an interrupt acknowledgement signal to an interrupt acknowledgement output.

Such a system is generally known in the computer art.

An object of the present invention is to provide a system of the above type but which is adapted to detect if the processor has entered a programme loop subsequent to the occurrence of an error, such a situation normally blocking the whole system.

According to the invention this object is achieved due to the fact that said acknowledgement output is connected to a reset input of said timer circuit which provides an alarm signal when it has not been reset by said acknowledgement signal.

In this way the alarm signal can also be used to reset the system to its initial condition. Then, as the above undesired loop condition is often due to a spurious error the processor will in general no longer re-enter a programme loop so that the system will no longer be blocked.

It should be noted that a processor controlled coin telephone system is already known e.g. from the article "N.T. 2000 Coin

Telephone Microprocessor Techniques" by D. Adolphs, published in Electrical Communication, Volume 52, N° 3, 1977, pp. 213-218.

The above mentioned and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings wherein :

Figs. 1 to 3 arranged below each other with Fig. 1 on top represent a processor controlled article recognition system and more particularly a processor controlled coin recognition system according to the invention;

Fig. 4 shows a waveform applied to comparator COR1 of Fig. 1;

Fig. 5 schematically represents a coin channel forming part of the system of Figs. 1 to 3;

Fig. 6 is a more detailed view of the data memory DMEM shown in Fig. 3.

This coin recognition system forms part of a coin controlled telephone system with a coin box (not shown) including a coin path CP (Fig. 5) which extends along three coin sensing circuits CSC1, CSC3 and CSC2 (Figs. 1 and 5) in succession and further leads to a coin collection box and to a coin refund box via deflector mechanisms (all not shown) able to be operated under the control of the system. This system includes a 1 MHz clock unit CLU (Fig. 2), a signal source SS (Fig. 2), a microprocessor MP (Fig. 2), a memory comprising a data memory DMEM (Fig. 3) and a programme memory (not shown), an input-output circuit IOC (Fig. 3), a control circuit CC (Fig. 2), the above mentioned

three coin sensing circuits CSC1 to CSC3 (Fig. 1), a coin detection and measuring circuit cooperating with CSC1 and CSC2 and mainly including a coin detection circuit CDC1 (Fig. 1) and a measuring circuit mainly comprising comparators COR1, COR2 (Fig. 1), digital-to-analogue converter DAC (Fig. 3) associated with circuit AFC and counters CR1 and CR2 (Fig. 2), a coin sensing and detection circuit including the above mentioned coin sensing circuit CSC3 and a coin detection circuit CDDC (Fig. 1), and an error detection circuit EDC mainly including a counter CR3 (Fig. 2). The arrangement operates with supply voltages Vo = 0 Volt, - V1 = -5.6 Volts and -V2 = -13 Volts.

All these circuits and their constituent parts are available on the market and to simplify the drawing only those terminals of the circuits are shown which are required to understand the invention.

The microprocessor MP (Fig. 2) is a COSMAC Microprocessor of the type CDP 1802 manufactured by RCA. It has a clock input CI connected to an output of the 1 MHz clock unit CLU, an interrupt input INT connected to a like named output INT of a NAND-gate NAND associated with counter CR3, data terminals D0 to D7 connected to like named data terminals of the data memory DMEM (Fig. 3) and of the input/output circuit IOC (Fig. 3), timing output TO controlling clock inputs CI of signal source SS and counter CR3 and control outputs CO1 to CO4 controlling control circuit CC, counter CR2, control circuit CC and counter CR3 respectively. At its timing output TO the microprocessor MP generates a square pulse waveform having a frequency f = 125 kHz derived from the 1MHz square pulse waveform provided by the clock unit CLU.

The microprocessor MP is able to execute a plurality of programmes stored in its programme memory, i.e. clock level programmes and base level programmes. These base level

programmes comprise a plurality of task programmes and a supervisory or monitor programme. Each time the processor MP has executed a task programme, control is given back to the monitor programme which amongst other operations then allocates a new task programme. The execution of the base level programmes is periodically interrupted, e.g. about every 9.3 milliseconds, by a clock interrupt signal applied to the interrupt input INT of the microprocessor MP by counter CR3. The microprocessor MP when accepting the request for interrupt activates its control output CO4 and executes a clock level programme and thereafter resumes the interrupted base level programme.

The data memory DMEM (Fig. 3) is a 256 Word x 8 Bit Static EEPROM memory of the type 1842 manufactured by RCA. It has data terminals Do to D7 connected to like named data terminals of the microprocessor MP and the input/output circuit IOC, address inputs Ao to A7, a programme input PI and an erase input EI. A storage procedure consists of addressing a cell of 8 memory locations by supplying the address thereof to the address inputs Ao to A7, applying the data to be stored to the data terminals Do to D7 and de-activating (logic 0) the programme input PI. A read procedure consists of addressing a cell and activating (logic 1) the programme input PI. The data then read appear at the data terminals Do to D7. Finally, to erase the contents of the memory it is sufficient to activate the erase input EI for 10 milliseconds with all other terminals de-activated.

The input/output circuit IOC (Fig. 3) is an 8-bit Input/Output Port of the type 1852 manufactured by RCA. It has data inputs Bo to B7 connected to data outputs Do to D7 of counter CR2 via terminals Jo to J7 and inverters INV3 to INV10 respectively, data outputs Do to D7 connected to the like named data terminals of MP and DMEM and a clock input CL connected to a like named control output of the coin detection circuit CDDC (Fig. 1),

more particularly to the output of the OR-gate OR thereof. Data applied to the data inputs Bo to B7 are strobed into the IOC when the clock input CL is activated (logic 1) and are latched therein when the activated clock input CL becomes de-activated (1 to 0 transition).

Signal source SS (Fig. 2) is a counter forming part of a Dual-Up Counter of the type 4520 manufactured by RCA and has a clock input CI fed by the square pulse waveform at frequency f = 125 kHz generated at the timing output TO of the microprocessor MP, a divide-by-2 output D2, a divide-by-4 output D4 and a divide-by-8 output D8 on which appear square pulse waveforms of frequency f3 = $\frac{125}{2}$ kHz, f2 = $\frac{125}{4}$ kHz and f1 = $\frac{125}{8}$ kHz respectively. All these square waveforms have pulses varying between -V1 and Vo.

The control circuit CC (Fig. 2) selectively enables the above pulse waveforms of frequency f1, f2 and f3 to be applied to the inputs I1, I2 and I3 of the coin sensing circuits CSC1, CSC2 and CSC3 respectively. It includes NOR-gates NOR1 to NOR3 and inverter INV1. NOR-gate NOR1 has inputs which are connected to the control output CO1 of microprocessor MP and to the divide-by-8 output D8 (fed by a pulse waveform of frequency f1) of signal source SS and an output I1 which is connected to input terminal I1 of coin sensing circuit CSC1 (Fig. 1). The control output CO1 of MP is also connected via the inverter INV1 to an input of NOR-gate NOR2 the other input of which is connected to the divide-by-4 output D4 (fed by a pulse waveform of frequency f2) of signal source SS. The output I2 of NOR-gate NOR2 is connected to input terminal I2 of coin sensing circuit CSC2 (Fig. 1). Finally, NOR-gate NOR3 has inputs which are connected to the divide-by-2 output D2 (fed by pulse waveform of frequency f3) of signal source SS and to the control output CO3 of the microprocessor MP. The output I3 of NOR3 is connected to the input terminal I3,

of coin sensing circuit CSC3 (Fig. 1).

The coin sensing circuit CSC1 (Fig. 1) with input terminal I1 and output terminal O1 includes a transformer Tr with cylindrical sensing coils L1 and L2 (Fig. 4) mounted along the above mentioned coin path CP and at a distance from each other so as to permit the passage of a coin. Input terminal I1 is connected to -V1 via resistors R1 and R2 in series, the latter resistor R2 being shunted by the series connection of filter capacitor C1 and sensing coil L1. Sensing coil L2 is shunted by filter capacitor C2 and by a further filter circuit comprising capacitor C3 in series with resistor R3, the junction point of C3 and R3 forming the output terminal O1 of CSC1.

Coin sensing circuit CSC2 with input terminal I2 and output terminal O2 is similar to coin sensing circuit CSC1 and includes a transformer with cylindrical sensing coils L3 and L4 (Fig. 1), the other components being indicated by the same numerals as those of CSC1, however provided with an accent. The coin sensing circuit CSC2 is also mounted along the above mentioned coin path CP and the same is true for coin sensing circuit CSC3 which is located between CSC1 and CSC2 (Fig. 5).

Each of the coin sensing circuits CSC1 and CSC2 is able to transform the square pulse waveform at frequency f1 or f2 applied to its input I1 or I2 into a substantially sinusoidal output voltage signal OVS (Fig. 4) appearing at the output O1 or O2 of CSC1 or CSC2, OVS varies around -V1 and has a maximum amplitude slightly larger than Vo + V1. Because Vo = 0 Volts the amplitude of this output voltage signal hence varies between a minimum value slightly smaller than -2V1 and a maximum value slightly larger than 0 Volts. As the signal is sinusoidal it is clear that it periodically becomes larger than -2V1 for nearly a whole period (Fig. 4).

When a coin CN (Fig. 5) passes between the cylindrical coils L1, L2 or L3, L4 the voltage induced in the coil L2 or L4 is damped so that the amplitude of the output voltage signal OVS (Fig. 4) is then reduced. This reduced amplitude is function of the material, i.e. the electric conductivity, of the coin at the frequency f1 or f2 and of the volume of the coin influencing the coils. This amplitude is minimum (see Fig. 4) when the centre of a coin and the centre of the coils are located on a same line perpendicular to the coin path (see Fig. 5, first coin CN from the left). Due to the amplitude reduction the time interval during which the amplitude of the output voltage signal is larger than -2V1 becomes larger than a predetermined time interval T1 (Fig. 5) and this is therefore used by CDC1 as a criterion for indicating that a coin is being sensed, as will be explained later.

The above maximum amplitude of the output voltage signal of CDC1 or CDC2 in the absence of a coin is obtained by a suitable choice of the values of R1 and R2 or R'1 and R'2. The purpose of filter circuit R3, C3 or R'3, C'3 is to suppress low frequency spurious signals generated in the coils L1, L2 or L3, L4 upon the passage between them of a magnetized coin, i.e. one having north and south poles.

The above mentioned coin detection and measuring circuit is used for detecting if a coin is being sensed or not by the coin sensing circuit CSC1 or CSC2 and for measuring the minimum reduced amplitude of the output voltage signal provided by this coin sensing circuit when a coin is being sensed. This detection and measuring circuit includes the above mentioned coin detection circuit CDC1 and a measuring circuit comprising an analogue-to-digital converter with two comparators COR1 and COR2 individually associated to CSC1 and CSC2 respectively, a common digital-to-analogue converter DAC (Fig. 3) with an associated circuit AFC and a common counter comprising CR1 ,

and CR2 (Fig. 2).

Each of the comparators COR1 and COR2 (Fig. 1) is of the type μA 339 manufactured by Fairchild and has an output I4 constituted by the collector of an NPN transistor T the emitter of which is coupled to -V2. The non-inverting input of each of these comparators is connected to the output O1, O2 of the corresponding coin sensing circuit CSC1, CSC2 respectively, and the output OT1 of the converter DAC (Fig. 3) is connected to the common inverting inputs of these comparators COR1 and COR2 via the amplifier and filter circuit AFC (Fig. 3). The outputs of COR1 and COR2 are both connected to an input I4 of the coin detection circuit CDC1 which is coupled to counter CR1 (Fig. 2). The circuit CDC1 comprises a parallel circuit constituted by collector resistor R5 and collector capacitor C4 and connected between Vo and the collector outputs of COR1 and COR2 and a series circuit constituted by clamping diode d1 and resistor R4 and connected between -V1 and I4. The junction point of d1 and R4 is connected to the output O4 of CDC1 via inverter INV2. The purpose of CDC1 is to establish the above mentioned predetermined time interval T1 which is for instance equal to 470 microseconds and to produce a de-activated binary output signal at its (normally activated) output O4 for instance when a coin is being sensed by CSC1 or CSC2 during at least this time interval. This output signal then authorizes the start of a measuring operation.

To be noted that the junction point of d1 and R4 is considered to be activated (logic 1) when its voltage is larger than $\frac{Vo - V1}{2}$ and de-activated (logic) when its voltage is smaller than this value.

Counter CR1 (Fig. 2) together with signal source SS forms the above mentioned Dual-Up counter and has a clock input CI connected to output D4 of signal source SS, a divide-by-2

output D2 on which appears a square pulse waveform of frequency $f_1 = \frac{125}{8}$ kHz when the counter is enabled, and a reset input RS which is connected to the output O4 of the coin detection circuit CDC1 and which when activated (logic 1) inhibits the counter CR1. This counter is enabled when this output O4 is de-activated i.e. when a coin is being sensed by CDC1 or CDC2 at least during the above mentioned time interval T1.

Counter CR2 (Fig. 2) is a Dual-Up-Counter of the above type but of which the two constituent counters have been interconnected so as to form a counter able to count N' from 0 to 255. This counter CR2 has a clock input CI connected to output D2 of counter CR1 and is therefore fed by a pulse waveform having a frequency f1 when this counter CR1 is enabled, a reset input RS connected to control output CO2 of microprocessor MP and outputs Do to D7 which are connected to like named inputs of IOC and DAC via inverters INV3 to INV10 and output terminals Jo to J7. Due to the presence of these inverters the counter CR2 is able to provide at the outputs Jo to J7 of these inverters a digital output signal N = 255 - N' when the digital value counted in CR2 is N'. When the counter CR2 is operated this output signal changes every period of f1 i.e. every 64 microseconds.

The digital-to-analogue converter circuit DAC (Fig. 3) is an 8-bit Buffered Multiplying DAC of the type AD7523 manufactured by Analog Devices. It has data inputs Do to D7 connected to like named outputs of counter CR2 and output terminals OT1 and RFB which are internally interconnected by a suitable feedback resistance (not shown). The DAC also has a reference input VREF connected to Vo, a ground input GND connected to -V1 and an output OUT2 also connected to -V1. When fed by the counter CR2 the DAC provides a staircase-shaped output current which is maximum for N' = 0 or N = 255 and minimum

for N' = 255 or N = 0, and which also changes every period of f1 i.e. every 64 microseconds. The circuit AFC (Fig. 3) which is connected to output OUT1 of the DAC mainly includes operational amplifier OA which is in fact of the same type as the comparators COR1 and COR2 but is now used as a low frequency operational amplifier. This use and the connection of amplifier OA to the output of the DAC is disclosed in data sheets provided by the manufacturers. The non-inverting input of this amplifier OA is connected to -V1 and its inverting input is connected to its collector output via a parallel circuit comprising filter capacitor C5 and the above mentioned feedback resistance (not shown) in the DAC. This collector output is further connected to Vo via collector resistor R5, to -V1 via filter capacitor C6 shunted by resistor R6 and capacitor C7. Capacitors C5 and C6 are filter capacitors to smoothen the staircase current waveform provided at the output of the DAC and to prevent oscillation or ringing. C7 and R6 constitute a low-pass filter providing a further filtering. The junction point 06 of C7 and R6 is connected to the common inverting inputs of COR1 and COR2. On this terminal 06 appears a linearized output or threshold voltage

$$E = -V1 - (Vo + V1)\frac{N}{256}$$

wherein N is the digital value applied to the DAC and to the DMEM. As N is able to vary between 255 and 0 and because Vo = 0 Volts the output or threshold voltage E is substantially able to vary between $-(1 + \frac{255}{256})V1$ or between about -2V1 and -V1.

As mentioned above the coin sensing and detection circuit includes coin sensing circuit CSC3 and coin detection circuit CDDC.

Coin sensing circuit CSC3 (Fig. 1) with input terminal I3 and output terminal 03 includes a cylindrical sensing coil L5 (Fig. 5) mounted along the above mentioned coin path CP and between

CSC1 and CSC2. CSC3 is however so close to CSC2 that even a coin with the smallest diameter able to be processed by the system is simultaneously sensed by CSC2 and CSC3 at least during a certain time interval. Cylindrical coil L5 has a diameter which is considerably smaller than that of coils L1 to L4 in order that the variation of the output signal at terminal O3 should be relatively abrupt. Because of the use of such a small diameter coil L5 a higher frequency f3 is required to obtain a suitable output voltage signal. Input terminal I3 is connected to one end of a parallel circuit comprising coil L5 and filter capacitor C10 via a lowpass filter circuit comprising resistor R7 and filter capacitor C9, one end of which is connected to -V1, and via coupling capacitor C8 which together with capacitor C10 constitutes a capacitive voltage divider and also prevents DC current flow from input I3 to -V1. The other end of L5, C10 is connected to -V1. Its one end is also connected to the output terminal O3 via a further filter circuit comprising capacitor C11 and resistor R8 one end of which is connected to Vo. This filter circuit C11, R8 serves for suppressing low frequency spurious signals generated by magnetized coins passing along coil L5. The coin sensing circuit CSC3 is able to transform a square pulse waveform at frequency f3 applied to its input I3 into a substantially sinusoidal signal the amplitude of which is function of the influence of a coin on sensing coil L5. In the absence of a coin this signal varies around Vo = 0 Volts and has an amplitude slightly larger than V1 so that this voltage then varies between a minimum value slightly smaller than -V1 and a maximum value slightly larger than +V1. In the absence of a coin the above sinusoidal signal periodically becomes larger than -V1 for a time interval about equal to a whole period. However, when the amplitude of this signal is reduced due to the influence of a coin it becomes larger than -V1 Volts for a time interval larger than a predetermined time interval T2 which is therefore used by CDDC as a criterion for

indicating that a coin is being sensed, as will be explained later.

The coin detection circuit CDDC is used for detecting if a coin is being sensed or not by CSC3 and for providing a corresponding binary output signal at the output of OR-gate OR (Fig. 3). A 1 to 0 transition of the latter signal is used in the case of diameter test for latching the result of the measurement then provided by the coin detection and measuring circuit.

The coin detection circuit CDDC (Fig. 1) includes a comparator COR3 which is of the same type as the comparators COR1 and COR2 and a detection circuit CDC2 which is of the same type as CDC1. The inverting input of COR3 is connected to -V1 via resistor R9 and its non-inverting input is connected to the output O3 of CSC3. The collector output or COR3 is connected to an input I5 of the detection circuit CDC2. This circuit CDC2 comprises a parallel circuit constituted by collector resistor R11 and collector capacitor C12 and connected between Vo and the collector output I5 of COR3 and a series circuit constituted by clamping diode d2 and resistor R10 and connected between -V1 and I5. The junction point O5 of d2 and R10 is connected to the like named input O5 of an OR-gate OR (Fig. 3) the other input of which is connected to the output CO3 of the microprocessor MP. The output CL of OR-gate OR is connected to the like named clock input CL of the input/output circuit IOC. To be noted that the junction point of d2 and R10 is considered to be activated and de-activated when its voltage is larger and smaller than $\frac{Vo - V1}{2}$ respectively.

The purpose of the detection circuit CDC2 is to establish the above mentioned predetermined time interval T2 which is for instance equal to 470 microseconds and to produce at the normally de-activated output O5 an activated binary output

signal only when a coin is being sensed by CDC3 during at least this time interval. A 1 to 0 transition produced on output O5 at the moment a coin is no longer sensed by CSC3 and when diameter testing is performed (CO3 on 0) is used to latch the contents of IOC via OR-gate OR.

The above mentioned error detection circuit EDC mainly includes the counter CR3 (Fig. 2) which is a COS/MOS 12-Stage-Ripple-Carry Binary Counter/Divider of the type CD4040 manufactured by RCA. It has a clock input CI which is connected to the timing output TO of the microprocessor MP and which is therefore fed by a f = 125 kHz pulse waveform, a reset input RS connected to control output CO4 of microprocessor MP and counter outputs G1 to G12. Hereby the outputs G8 and G12 are connected to the clock interrupt input INT of the micro-processor MP via a NAND-gate NAND. When the counter is regularly reset - as will be explained later - a pulse waveform comprising positive pulses having a length of about 9.216 milliseconds separated by very small reset intervals appears at the output INT of this NAND-gate NAND.

The operation of the coin recognition system is described hereinafter. Hereby it is supposed that initially the counters CR1 to CR3 are in the reset condition, that the control outputs CO1, CO2 and CO4 of the microprocessor MP are de-activated, whereas control output CO3 is activated and that the outputs O4 and O5 in the coin detecting circuits CDC1 and CDC2 are activated and de-activated respectively.

The f = 125 kHz square pulse waveform varying between -V1 and Vo = 0 Volts generated at the timing output TO of the microprocessor MP is applied to the clock inputs CI of signal source SS and counter CR3. The counter CR3 is stepped and at a certain moment the interrupt output INT of the associated gate NAND is activated, this signal having no influence on the

operation of the microprocessor MP which is for instance executing one of the base level programmes. The signal source SS provides at its outputs D8, D4 and D2 the above square pulse waveforms of frequency f1, f2 and f3 which are applied to NOR-gates NOR1, NOR2 and NOR3 of which only NOR1 is enabled. The square pulse waveform at frequency f2 is also applied to the clock input CI of counter CR1 the operation of which, however, is inhibited as its reset input RS is activated by the activated output O4 of the detection circuit CDC1.

Due to the NOR-gate NOR1 being enabled a square pulse waveform at frequency f1 is applied to input I1 of coin sensing circuit CSC1. In the absence of a coin between the sensing coils L1 and L2 of transformer Tr a substantially sinusoidal output voltage signal OVS (Fig. 4) varying between a minimum value slightly smaller than $-2V1 - Vo$ or $-2V1$ because $Vo = 0$ Volt and a maximum value slightly larger than $Vo = 0$ Volt is applied to the non-inverting input O1 of comparator COR1. Because the counter CR2 has been reset its digital output N' is zero so that, via the DAC, a threshold signal $E = -(1 + \frac{255}{256})V1$ or about $-2V1$ is applied to the inverting input of COR1. During the time intervals that the sinusoidal output voltage signal at the non-inverting input of COR1 decreases below this threshold value the output transistor T of COR1 becomes conductive so that the voltage at the output terminal I4 of COR1 then becomes equal to -V2, the capacitor C4 being thereby charged between Vo and -V2. Consequently the junction point of diode d1 and resistor R4 is then de-activated, its potential being substantially equal to -V1 due to diode d1 being conductive, and the output O4 of CDC1 is then activated (logic 1). As soon as the sinusoidal voltage at the non-inverting input of COR1 again increases above this threshold value E, about equal to -2V1, the output transistor T of COR1 is again blocked so that capacitor C4 is then allowed to discharge via resistor R5 and via diode d1 and resistor R4 (as long as diode d1 remains

conductive). Thus the voltage at the output terminal I4 gradually increases towards Vo. Also the junction point of diode d1 and resistor R4 then gradually increases from about -V1 towards Vo, whilst the output terminal O4 of CDC1 gradually decreases from logic 1 to logic O. This logic O can however only be reached if the capacitor C4 is allowed to discharge during a predetermined time interval T1 of about 470 microseconds. Because in the absence of a coin the output transistor T of comparator COR1 is periodically blocked for time intervals smaller than T1 (see Fig. 4), it is clear that the output terminal O4 of the CDC1 remains activated so that a measuring operation cannot be started.

When a coin such as CN (Fig. 5) is introduced in the coin box, it first passes between the sensing coils L1 and L2 of the transformer Tr of coin sensing circuit CSC1 due to which the amplitude of the sinusoidal voltage signal normally varying between a minimum value slightly smaller than -2V1 + Vo and a maximum value slightly larger than Vo gradually decreases towards a minimum value and afterwards again gradually increases. This is shown in Fig. 4 wherein two different time scales are used in the left and right hand parts of the drawing. More particularly when a coin is present the amplitude of this reduced signal becomes larger than -2V1 + Vo for a time interval much larger than the above mentioned predetermined time interval T1. This amplitude reduction and more particularly the minimum amplitude is detected by the coin detection circuit CDC1. Indeed, because a threshold voltage signal having an amplitude equal to $E = -(1 + \frac{255}{256})$ V1 or about -2V1 is still being applied to the inverting input of the comparator COR1 the output transistor T thereof remains blocked for a time interval much larger than T1. Thus the capacitor C4 is allowed to discharge to such a value that the junction point of diode d1 and resistor R4 becomes activated and that the output O4 of CDC1 becomes de-activated. Thus

counter CR1 is enabled. As soon as this happens a measuring or analogue-to-digital operation is started. Indeed, this counter CR1 then counts the pulses of the square pulse waveform at frequency f2 applied to its clock input CI, and at its output D2 it generates a pulse waveform of frequency f1 which is applied to counter CR2. The pulses of this waveform are counted in counter CR2 which provides at its data outputs Do to D7 a gradually increasing digital value N' which is inverted so as to become a gradually decreasing digital value N = 255 - N' applied to converter DAC coupled to circuit AFC. At the output O6 thereof appears the above mentioned threshold voltage E which substantially linearly increases from about -2V1 towards -V1 with a speed depending on the period of f1, this period being equal to 64 microseconds. This voltage is applied to the inverting input of comparator COR1.

The threshold voltage increases together with the increasing output voltage signal OVS until the voltage amplitude of the latter signal has reached its minimum value and again starts increasing. From that moment on the output transistor T of comparator COR1 becomes conductive for a time interval sufficiently long to activate output O4 of CDC1. As a consequence counter CR1 is reset so that pulses are then no longer allowed to counter CR2 which therefore remains in the position attained wherein it stores the result of the measurement of the above minimum amplitude of the output voltage signal OVS. This result which is for instance N = N1 also appears at the outputs Do to D7 of the input/output circuit IOC due to the input CL thereof being on 1(CO3 activated).

From the above it follows that the digital value N = N1 stored in the IOC is a measure of the minimum amplitude of the sinusoidal voltage signal applied to COR1 this minimum amplitude being caused by the introduction of a coin between the two sensing coils L1 and L2 of the transformer Tr and being function

of the material and the volume of the coin.

During the gradual increase of the threshold voltage E it may happen that it temporarily increases beyond the voltage level of the output voltage signals OVS, before the latter has reached its minimum amplitude. However the time intervals during which this happens are so small that the output O4 remains de-activated.

When the counter CR3 which is continuously operated has counted 9.216 milliseconds the output INT of the NAND-gate NAND is de-activated and the same is true for the interrupt input INT of the microprocessor MP. Thus this microprocessor is requested to interrupt the base level programme it is executing and to start the clock level programme. When the microprocessor MP grants this request it activates its control input CO4 which is in fact a request acknowledgement output due to which the counter CR3 is reset. As a consequence the output INT of the NAND gate NAND associated to this counter CR3 is again activated.

During the execution of the clock interrupt programme the processor MP enters the digital value appearing at the outputs D_0 - D7 of the input/output circuit IOC in one of its internal registers (not shown).

Because the execution of a clock programme is not synchronized with a measuring operation it may happen that this measuring operation is not yet finished at the moment the contents of the counter CR2 are read by the microprocessor. However this is without importance because during a following clock level programme the processor MP will again enter the measured result stored in IOC in one of its internal registers, and will then also compare the newly entered result entered with the previous entered result and accept the new result only definitively when it is equal to the previous result (except

when the result is O). If not, the previous result is disregarded.

During the clock interrupt programme wherein the digital value, e.g. N = N1, is finally definitively accepted by the processor MP the latter activates control output CO1 to enable NOR-gate NOR2 and to inhibit NOR-gate NOR1. The MP further activates control output CO2 to reset counter CR2 and de-activates or activates control output CO3 depending on a diameter test having to be performed or not respectively.

In case no diameter test has to be performed the output of NOR-gate NOR3 remains on O as the input of this gate which is connected to output CO3 of the MP is then activated..

On the contrary, in case a diameter test has to be performed output CO3 is de-activated so that a square pulse waveform at frequency f3 then appears at the output of NOR-gate NOR3 and is applied to coin sensing circuit CSC3. Therein this pulse waveform is transformed into a substantially sinusoidal waveform. As long as the above coin CN (Fig. 5) which has left the coin sensing circuit CSC1 does not influence coil L5 of coin sensing circuit CSC3 the last mentioned sinusoidal waveform has its maximum amplitude which is such that its negative half waves slightly exceed the voltage -V1. Consequently the output transistor (not shown) of the comparator COR3 to which this waveform is applied regularly becomes conductive so that the voltage at the junction point O5 of diode d2 and resistor R10 in the coin detection circuit CDC2 remains de-activated and the same is true for the clock output CL of OR gate OR (Fig. 3).

When the coin CN at a certain moment influences coil L5 of coin sensing circuit CSC3 the amplitude of the sinusoidal waveform applied to the comparator COR3 of the coin detecting circuit

CDC2 decreases to such an extent that the negative half waves of this waveform no longer exceed the voltage -V1. This condition remains as long as the coin influences coil L5 i.e. for a time interval much larger than the predetermined time interval T2 of about 470 microseconds established by the coin detecting circuit CDC2. As a consequence the output transistor (not shown) forming part of the comparator COR3 remains blocked for a time sufficient to permit the junction point 05 of diode d2 and resistor R10 in the circuit CDC2 to become activated. As a result the clock output CL of OR-gate OR (Fig. 3) is then activated due to which the data applied to the data input D_0-D7 of the IOC are strobed but not latched in this register.

Coil L5 of CSC3 is so mounted with respect to coils L3, L4 of CSC2 that even a coin with the smallest diameter able to be handled is sensed by CSC2 at the moment the passage of its trailing edge is sensed by CSC3. Obviously the coin volume then sensed by CSC2 is proportional to the coin diameter. As soon as a coin is being sensed by the sensing coils L3, L4 of CSC2 a measuring operation similar to that described in relation with CSC1 but now using comparator COR2 is started so that the digital result of this operation at the moment the trailing edge of the coin no longer influences the sensing coil L5 is also a measure of this diameter.

For this reason the moment at which the above mentioned coin no longer influences sensing coil L5 is detected and the digital result, say N = N3 then applied to the DAC is latched in the IOC, in the way described hereinafter. More particularly, at the moment the coin no longer influences the sensing coil L5 the amplitude of the sinusoidal waveform applied to the comparator COR3 again increases beyond -V1 and the junction point 05 of diode d2 and resistor R10 in the circuit CDDC then again becomes de-activated and the same is true for the clock

output CL of OR-gate OR. By this 1 to 0 transition of the clock output CL the data N = N3 applied to the IOC is latched therein. This latching is necessary because the contents of CR2 do not remain constant as CSC2 continues its measurement.

During the execution of a subsequent clock interrupt programme the microprocessor MP reads the value N = N3 stored in the IOC and stores it in one of its internal registers. Again, this value is only accepted definitively when a same value is found during the execution of two immediately successive clock interrupts. If this is the case the MP then activates its output CO3 to inhibit the diameter test.

As already mentioned above, during this test the coin is also sensed by the coin sensing circuit CSC2. At the end of this sensing operation a digital value e.g. N = N2 is stored in the IOC. In a same way as described above this value is then stored in a register of the MP and only accepted definitively when a same value has been found two times in succession.

From the above it follows that three digital values N1, N2 and N3 have been stored in the microprocessor MP. The latter then uses these values and the contents of memory DMEM to find out if the coin measured should be accepted as valid or not. These contents are schematically represented in Fig. 4 and comprise three sets of two digital values, i.e. a minimum and a maximum value. Each three sets of minimum and maximum digital values for a particular type of coin has been obtained by performing a plurality of measurements on a plurality of coins of this type at the frequencies f1, f2 and f2.
For instance :
- for a coin of a type o = a first set N11 MIN and N11 MAX;
a second set N21 MIN and N21 MAX;

a third set N31 MIN and N31 MAX.

- for a coin of type m = a first set N1m MIN and N1m MAX;
a second set N2m MIN and N2m MAX;
a third set N3m MIN and N3m MAX.

The microprocessor MP compares the measured digital value N1 successively with the sets of stored digital values of the first series N11 MIN, N11 MAX to N1m MIN, N1m MAX to find out to which set the coin measured belongs. If N1 does not belong to this first series of sets the coin is not accepted as valid and led to the refund box, whereas when it belongs to one of these sets the microprocessor MP successively checks whether or not the measured digital values N2 and N3 belong to the homologue or correlated sets in the second and third series of sets of stored digital values N21 MIN, N21 MAX to N2m MIN, N2m MAX and N31 MIN, N31 MAX to N3m MIN, N3m MAX. If the coin does not belong to both these related sets it is rejected and led to the refund box, whereas otherwise it is accepted as valid.

Using only the minimum and maximum digital values of the number of values which have been obtained by testing several coins of a same type has in certain cases proved to be insufficient to distinguish between valid and non-valid coins. Indeed, it has for instance been found, in case no diameter test is performed, that some valid coins provide measured values N1 and N2, e.g. situated in the range between N11 MIN and N11 MAX and in the range between N21 MIN and N21 MAX respectively whilst non-valid coins provide measured values say N4 and N5, situated in the same ranges. In this case one has to further narrow each of these ranges, e.g. in three possible overlapping subranges N11 MIN, N1a; N1b, N1c; and N1d, N11 MAX and N21 MIN, N2a; N2b, N2c; and N2d, N21 MAX and to accept a coin as valid only when it belongs to homologue or correlated subranges e.g. N11 MIN, N1a and N21 MIN, N2a.

As already mentioned above, when the microprocessor MP grants a request (de-activation of interrupt input INT) for a clock interrupt programme it activates its control output CO4, due to which counter CR3 is then reset by the activation of its reset input RS. The processor MP then also substracts a unit from a value stored in a counter word CR of the memory MEM, this value being at most equal to Np (Fig. 6). As also described above, after the microprocessor MP has finished a clock level programme it resumes the interrupted task level programme and after having executed this programme it executes the monitor programme. Under the control of this programme the value stored in the counter word CR is made equal to the maximum value Np. The latter value has been so chosen that taking the interrupts into account the resultant value stored in the counter word CR never becomes zero under normal operating conditions.

However, if due to an error which is generally a spurious one, the processor MP enters a programme loop during the execution of a clock interrupt programme, it will in general not be able to react to a request for a clock interrupt, i.e. to a de-activation of its interrupt input INT by the counter CR3. The microprocessor MP will therefore also not activate its control output CO4 to reset the counter CR3 and the latter will therefore be able to count further than 9.216 milliseconds. At a certain moment the alarm output G12 which is a general reset output will therefore be activated to reset all the constituent parts of the system (not shown). All operations will then start from the beginning under the control of the processor MP and in most cases the system will then operate correctly because the error is generally a spurious one.

If the processor MP enters a programme loop during the execution of a base level programme it generally remains able to react to a request for a clock interrupt applied to its interrupt,

input INT by the counter CR3. However, because no monitor programme is executed the value stored in the counter word CR will not periodically be set to Np but will each time be decreased by 1 and finally reach O. When this happens the processor MP disables the interrupt input INT so that it is no longer able to react to request for a clock interrupt and that the counter CR3 is not reset. Just as in the above considered case this counter is therefore able to count further until its alarm output G12 is activated.

In the above described coin detection arrangement the end of the passage of a coin is sensed by the coin sensing and detection circuit CSC3, CDDC. It would also be possible to mount CSC3, behind CSC2 and to sense the start of such a passage. Obviously the coils L3, L4 and L5 have then still to be located at such a distance from each other that a coin which is just sensed by L5 is also sensed by L3, L4.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention.

Claims

1. Article recognition system including measuring means producing a measurement signal varying at least in function of the relative position of said article with respect to said measuring means and of the material of said article, characterized in that it further includes article sensing means (CSC3, CDDC) able to produce a control signal (O5) upon a part of said article occupying with respect to said measuring means (CSC2, CDC2, COR2, DAC, AFC, CR1, CR2) a predetermined position wherein said article influences said measuring means, said control signal (O5) authorizing the recording in a register (IOC) of the measurement signal then provided by said measuring means.

2. Article recognition system according to claim 1, characterized in that said part of said article is moving with respect to said article sensing means (CSC3, CDDC) and is constituted by the trailing edge of said article when considered in the direction of said predetermined position towards said measuring means.

3. Article recognition system according to claim 1, characterized in that said article sensing circuit (CSC3, CDDC) includes a first sensing circuit (CSC3) providing a first output signal having an electric characteristic which is function at least of said material and the relative position of an article and said first sensing circuit, and a first

detection circuit (CDDC) coupled to said first sensing circuit (CSC3) for detecting a modification of said electric characteristic caused in said first sensing circuit (CSC3) by the passage of an article and for providing said control signal (O5).

4. Article recognition system according to claim 3, characterized in that said first sensing circuit (CSC3) provides said first output signal the amplitude of which varies around a first reference level (Vo) in such a way that it periodically exceeds a second reference level (-V1) for a time interval smaller than a predetermined first time interval (T2) in the absence of an article and for a time interval larger than said predetermined first time interval (T1) in the presence of an article and that said first detection circuit (CDDC) includes a first comparator (COR3) with a first input to which said first output signal is directly applied, with a second input to which said second reference level (-V1) is applied and with an output (I5) coupled to the input of a first timing circuit (C12, R11, R10, d2) which is able to establish said predetermined first time interval and which is started and reset when the inputs of said first comparator (COR3) have a first and a second relationship with respect to each other respectively, said first timing circuit providing a second output signal when said inputs of said comparator (COR2) have a first predetermined relationship for a time interval larger than said predetermined first time interval (T2) due to an article being sensed by said first sensing circuit (CSC3).

5. Article recognition system according to claims 2 and 4, characterized in that said control signal (O5) is constituted by a predetermined variation of said second output signal, said predetermined variation being produced upon said trailing edge of said article leaving said first sensing circuit (CSC3).

6. Article recognition system according to claim 4, characterized in that said first comparator (COR3) includes a first transistor the collector-emitter path of which is coupled between said output (I5) of said comparator (COR3) and a third reference level (-V2) and that said first timing circuit (C12, R11, R10, d2) includes a first parallel circuit connected between said first reference level (Vo) and said comparator output (I5) and comprising a first capacitor (C12) and a first resistor (R11), and a first series circuit (d2; R10) connected between said second reference level (-V1) and said comparator output (I5) and comprising a first diode (d2) and a second resistor (R10), the junction point (05) of said first diode (d1) and said second resistor (R10) being coupled to a latch input of said register (IOC).

7. Article recognition system according to claim 4, characterized in that said first sensing circuit (CSC3) is adapted to transform a first square pulse waveform varying between said first (Vo) and second (-V1) reference levels into a first substantially sinusoidal output signal which constitutes said first output signal.

8. Article recognition system according to claim 7, characterized in that said first sensing circuit (CSC3) includes at least one sensing coil (L5) mounted along a path followed by said article and forming part of a first filter circuit having an input (I3, -V1) to which said square pulse waveform is applied and across which a third resistor (R7), a second capacitor (C8) and a third capacitor (C10) which shunts said sensing coil (L5) are connected in series, a fourth capacitor (C9) shunting the series connection of said second (C8) and third (C10) capacitors.

9. Article recognition system according to claim 1, characterized in that said measuring means include a second

sensing circuit (CSC2) providing a third output signal having an electric characteristic which is function at least of said material and relative position of said article and said second sensing circuit, and a detection and measuring circuit (CDC1, COR2, DAC, AFC, CR1, CR2) coupled to said second sensing circuit and including a second detection circuit (CDC1) for detecting a modification of said electric characteristic caused in said second sensing circuit by the presence of an article, and a measuring circuit (COR2, DAC, AFC, CR1, CR2) for measuring a thus modified electric characteristic and providing said measurement signal.

10. Article recognition system according to claim 9, characterized in that said measuring circuit provides said measurement signal under digital form and includes an analogue-to-digital converter (COR2, DAC, AFC, CR1, CR2) adapted to convert said electric characteristic of said third output signal into said digital form after said second detection circuit (CDC1) has detected a modification of said electric characteristic and has provided a second control signal (O4) to enable the operation of said analogue-to-digital converter, and that said analogue-to-digital converter includes a second comparator (COR2) with a first input to which said third output signal is directly applied, with a second input and with an output (I4) coupled via said second detection circuit (CDC1) with a control input (RS) of a counter (CR1, CR2) which stores said measurement signal under digital form and which has an output coupled with an input of a digital-to-analogue converter (DAC, AFC) having an output coupled with said second input of said second comparator (COR2), said second detection circuit (CDC1) providing said second control signal (O4) on said control input (RS) of said counter (CR1, CR2) when an article is being sensed by said second sensing circuit (CSC2), said second control signal enabling the operation of said counter (CR1, CR2) and of said digital-

to-analogue converter (DAC, AFC) which then provides a varying threshold signal at its output, the output of said counter (CR1, CR2) being also coupled with said register (IOC).

11. Article recognition system according to claim 10, characterized in that said second sensing circuit (CSC2) provides said third output signal the amplitude of which varies around a third reference level (-V1) in such a way that it periodically exceeds a fourth reference level (-2V1) for time intervals smaller than a predetermined second time interval (T1) in the absence of an article and for a time interval larger than said predetermined second time interval (T1) in the presence of an article, and that said second detection circuit (CDC1) comprises a second timing circuit (C4, R5, R4, d1) able to count said predetermined second time interval (T1) and the input of which is coupled to the output of said second comparator (COR1) and which is started and reset when the inputs of said second comparator (COR1) have a first and a second relationship with respect to each other respectively, said second timing circuit providing said second control signal (O4) when said inputs of said comparator (COR1) have a first predetermined relationship for a time interval larger than said predetermined time interval (T1) due to an article being sensed, said second control signal (O4) then starting the operation of said analogue-to-digital converter which provides said variable threshold signal varying from said fourth reference level (-2V1) towards said third reference level (-V1) until said inputs of said comparator (COR2) have said second predetermined relationship, said counter then providing said measurement signal.

12. Article recognition system according to claim 9, characterized in that said second sensing circuit (CSC2) is adapted to transform a second square pulse waveform into a second substantially sinusoidal waveform which constitutes said third output signal.

13. Article recognition system according to claims 11 and 12, characterized in that said second square pulse waveform varies between Vo and -V1, whilst said second sinusoidal signal varies around -V1 and has an amplitude equal to V1 + Vo, and that said digital-to-analogue converter provides at its output said threshold signal $E = -V1 + (Vo + V1) \frac{N}{256}$, wherein -V1 is said third reference level, Vo is a fifth reference level and N is the digital value supplied by said counter (CR1, CR2) to said digital-to-analogue converter (DAC, AFC).

14. Article recognition system according to claim 12, characterized in that said second sensing circuit (CSC2) includes two first sensing coils (L3, L4) mounted at opposite sides of a path followed by said article and constituting the primary (L3) and secondary (L4) windings of a transformer which forms part of a second filter circuit having an input (-V1, I1) to which said square pulse waveform is applied and across which said primary winding (L3), a fifth capacitor (C'1) and a fourth resistor (R'1) are connected in series, the series connection of said primary winding (L3) and said fifth capacitor (C'1) being shunted by a fifth resistor (R'2) and said secondary winding (L4) being connected in parallel with a sixth capacitor (C'2) across an output (-V1, O2) of said second filter circuit, said second sinusoidal signal appearing at said output of said second filter circuit.

15. Article recognition system according to claim 8 or 14, characterized in that at least one of said first and second sensing circuits includes a first and a second lowpass filter C10, R8; (R'3, C'3) respectively for preventing magnetized articles from having an influence on said first and third output signal respectively.

16. Article recognition system according to claims 14 and 15, characterized in that said second lowpass filter (R3, C3) ,

includes the series connection of a sixth resistor (R'3) and a seventh capacitor (C'3) connected across said secondary winding (L4) and said sixth resistor (R3) being connected across said output (-V1, O1) of said second filter circuit.

17. Processor controlled system wherein the processor periodically executes clock level programmes inter-leaved with base level programmes, said system including a timer circuit which periodically applies a request signal for a clock interrupt programme to an interrupt input of said processor which in response to this signal and when operating correctly grants this request by applying an interrupt acknowledgement signal to an interrupt acknowledgement output, characterized in that said acknowledgement output (CO4) is connected to a reset input (RS) of said timer circuit (CR3) which provides an alarm signal when it has not been reset by said acknowledgement signal.

18. Processor controlled system according to claim 17, characterized in that said processor (MP) has an associated memory (DMEM) which stores a counter word (CR) and is able to periodically set said counter word (CR) to a first predetermined value (Np) and to modify said value each time it grants a said interrupt request and that said processor after the contents of said counter word (CR) have reached a second predetermined value (O) because it has not been set by said processor disables its said interrupt input and therefore also said acknowledgement output (CO4).

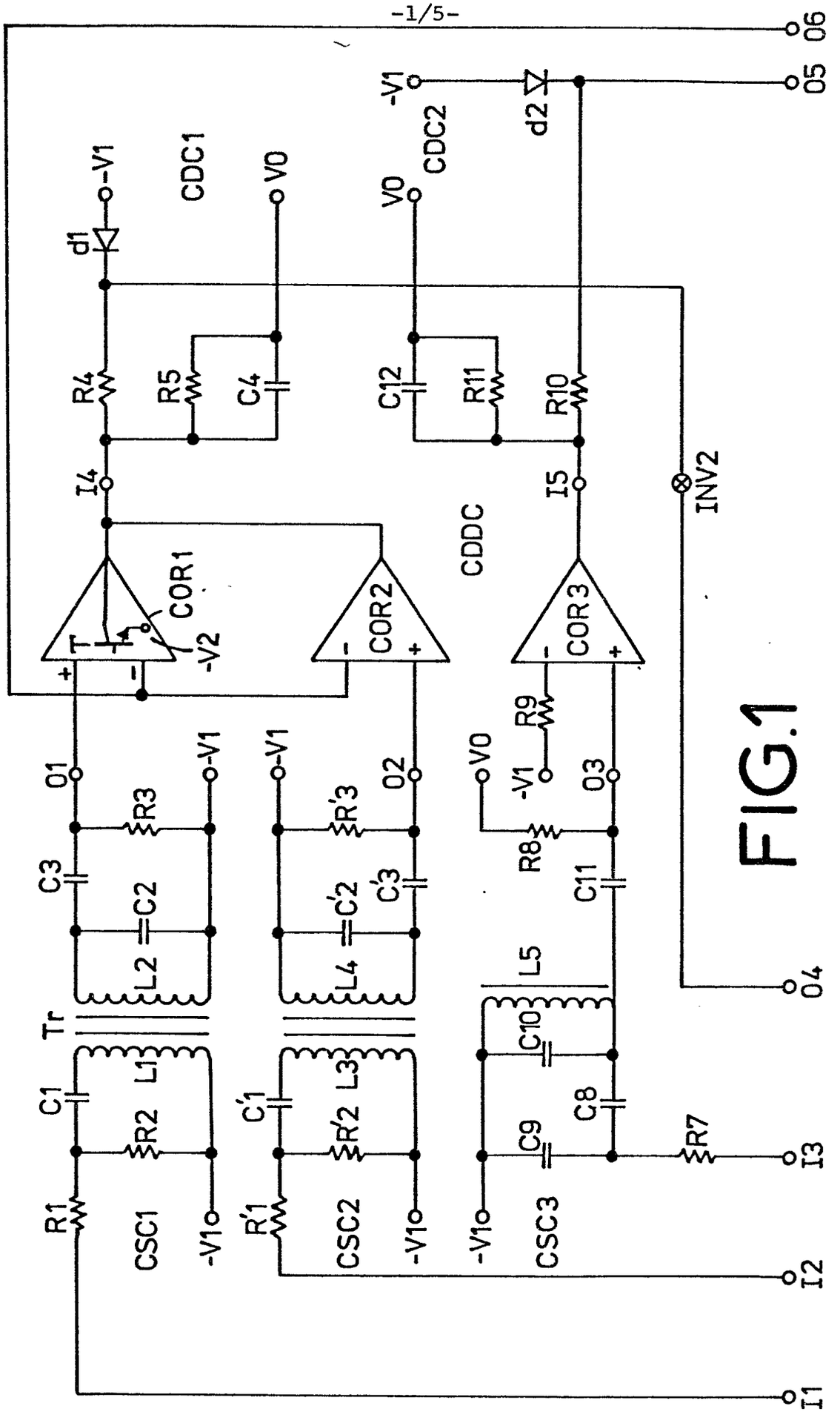
I1
I2
I3
I4
I5
O1
O2
O3
O4
O5
O6
-V1
V0
d1
d2
CDC1
CDC2
CDDC
INV2
COR1
COR2
COR3
T
-V2
R1
R2
R3
R4
R5
R7
R8
R9
R10
R11
R'1
R'2
R'3
C1
C2
C3
C4
C'1
C'2
C'3
C8
C9
C10
C11
C12
L1
L2
L3
L4
L5
Tr
CSC1
CSC2
CSC3
-V1o

FIG.1

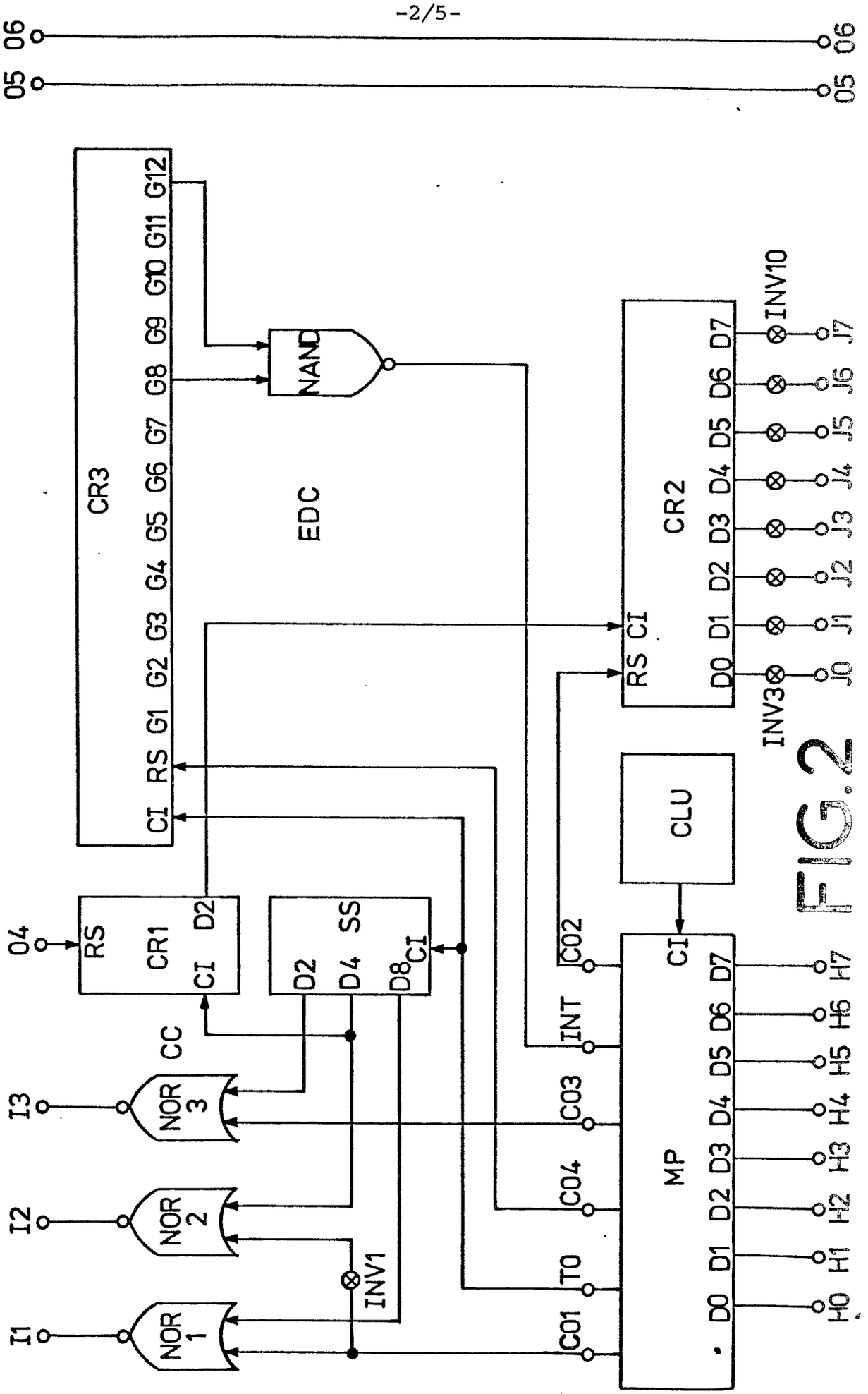
O6
O5
O6
O5
CR3
G12 G11 G10 G9 G8 G7 G6 G5 G4 G3 G2 G1
CI RS
EDC
NAND
CR2
D7 D6 D5 D4 D3 D2 D1 D0
RS CI
INV10
INV3
J7 J6 J5 J4 J3 J2 J1 J0
CLU
O4
RS
CR1
D2
CI
CC
SS
D2 D4 D8 CI
I3
I2
I1
NOR 3
NOR 2
NOR 1
INV1
C02
INT
C03
C04
T0
C01
CI
MP
D7 D6 D5 D4 D3 D2 D1 D0
H7 H6 H5 H4 H3 H2 H1 H0

FIG. 2

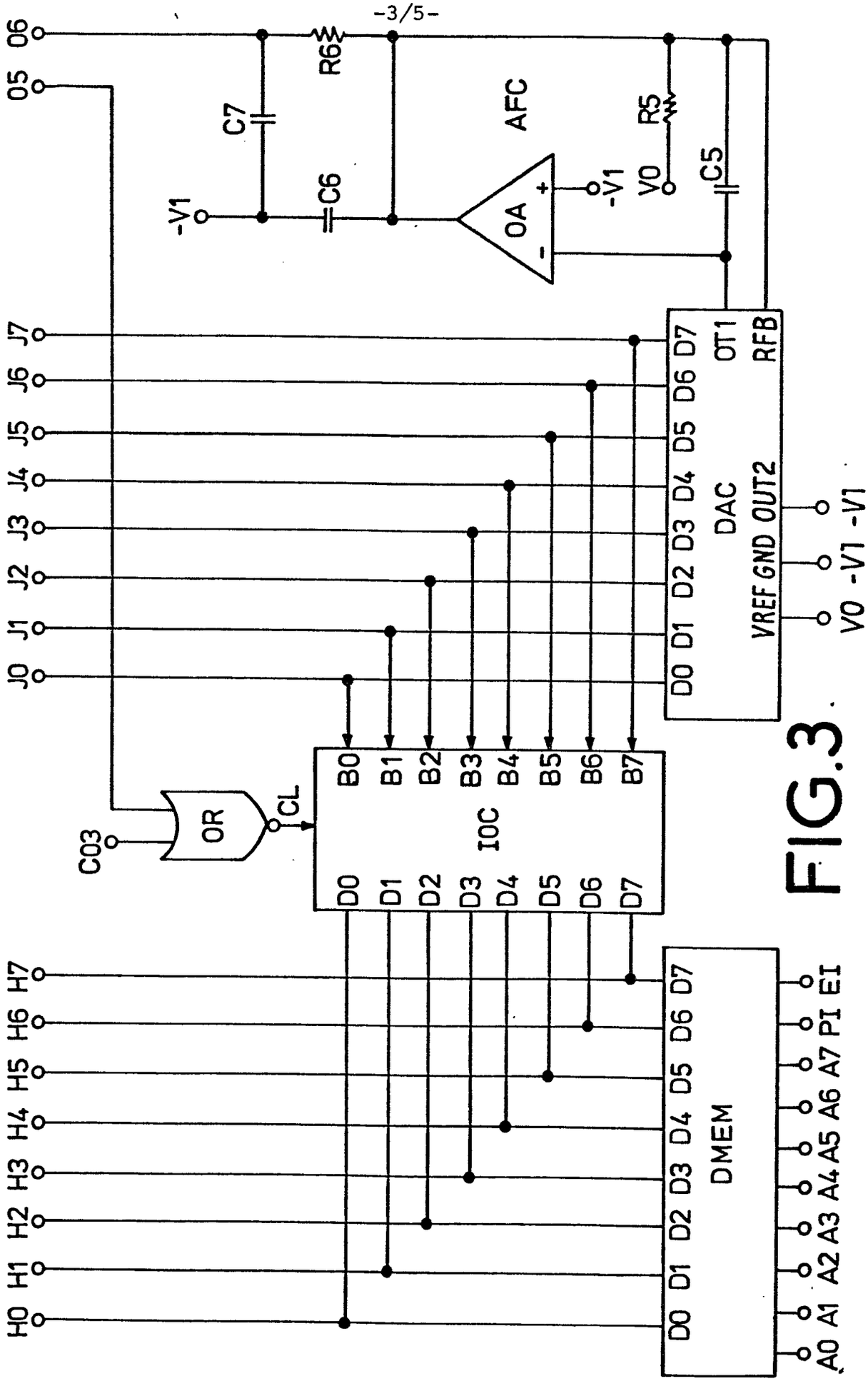
O6
O5
R6
C7
C6
-V1
AFC
OA
-V1
V0
R5
C5
J7
J6
J5
J4
J3
J2
J1
J0
D0 D1 D2 D3 D4 D5 D6 D7
OT1
RFB
DAC
VREF GND OUT2
V0 -V1 -V1
C03
OR
CL
B0 B1 B2 B3 B4 B5 B6 B7
IOC
D0 D1 D2 D3 D4 D5 D6 D7
H7
H6
H5
H4
H3
H2
H1
H0
D0 D1 D2 D3 D4 D5 D6 D7
DMEM
A0 A1 A2 A3 A4 A5 A6 A7 PI EI

FIG.3

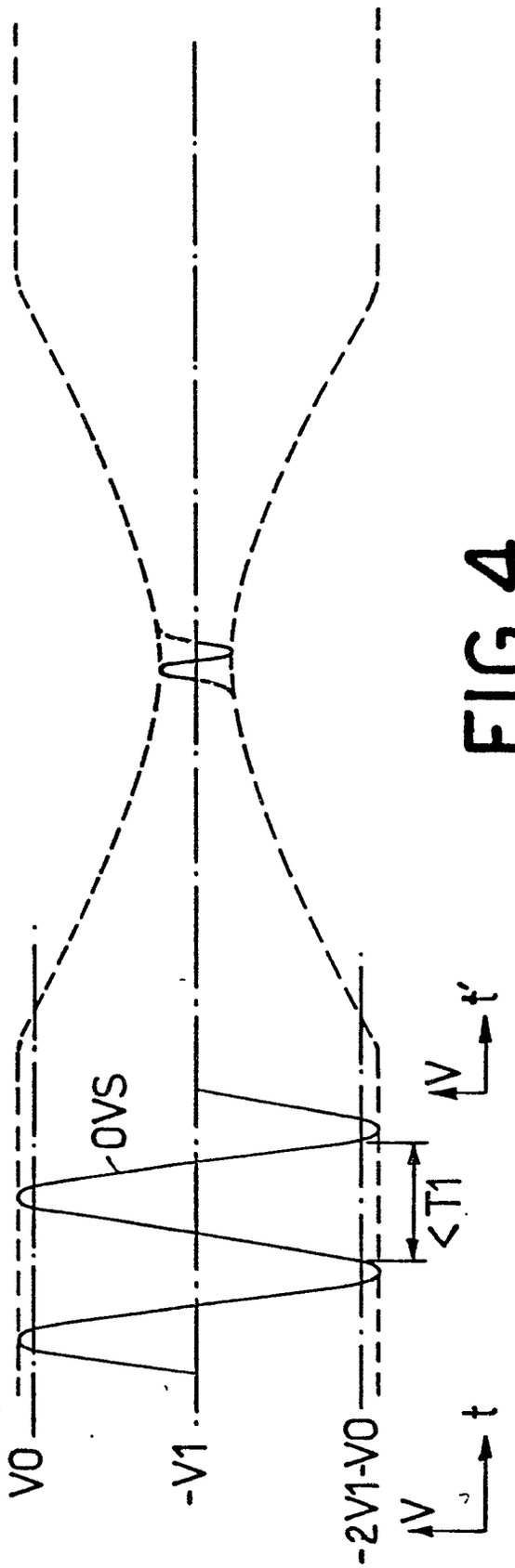

FIG. 4

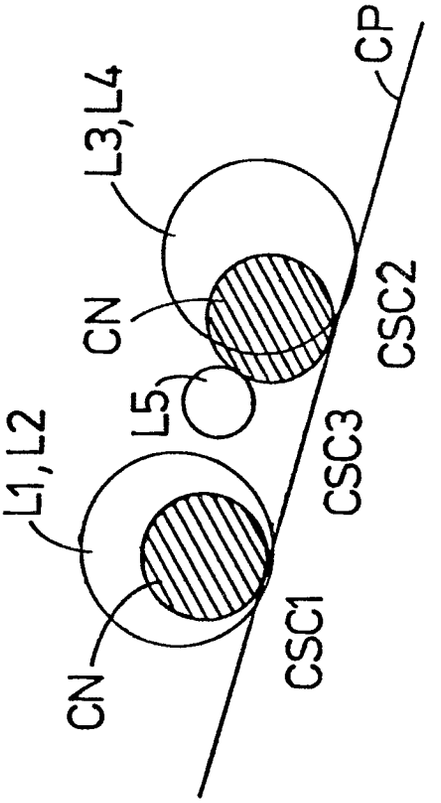

FIG. 5

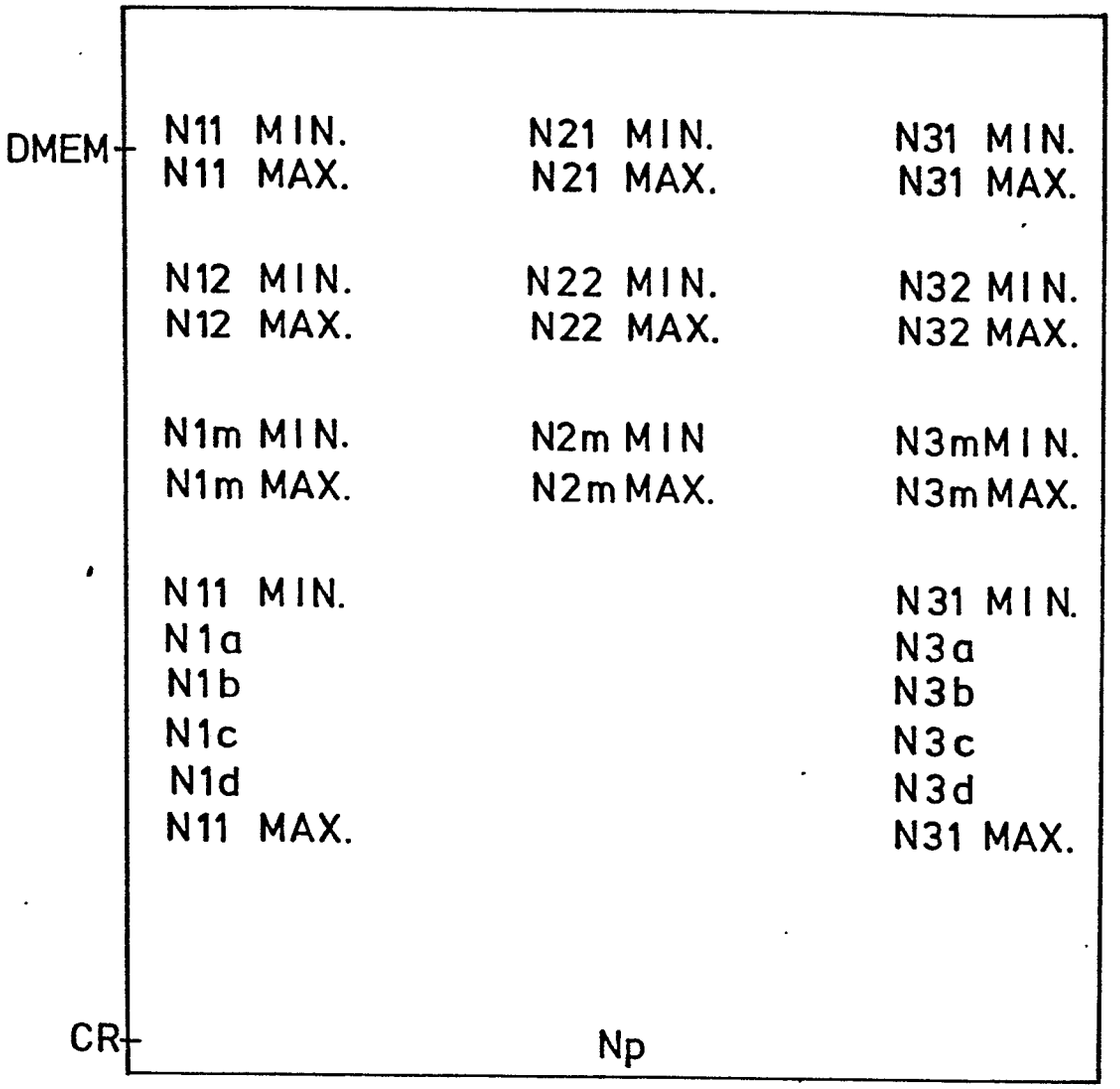
DMEM
N11 MIN.
N11 MAX.
N21 MIN.
N21 MAX.
N31 MIN.
N31 MAX.
N12 MIN.
N12 MAX.
N22 MIN.
N22 MAX.
N32 MIN.
N32 MAX.
N1m MIN.
N1m MAX.
N2m MIN
N2m MAX.
N3mMIN.
N3m MAX.
N11 MIN.
N1a
N1b
N1c
N1d
N11 MAX.
N31 MIN.
N3a
N3b
N3c
N3d
N31 MAX.
CR
Np

FIG.6

European Patent Office

EUROPEAN SEARCH REPORT

Application number EP 81 20 0602

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim
Y	FR - A - 2 359 468 (CROUZET) * Claims; figures; page 2, line 9 - page 3, line 9 *	1-3,5, 9,10, 14
Y	US - A - 3 869 663 (K. TSCHIERSE) * Abstract; figure 7; column 8, line 59 - column 9, line 9; figure 10 *	1-3,9, 14
Y	US - A - 4 108 296 (Y. HAYASHI) * Abstract; figures; column 1, line 30 - column 2, line 62 *	1-3,9, 10,14
A	US - A - 4 124 111 (Y. HAYASHI) * Abstract; figures, column 1, line 25 - column 2, line 4 *	1-3,9 10,14
A	US - A - 3 918 565 (G.L. FOUGERE) * Complete document *	1,9,10
A	US - A - 3 152 677 (W.C. PHILLIPS) * Figures; column 1, line 58 - column 2, line 9 *	1-3,5, 9
A	GB - A - 2 045 500 (MATSUSHITA) * Figures; Abstract; claims *	1-3,9 10,14

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CLASSIFICATION OF THE APPLICATION (Int. Cl. 3)

G 07 F 3/02
G 07 D 5/08

TECHNICAL FIELDS SEARCHED (Int.Cl. 3)

G 07 F 3/00
3/02
G 07 D 5/00
5/08

CATEGORY OF CITED DOCUMENTS

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E: earlier patent document, but published on, or after the filing date
D: document cited in the application
L: document cited for other reasons

&: member of the same patent family, corresponding document

X The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	18-03-1982	DAVID

EPO Form 1503.1 06.78

European Patent Office

EUROPEAN SEARCH REPORT

Application number

EP 81 20 0602

-2-

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int. Cl.³)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
A	DE - A - 2 213 376 (M. PRUMM) * Claims; pages 4-6; figures *	1-3,5, 9	

TECHNICAL FIELDS SEARCHED (Int. Cl.³)

EPO Form 1503.2 06.78