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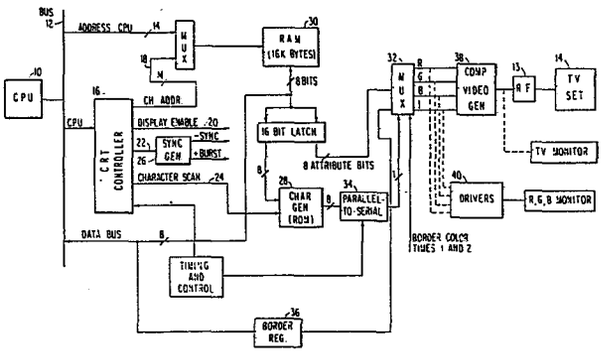
(54) Programmable border color for CRT of color TV.

(57) A central processing unit (10) loads a border register (36) with four color bits representing digital color signals to be used in determining the color of only the border area surrounding the video area of a cathode ray tube display screen (14). A BORDER CONTROL TIME signal is generated at the appropriate times in the horizontal and vertical scanning periods of the cathode ray tube to apply the digital color border signals (R, G, B, I) to a composite video signal generator (38) which generates the composite video signal for a TV set (14) or a TV monitor.



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PROGRAMMABLE BORDER COLOR FOR CRT OF COLOR TV

Description

Technical Field

This invention relates generally to color television systems and, more particularly, to a circuit for independently controlling the color of only the border around the video area of the screen of a TV receiver or monitor employing a cathod ray tube (CRT) display device.

Background of the Invention

In a cathod ray tube display devices used to display alphanumeric and graphic images in a data processing system, such as a small personal computer or computer-controlled TV game, it is often desirable to control the color of the border area surrounding the video or image area in order to make the total display more aesthetically pleasing or easier to view. The color of this border should be controlled independently of the color and data displayed in the video area of the CRT screen.

Controlling the color of the border around the video area of the display screen is different from controlling the color of the edge of an individual character (e.g. US Patent No. 3,984,828) or the color of the background of a displayed word (e.g. US Patent No. 3,911,418).

Summary of the Invention

In a data processing system, such as a small personal computer, a 4-bit software-loadable border register is provided which will independently determine the color of only the border area around the video raster zone of the CRT in a conventional television receiver or monitor. A border color

control signal is enabled through the same multiplexer or color video control unit that provides the video (data and color) information supplied to the video area of the CRT screen, but this control signal is enabled at pre-defined time intervals during the scanning of the screen such that the color of the border, only, is completely independent of the video information displayed on the screen. Up to sixteen colors are available for the border.

For a better understanding of the present invention, together with other and further advantages and features thereof, reference is made to the following description taken in connection with the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a block diagram of a portion of a data processing system, such as a personal computer, which generates a composite video color signal usable by a conventional NSTC television receiver or a monitor for displaying in the video area of the screen thereof alpha-numeric and graphic information in colors determined by digital color signals generated within the system, and which indludes the novel border register of this invention.

Figure 2 is a combined logic and circuit schematic diagram of the composite video generator of Figure 1.

Figure 3 illustrates the manner in which the border register contents are applied to the video information multiplexer for controlling the color of the border area around the video area of the CRT of the television receiver or a monitor.

Figure 4 is a timing diagram illustrating the pre-defined times at which the border color control signal is enabled in order to control the color of the complete border surrounding the filed area of a TV screen.

Figure 5 is a schematic diagram of a TV screen showing the "video" and "border" areas.

Detailed Description of the Preferred Embodiment

Figure 1 is a block diagram of a portion of a data processing system, such as a personal computer, in which alpha-numeric and graphic data, generated by a keyboard or other components of the system, are displayed on a cathode ray tube, such as a conventional television receiver or monitor.

A central processing unit (CPU) 10 is connected to a three-state system bus 12 including a 8-bit data bus. Let us assume that a character, such as one entered by a keyboard coupled to the bus, is to be displayed on the cathode ray tube (CRT) of a conventional TV receiver 14 designed in accordance with the National Television Standards Committee (NTSC) standards. A conventional CRT controller 16, such as a Motorola 6845 chip, controlled by CPU 10 via the bus 12, generates the CHARACTER ADDRESS on output line 18, CHARACTER SCAN on line 24, and the television frequency components on lines 20 and 22. There are produced on output line 22 the horizontal and vertical synchronizing pulses which are applied to a logic circuit (Figure 2) and to a sync generator 26 which produces -SYNC and +BURST signals. A DISPLAY ENABLE signal is produced on line 20, and the scanning pulses are produced on line 24 and applied to a character generator (ROM) 28. An 8-bit character code is fetched from a random access memory (RAM) 30 at the specified character address. An 8-bit attribute code is also fetched, and four of these bits designate the color of the character to be displayed, i.e., the foreground color of the character, as opposed to the background color of the character. The four character color bits are applied to a multiplexer (MUX) 32, such as a 74LS157 chip, which outputs the red (R), green (G), blue (B) and intensity (I) signals from which there is derived the composite video color signal to be applied to the TV receiver.

Multiplexer 32 is under the control of the serial character dots from the 8-to-1 parallel-to-serial converter 34 connected to the output of the character generator 28. The digital R, G, B and I signals on the output of multiplexer 32 are applied as inputs to a composite video generator 38 which produces the composite video color signal which can be used directly by a conventional composite monitor or, after being modulated by an R.F. modulator 13, by TV receiver 14 to display the colored character, or as inputs to the drivers 40 of a conventional direct drive TV monitor which operates directly from the R, G, B and I signals without the RF modulation required by the TV receiver 14, but which requires externally supplied synchronizing and blanking signals.

Figure 2 is a logic and schematic circuit diagram of the composite video generator 38 of Figure 1, and functions directly to convert the R, G, B and I digital color signals on the output of MUX 32 to a composite video color signal which can be utilized by the TV receiver 14 to display the character image having the color designated by a particular set of digital color signals. In the following description, a line is UP, i.e. has a logical value of 1 (+5 volts), when the indicated signal is present, and is DOWN, i.e. has the logical value of 0 (0 volt), when that signal does not exist.

The circuit of Figure 2 consists of three digital delay devices in the form of three 74LS74 edge-triggered D-type latches or flipflops 50, 52 and 54, each of which has a D input, a clock (CLK) input, a Q set output, and a $\bar{Q}$ reset output. The outputs of the three latches are connected as six inputs to an 8-to-1 74LS151 multiplexer 56 to whose output Y are switched, under the control of digital color signals B, G, R applied to its SELECT terminals A, B and C, respectively, individual ones of the eight phase-shifted color subcarriers appearing on the eight inputs of the multiplexer. The 0 input terminal of multiplexer 56 is grounded and represents the color black, and the white input is connected to +5 volts. The S (strobe) terminal of the multiplexer chip 56 is not used and is grounded.

A 14.318 MHz clock signal from the system bus is applied to the CLK terminal of latches 50 and 52, and inverted and applied to the CLK terminal of latch 54. The system clock signal is also divided by four in a frequency divider 58 to produce the 3.58 MHz (actually 3.5795) NTSC color subcarrier signal. A delay of one clock period of the 14.318 MHz signal corresponds to a 90° phase shift of the 3.58 MHz subcarrier. One-half of the 14.318 MHz clock period thus correspond to a 45° phase shift of the subcarrier. The Q or 0° phase output of latch 50 is applied to the D input of latch 52, and the Q or 90° delay output of latch 52 is applied to the D input of latch 54.

The subcarrier signal is synchronized by the rising edges of the clock signal. Because of the inherent delay between the inputs and the outputs of such D-type latches, the zero phase output of latch 50, for example, will be slightly delayed from its D input. Thus, when the Q output of latch 50 is applied to the D input of latch 52, it will no be up for the first rising edge of the clock signal which is also applied to latch 52. Thus, the outputs of latch 52 will be delayed by ninety degrees relative to those of latch 50. Similarly, a 45° phase shift occurs between the outputs of latches 52 and 54; that is, when the Q output of latch 52 goes high, the Q output of latch 54 will go high one-half of the 14.318 MHz period later to produce the 45° phase shift. The same operation occurs for the $\bar{Q}$ outputs of latches 52 and 54.

Thus, and as indicated by the legends in Figure 3, the two outputs of latch or flip-flop 50 provide a 3.58 MHz color subcarrier signal at both, 0° phase shift (yellow, brown, burst) and also 180° phase shift (blue, brigth blue). Latch 52 delays the 0° phase shift signal from latch 50 and provides a 3.58 MHz signal at 90° phase shift (red, pink) and at 270° phase shift (cyan, bright cyan). Latch 54 delays the 90° phase shift signal from latch 52 by 45°, and its outputs provide a 3.58 MHz signal at 135° phase shift (magenta, bright magenta) and at 315° phase shift (green, bright green).

The phase-shifted subcarriers at the output Y of multiplexer 56 are passed through a buffer 60 and a 2.2 K resistor to the summing node 62 connected to the base of an NPN emitter-follower transistor 64 whose emitter-resistor output contains the composite video color signal which is applied through R.F. modulator 13 to the input terminals of the TV receiver 14. Also connected to summing node 62 via corresponding buffer 66, 68 and 69 and corresponding summing resistors having ohmic values of 3.3K, 13K and 4.7K are the -SYNC and -BLANK signals from the CRT controller 16 and the +INTENSITY (I) signal from the color video control circuit or multiplexer 32 of Figure 1. It should be noted that the red, green, blue and intensity signals are forced low during blanking times. The OR gates 70 and 72 are used to select the 3.58 MHz 0° phase shift signal during BURST time to provide the color burst signal. The -SYNC signal is a composite of the horizontal and vertical synchronizing pulses. In the steady state condition, i.e. when the T.V. screen is black, the Y output is 0, -SYNC is 1, -BLANK is 1, and I is 0.

Following is a truth table showing the individual phase-shifted color signals which are outputted by multiplexer 56 for different combinations of the +BLUE, +GREEN and +RED signals on the multiplexer terminals A, B and C, respectively, and for I=0.

COLOR	A	B	C
Black	0	0	0
Red	0	0	1
Green	0	1	0
Yellow	0	1	1
Blue	1	0	0
Magenta	1	0	1
Cyan	1	1	0
White	1	1	1

When I=1, the complementary "brighter" colors are produced.

As shown in Figure 3, the CPU sends via the data bus a four bit data byte specifying the red, green, blue and intensity digital color signals for a particular one of the sixteen colors available for the border. The intensity signal represents a D.C. level which is applied to the composite video signal generator 38 to provide the "brighter" versions of the eight basic colors as described in detail with reference to Figure 2.

The contents of the border register 36 are gated to the multiplexer 32 at BORDER COLOR TIME via the CRT CONTROLLER 16 at predetermined time intervals during the horizontal and vertical scannings of the screen, which intervals are illustrated in the timing diagram of Figure 4. As shown there, at each BORDER COLOR TIME 1 the border areas 1 of the screen are "painted" the designated color, and at each BORDER COLOR TIME 2 the border areas 2 are painted.

Figure 5 is a pictorial representation of a TV screen 44 illustrating the video area 42 and border area 40 and the portions of the border area which are painted at times 1 and 2.

CLAIM

1. In a data processing system including a memory and a central processing unit for controlling a cathode ray tube controller via a data bus and also including a multiplexer for producing video information signals to display colored data in the video area of the display screen of a cathode ray tube, the circuit for providing independent control of the color of the border around the video area, characterized in that it comprises a border register, connected between the bus and the multiplexer, for receiving border color signals from the central processing unit, the multiplexer gating the signals to the color control circuits of the cathode ray tube at pre-defined times corresponding only to the border areas around the video area of the cathode ray tube screen.

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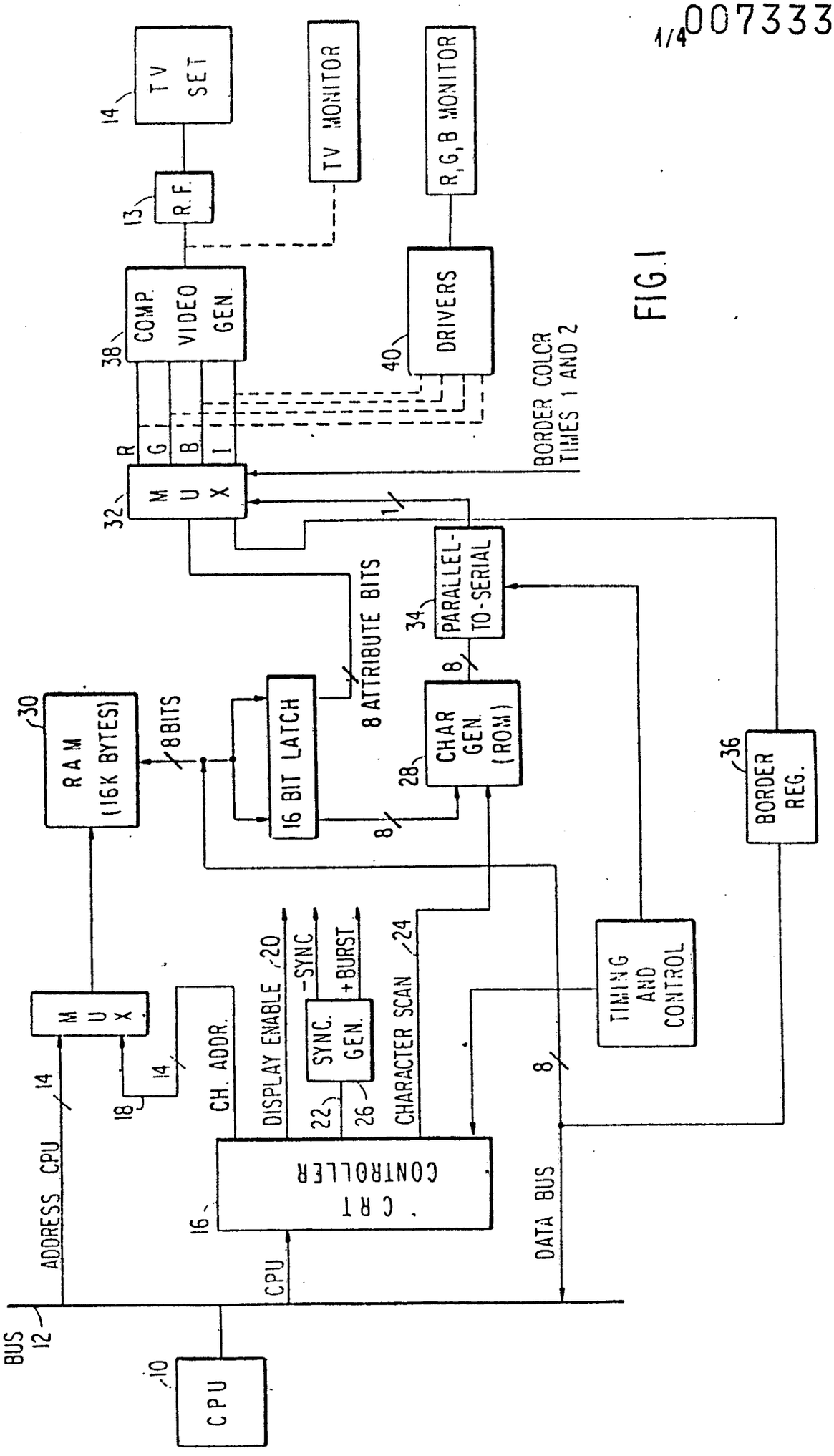
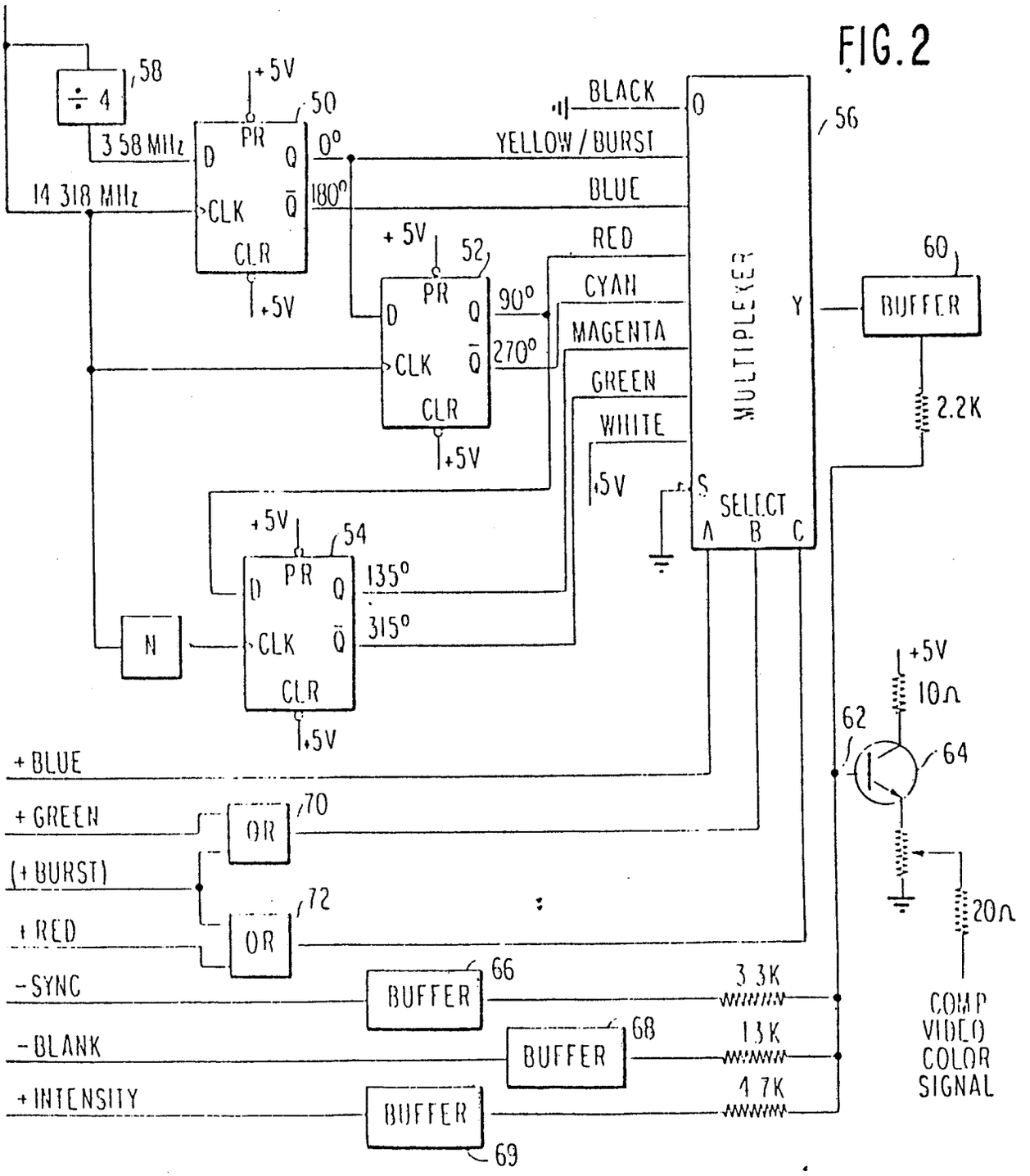


FIG.1

FIG.2


÷ 4
58
3.58 MHz
14.318 MHz
+5V
50
PR
D
Q
CLK
Q̄
CLR
0°
180°
+5V
+5V
52
PR
D
Q
CLK
Q̄
CLR
90°
270°
+5V
+5V
54
PR
D
Q
CLK
Q̄
CLR
135°
315°
+5V
N
BLACK
YELLOW / BURST
BLUE
RED
CYAN
MAGENTA
GREEN
WHITE
+5V
0
S
SELECT
A B C
MULTIPLEXER
Y
56
60
BUFFER
2.2K
+5V
10Ω
62
64
20Ω
COMP VIDEO COLOR SIGNAL
+BLUE
+GREEN
(+BURST)
+RED
-SYNC
-BLANK
+INTENSITY
OR
70
OR
72
BUFFER
66
BUFFER
68
BUFFER
69
3.3K
1.3K
4.7K

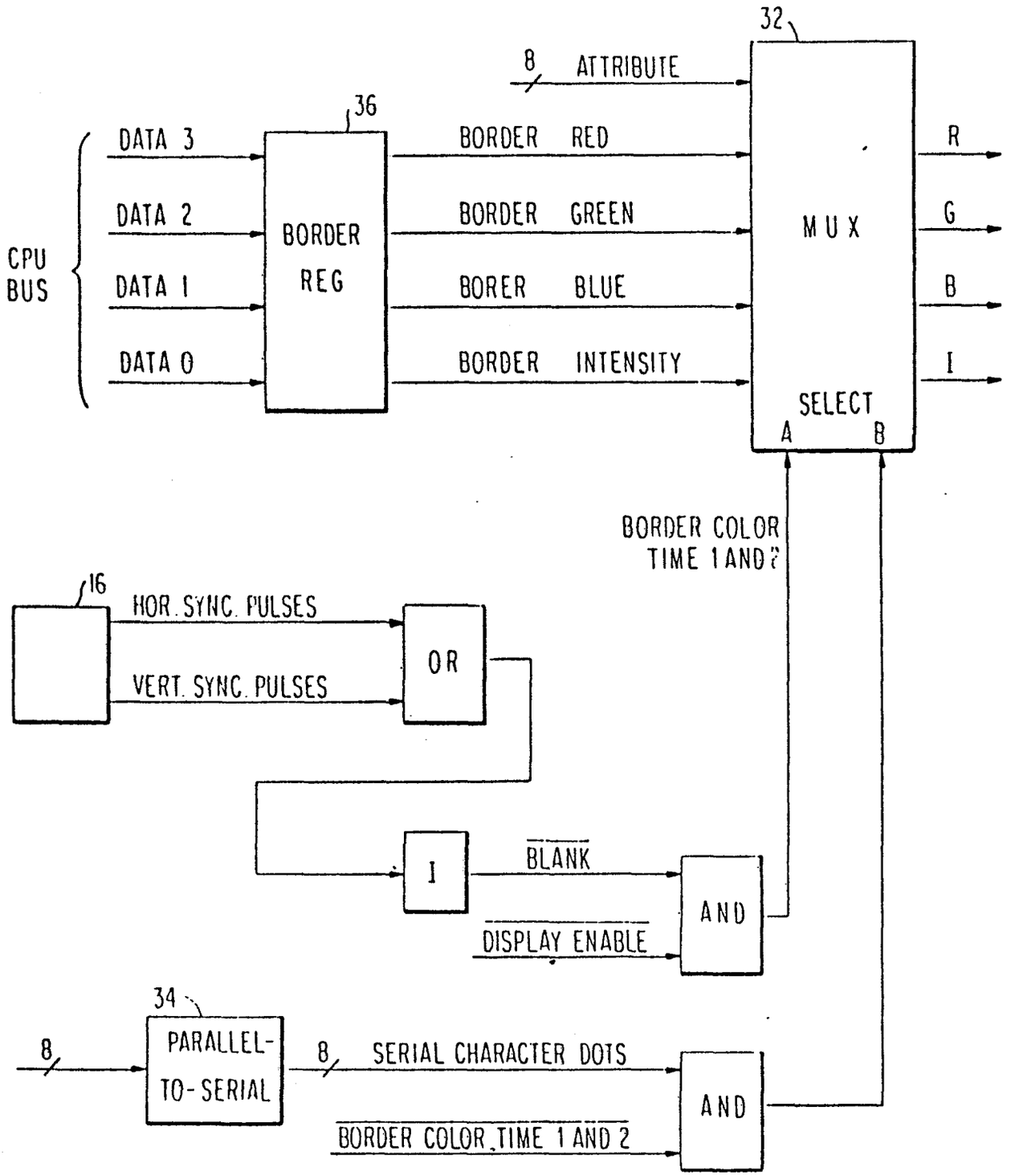

32
8 ATTRIBUTE
36
DATA 3
DATA 2
DATA 1
DATA 0
CPU BUS
BORDER REG
BORDER RED
BORDER GREEN
BORER BLUE
BORDER INTENSITY
MUX
R
G
B
I
SELECT
A
B
BORDER COLOR TIME 1 AND 2
16
HOR. SYNC. PULSES
VERT. SYNC. PULSES
OR
I
BLANK
DISPLAY ENABLE
AND
34
8
PARALLEL-TO-SERIAL
8 SERIAL CHARACTER DOTS
BORDER COLOR TIME 1 AND 2
AND

FIG.3

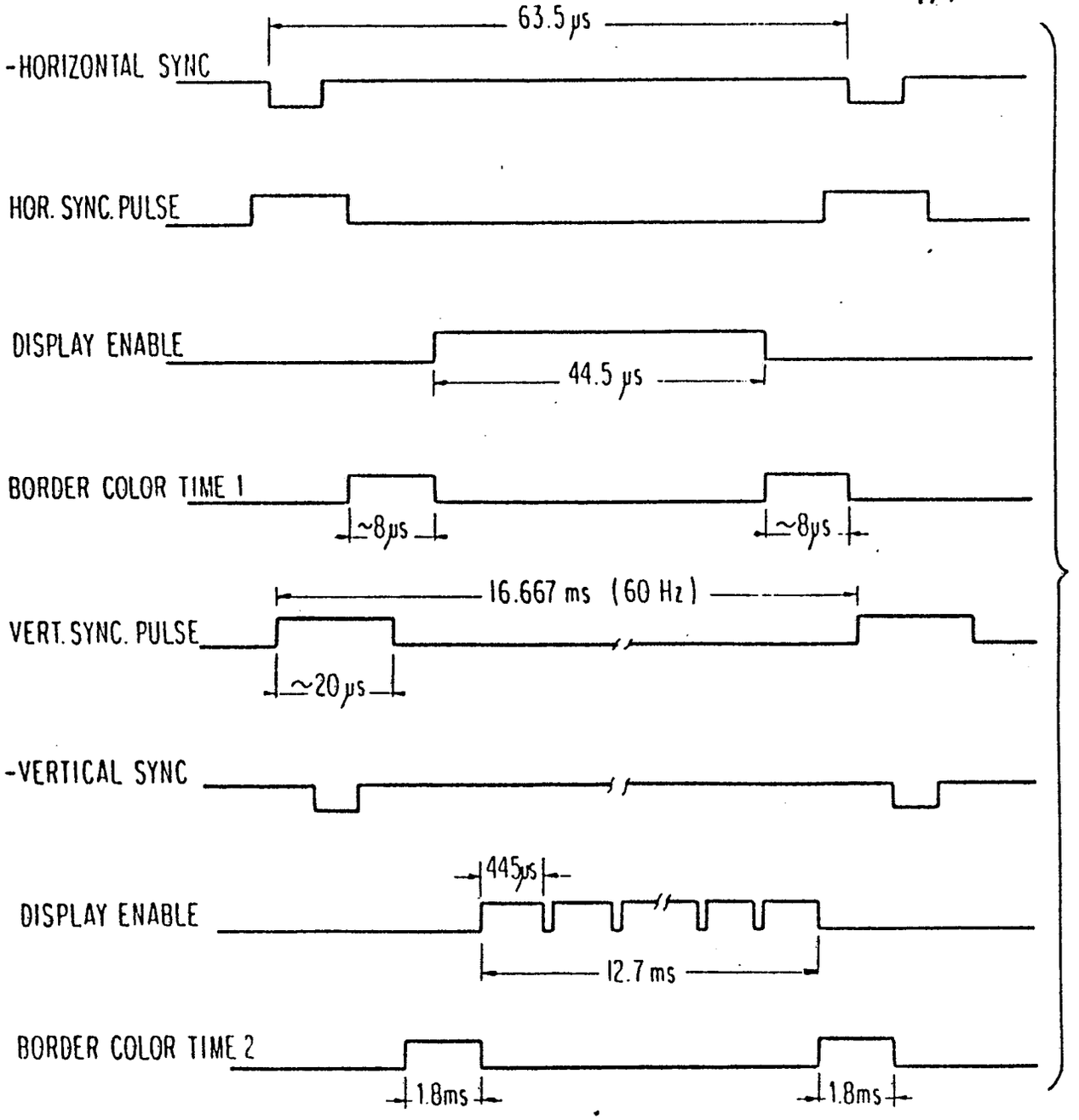

63.5 μs
-HORIZONTAL SYNC
HOR. SYNC. PULSE
DISPLAY ENABLE
44.5 μs
BORDER COLOR TIME 1
~8μs
~8μs
16.667 ms (60 Hz)
VERT. SYNC. PULSE
~20μs
-VERTICAL SYNC
445μs
DISPLAY ENABLE
12.7 ms
BORDER COLOR TIME 2
1.8ms
1.8ms

FIG.4

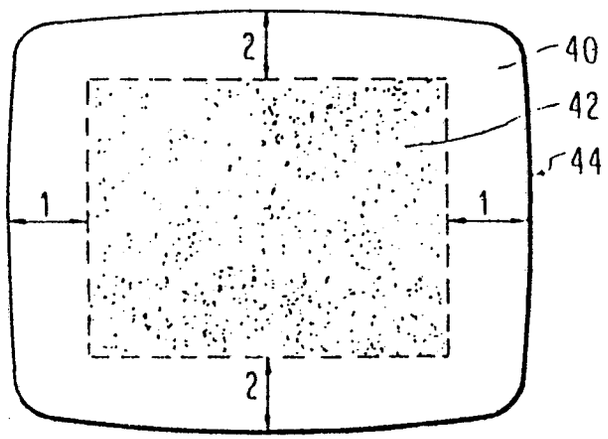

2
40
42
44
1
1
2

FIG.5