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(71) Applicant: International Business Machines Corporation

Armonk, N.Y. 10504(US)

(72) Inventor: Saenz, Jesus Andres
983 Ramblewood Dr.
Coral Springs Florida 33065(US)

(72) Inventor: Dean, Mark Edward
725 NW 4th Street
Boynton Beach Florida 33435(US)

(72) Inventor: Kummer, David Allen
18428 Alydar Way
Boca Raton Florida 33434(US)

(74) Representative: Vekemans, André
COMPAGNIE IBM FRANCE Département de Propriété Industrielle
F-06610 La Gaude(FR)

(64) Circuit for individually controlling the color of the font and background of a character displayed on a color tv receiver or monitor.

(67) An 8-bit character byte is fetched from a random access memory (30) and applied to a character generator (28). An associated 8-bit attribute bit is also fetched from the random access memory (30) and applied to the inputs of a multiplexer (32). Four of the attribute bits designate the color of the font of a character to be displayed on a TV set (14). The remaining four attribute bits designate the background color of the displayed character. The eight attribute bits are selectively gated to the outputs of the multiplexer (32) under the control of character serial dots from the parallel-to-serial converter (34) as red (R), green (G) and blue (B) digital color signals which are applied to a composite video signal generator (38) which produces a composite video color signal. The colors of the font and background of each individual character displayed on the TV set (14) thus are independently controlled by the font and background color bits.

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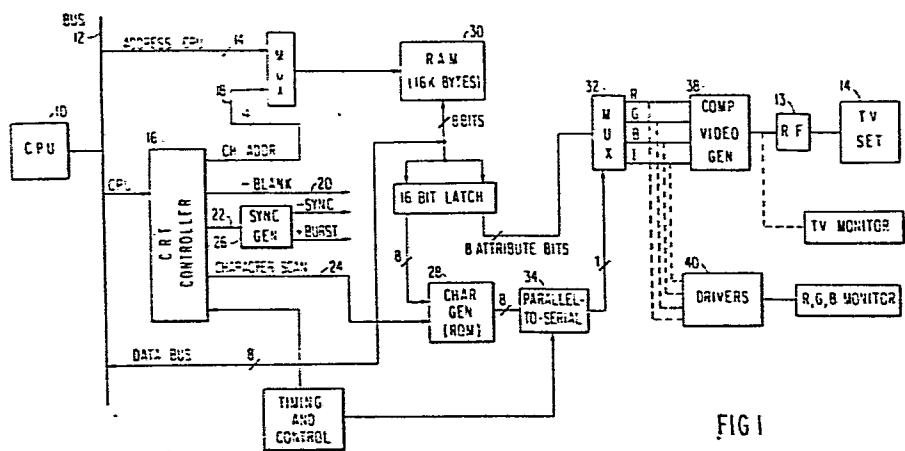


FIG 1

CIRCUIT FOR INDIVIDUALLY CONTROLLING THE COLOR
OF THE FONT AND BACKGROUND OF A CHARACTER DISPLAYED
ON A COLOR TV RECEIVER OR MONITOR

Description

Technical Field

This invention relates generally to color television, and, more particularly, to a circuit for independently controlling the colors of the font and background of a character displayed on the cathode ray tube (CRT) screen employed in a conventional television receiver or monitor as used in a data processing system, such as a small personal computer, for displaying computer-generated alpha-numeric and graphic data.

Background of the Invention

In a data processing system, such as a small personal computer, employing a conventional television receiver or a monitor for displaying characters in a color determined by computer-generated digital color signals, it is desirable independently to control both the color of the character font and character background in order to enhance the visual presentation of each character. Also, for security reasons or for playing certain TV games, it is desirable to have the capability of making a character invisible on the CRT display screen, even though the character code is being applied to the control circuitry of the CRT. Such a result could be achieved if it were possible to make the colors of both the font and background of the character the same.

In the prior art, e.g. US Patent 3,911,418, it is known independently to control the background color of a word consisting of a plurality of characters by inserting a background color code in the space between adjacent words; however, the background color of each single character cannot be controlled except in the special case where a word contains only one character. Furthermore, it is known to control the

color of the edge or border of each character differently from the body of the character, as shown in US Patent No. 3,984,828.

Summary of the Invention

In accordance with the present invention, in addition to the character code which is applied to the control circuits of the CRT for each character, there is also provided an 8-bit character attribute code which is applied to the existing multiplexer or color video control unit in the data processing system. One part of this attribute code is dedicated to the color of the font ("foreground") of each character, and the other part of the code is dedicated to the color of the background of the character, whereby the colors of both the font and background of each character within a word are independently controlled. The two portions of the code are independently selectable so that all possible combinations of font and background color are possible. In particular, if both the font and background colors are selected to be the same, the character which otherwise would be displayed on the CRT screen is invisible to a viewer.

For a better understanding of the present invention, together with other and further advantages and features thereof, reference is made to the following description taken in connection with the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a block diagram of a portion of a data processing system, such as a small personal computer, in which computer-generated digital color signals are used to control the color of alpha-numeric and graphic data displayed on the screen of a conventional TV receiver or monitor.

Figure 2 is a combined logic and circuit schematic diagram of the composite video generator of Figure 1.

Figure 3 illustrates the manner in which the color attribute byte is applied to the video information multiplexer to produce the independent font and background digital color signals.

Figure 4 is a timing diagram illustrating the times, within a character block, at which the respective font color and background color control signals are generated for a particular character.

Detailed Description of the Preferred Embodiment

Figure 1 is a block diagram of a portion of a data processing system, such as a personal computer, in which alpha-numeric and graphic data, generated by a keyboard or other components of the system, are displayed on a cathode ray tube, such as a conventional television receiver or monitor.

A central processing unit (CPU) 10 is connected to a three-state system bus 12 including a 8-bit data bus. Let us assume that a character, such as one entered by a keyboard coupled to the bus, is to be displayed on the cathode ray tube (CRT) of a conventional TV receiver 14 designed in accordance with the National Television Standards Committee (NTSC) standards. A conventional CRT controller 16, such as a Motorola 6845 chip, controlled by CPU 10 via the bus 12, generates the CHARACTER ADDRESS on output line 18, CHARACTER SCAN on line 24, and the television frequency components on lines 20 and 22. There are produced on output line 22 the horizontal and vertical synchronizing pulses which are applied to a sync generator 26 which produces -SYNC and +BURST signals. A -BLANK signal is produced on line 20, and the scanning pulses are produced on line 24 and applied to a character generator (ROM) 28. An 8-bit character code is fetched from a random access memory (RAM) 30 at the specified character address. An 8-bit attribute code is also fetched, and four of these bits designate the color of the character to be displayed, i.e.,

the foreground color of the character, as opposed to the background color of the character. The four character color bits are applied to a multiplexer (MUX) 32, such as a 74LS157 chip, which outputs the red (R), green (G), blue (B) and intensity (I) signals from which there is derived the composite video color signal to be applied to the TV receiver.

Multiplexer 32 is under the control of the serial character dots from the 8-to-1 parallel-to-serial converter 34 connected to the output of the character generator 28. The digital R, G, B and I signals on the output of multiplexer 32 are applied as inputs to a composite video generator 38 which produces the composite video color signal which can be used directly by a conventional composite monitor or, after being modulated by an R.F. modulator 13, by TV receiver 14 to display the colored character, or as inputs to the drivers 40 of a conventional direct drive TV monitor which operates directly from the R, G, B and I signals without the RF modulation required by the TV receiver 14, but which requires externally supplied synchronizing and blanking signals.

Figure 2 is a logic and schematic circuit diagram of the composite video generator 38 of Figure 1, and functions directly to convert the R, G, B and I digital color signals on the output of MUX 32 to a composite video color signal which can be utilized by the TV receiver 14 to display the character image having the color designated by a particular set of digital color signals. In the following description, a line is UP, i.e. has a logical value of 1 (+5 volts), when the indicated signal is present, and is DOWN, i.e. has the logical value of 0 (0 volt), when that signal does not exist.

The circuit of Figure 2 consists of three digital delay devices in the form of three 74LS74 edge-triggered D-type latches or flipflops 50, 52 and 54, each of which has a D input, a clock (CLK) input, a Q set output, and a $\bar{Q}$ reset output. The outputs of the three latches are connected as six inputs to an 8-to-1 74LS151 multiplexer 56 to whose output Y

are switched, under the control of digital color signals B, G, R applied to its SELECT terminals A, B and C, respectively, individual ones of the eight phase-shifted color subcarriers appearing on the eight inputs of the multiplexer. The 0 input terminal of multiplexer 56 is grounded and represents the color black, and the white input is connected to +5 volts. The S (strobe) terminal of the multiplexer chip 56 is not used and is grounded.

A 14.318 MHz clock signal from the system bus is applied to the CLK terminal of latches 50 and 52, and inverted and applied to the CLK terminal of latch 54. The system clock signal is also divided by four in a frequency divider 58 to produce the 3.58 MHz (actually 3.5795) NTSC color subcarrier signal. A delay of one clock period of the 14.318 MHz signal corresponds to a 90° phase shift of the 3.58 MHz subcarrier. One-half of the 14.318 MHz clock period thus correspond to a 45° phase shift of the subcarrier. The Q or 0° phase output of latch 50 is applied to the D input of latch 52, and the Q or 90° delay output of latch 52 is applied to the D input of latch 54.

The subcarrier signal is synchronized by the rising edges of the clock signal. Because of the inherent delay between the inputs and the outputs of such D-type latches, the zero phase output of latch 50, for example, will be slightly delayed from its D input. Thus, when the Q output of latch 50 is applied to the D input of latch 52, it will not be up for the first rising edge of the clock signal which is also applied to latch 52. Thus, the outputs of latch 52 will be delayed by ninety degrees relative to those of latch 50. Similarly, a 45° phase shift occurs between the outputs of latches 52 and 54; that is, when the Q output of latch 52 goes high, the Q output of latch 54 will go high one-half of the 14.318 MHz period later to produce the 45° phase shift. The same operation occurs for the $\bar{Q}$ outputs of latches 52 and 54.

Thus, and as indicated by the legends in Figure 3, the two outputs of latch or flip-flop 50 provide a 3.58 MHz color subcarrier signal at both, 0° phase shift (yellow, brown, burst) and also 180° phase shift (blue, bright blue). Latch 52 delays the 0° phase shift signal from latch 50 and provides a 3.58 MHz signal at 90° phase shift (red, pink) and at 270° phase shift (cyan, bright cyan). Latch 54 delays the 90° phase shift signal from latch 52 by 45°, and its outputs provide a 3.58 MHz signal at 135° phase shift (magenta, bright magenta) and at 315° phase shift (green, bright green).

The phase-shifted subcarriers at the output Y of multiplexer 56 are passed through a buffer 60 and a 2.2 K resistor to the summing node 62 connected to the base of an NPN emitter-follower transistor 64 whose emitter-resistor output contains the composite video color signal which is applied through R.F. modulator 13 to the input terminals of the TV receiver 14. Also connected to summing node 62 via corresponding buffer 66, 68 and 69 and corresponding summing resistors having ohmic values of 3.3K, 13K and 4.7K are the -SYNC and -BLANK signals from the CRT controller 16 and the +INTENSITY (I) signal from the color video control circuit or multiplexer 32 of Figure 1. It should be noted that the red, green, blue and intensity signals are forced low during blanking times. The OR gates 70 and 72 are used to select the 3.58 MHz 0° phase shift signal during BURST time to provide the color burst signal. The -SYNC signal is a composite of the horizontal and vertical synchronizing pulses. In the steady state condition, i.e. when the T.V. screen is black, the Y output is 0, -SYNC is 1, -BLANK is 1, and I is 0.

Following is a truth table showing the individual phase-shifted color signals which are outputted by multiplexer 56 for different combinations of the +BLUE, +GREEN and +RED signals on the multiplexer terminals A, B and C, respectively, and for I=0.

<u>COLOR</u>	<u>A</u>	<u>B</u>	<u>C</u>
Black	0	0	0
Red	0	0	1
Green	0	1	0
Yellow	0	1	1
Blue	1	0	0
Magenta	1	0	1
Cyan	1	1	0
White	1	1	1

When I=1, the complementary "brighter" colors are produced.

Figure 3 shows the eight color attribute bits applied to the inputs of the 74LS151 multiplexer 32 to produce the red (R), green (G), blue (B) and intensity (I) digital color signals which are applied to the composite video generator 38 to produce the video composite color signal as described in detail with reference to Figure 2. The intensity signal (I) produces a D.C. level which produces "brighter" versions of the eight colors which are derived from the three basic colors of blue, green and red. The eight character color attribute bits (four font or foreground color bits and four background color bits) are applied to the inputs of the multiplexer 32 and are selectively switched to the output lines of the multiplexer under the control of the serial character dots from the parallel to serial converter 34.

Figure 3 illustrates the format of the eight bit attribute code which is fetched from the RAM 30 and applied to the multiplexer 32.

Figure 4 illustrates the relative timing of the foreground (font) and the background color signals in the horizontal and vertical scanings of a CRT for a typical 7x7 character block for the character "A". The shaded areas represent font or foreground times, and the unshaded areas represent background times.

The attribute byte also can be used to render a character invisible on the display screen by choosing the foreground (font) and background colors to be the same. In the prior art, a separate DON'T DISPLAY code and hardware were required to prevent display of a character.

CLAIMS

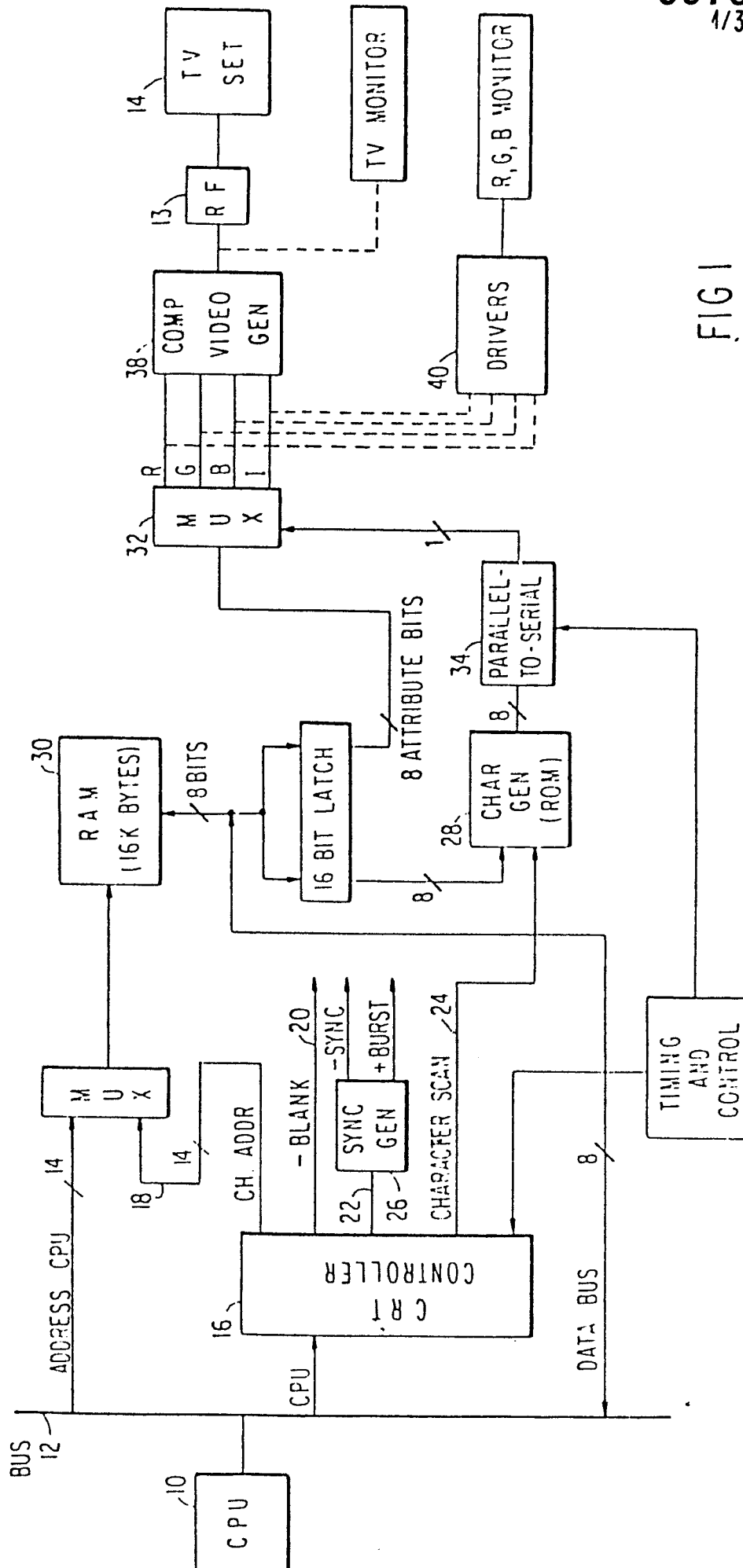
1. In a data processing system including a memory and a central processing unit for controlling a cathode ray tube controller via a data bus and also including a multiplexer for producing video information signals to display colored data on a display screen of a cathode ray tube in a television receiver or monitor, a circuit for providing independent control of the colors of the font and background displayed on the tube characterized in that it comprises :

means for fetching from the random access memory a character code and an associated character attribute code containing character font color bits and character background bits;

means for applying to the multiplexer serial character dots selectively to gate the font color bits and background color bits to a composite video signal generator to produce a composite video color signal; and

means to apply said composite video signal generator to the cathode ray tube to display thereon a character having font and background colors in accordance with the gated bits.

2. The improvement of claim 1 further comprising means for making said font and background color bits identical to each other.



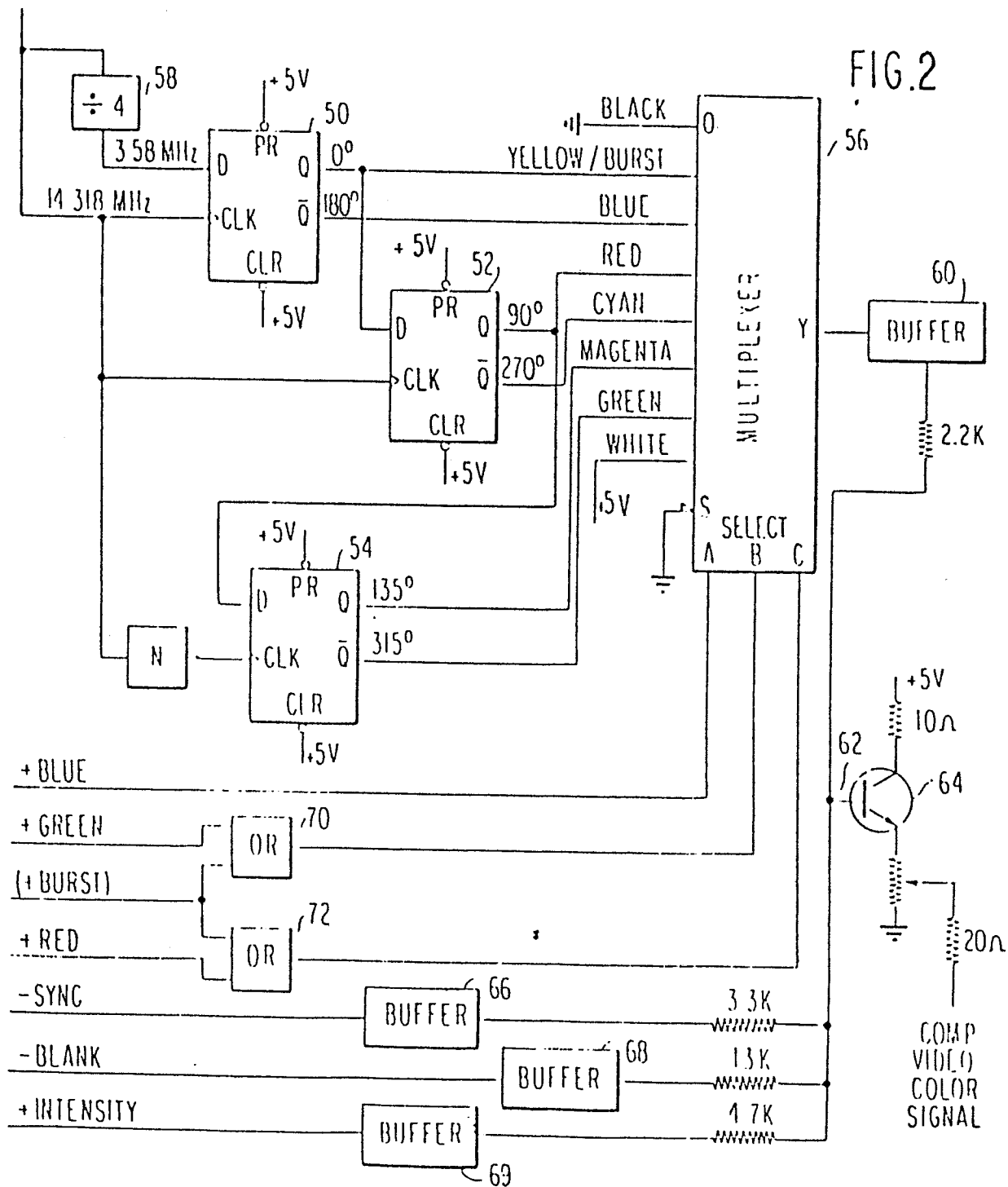


FIG. 3

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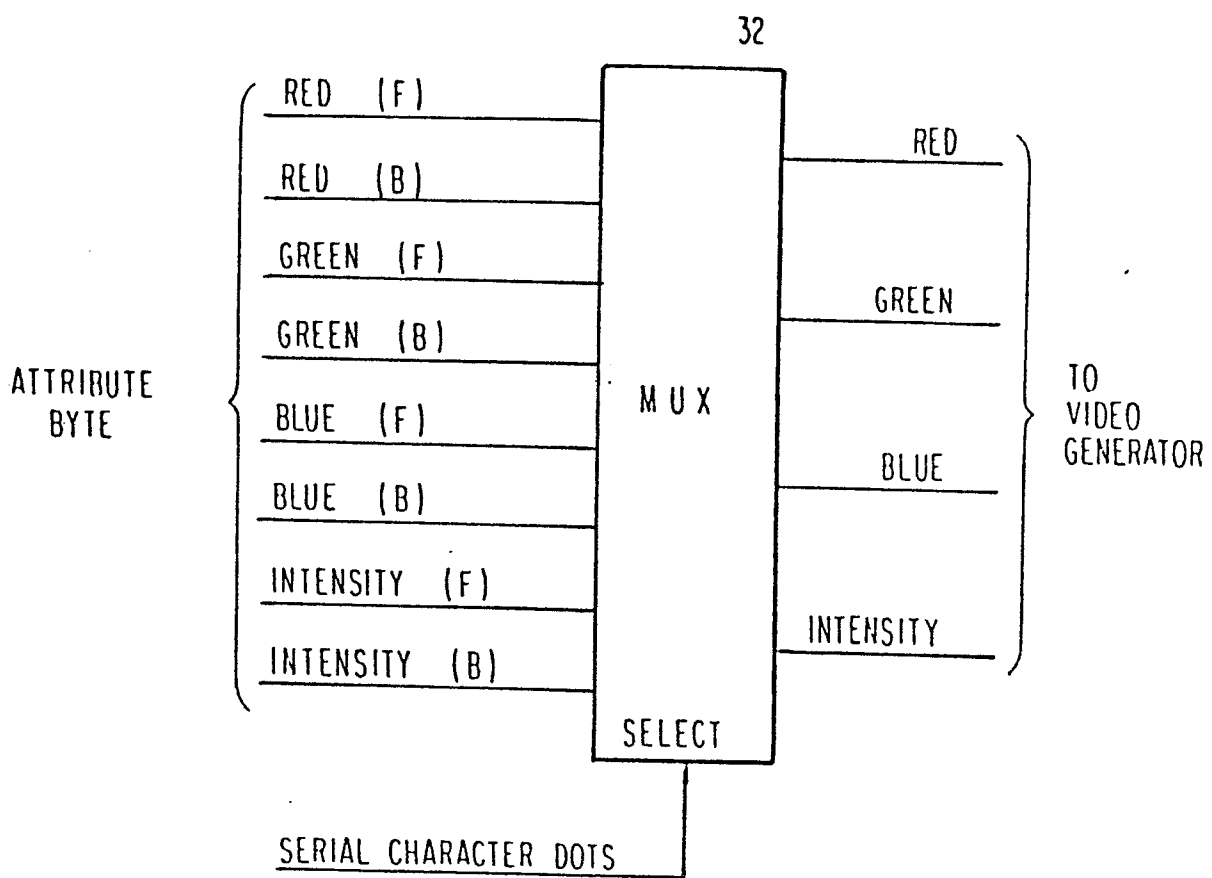
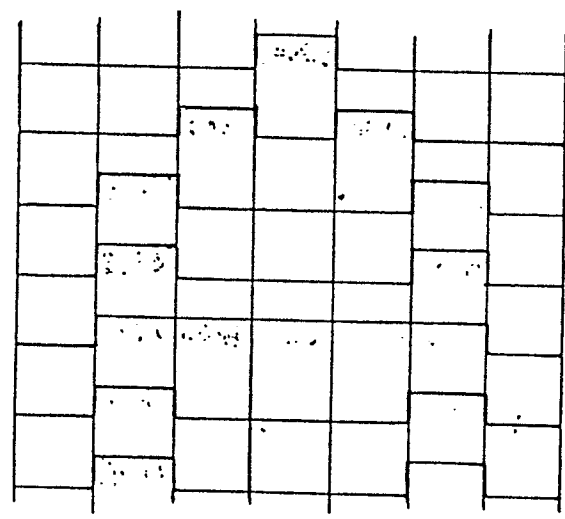


FIG. 4



SHADED ZONES = FOREGROUND COLOR
UNSHADED ZONES = BACKGROUND COLOR