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(54) Mains-wired monitoring and security system.

(57) A mains-wired monitoring and security system comprises an electric supply mains network (10) having connected thereto a control unit (Figure 1), a plurality of detecting units (Figure 2), and a plurality of actuating units (Figure 3). Each unit includes associated counter means (5, 15, 29) controlled in synchronism with each other. Each detecting unit transmits a coded signal (f2) along the mains network when an associated sensor (14) detects an alarm condition and its associated counter means (15) simultaneously counts a specific number N. At least one actuating unit activates an associated actuator (37) in response to said coded signal if its associated counter simultaneously counts the number N. The central unot visually displays said number N, which is common to at least one detecting unit and at least one actuating unit, in response to said coded signal.

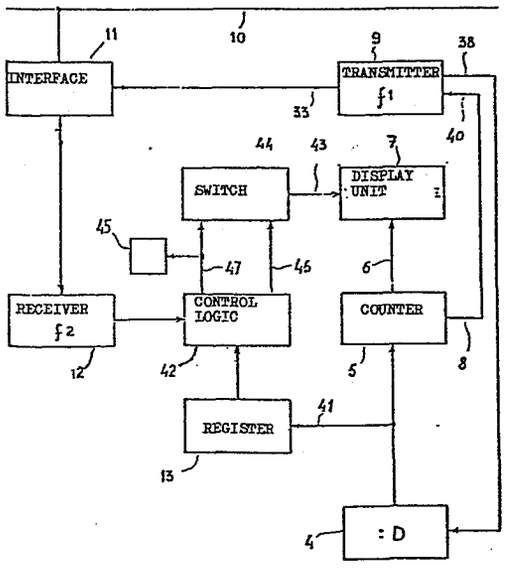

Fig. 1

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Mains-Wired Monitoring and Security System

This invention relates to a mains-wired system for monitoring predetermined zones spaced throughout a building, for instance residential premises, and for automatically initiating suitable action on the occurrence of an alarm condition.

Known mains-wired monitoring and security systems, i.e. systems employing the electric supply mains network for signal transmission, comprise a sensor, for example a temperature sensor, adapted to transmit to a remote location an alarm signal for energizing a suitable actuator. Systems of this type are not able, however, to monitor and to distinguish from one another a plurality of zones spaced throughout a building. For this purpose one usually employs systems having a plurality of sensors of different types, such as incendiary sensors, innundation sensors, break-in sensors and the like,

connected to associated actuators by means of additional wiring provided along with the electrical supply mains network, whereby the installation and operation of the entire system is undesirably complicated. Alternatively, the sensors may be connected to the associated actuators through special transmission systems, such as infrared radiation transmission systems, whereby the problems of the additional wiring is avoided. Such systems, however, require the employ of sophisticated and expensive transmitting and receiving equipment, whereby the overall construction of the system is again complicated and its operation rendered less reliable.

In any case the correct operation of such known systems necessarily requires that all of their components as well as the connections between sensors and associated actuators are always in perfect working condition. On the other hand, any fault in the connections of the system does not become immediately apparent, so that in the case of an alarm condition the system can fail to react altogether or may even react in an incorrect manner.

It is therefore an object of the invention to provide a mains-wired monitoring and security system of a relatively simple construction and reliable operation, which may be employed for monitoring a plurality of zones and for controlling a plurality of actuators spaced throughout a building.

A further object of the invention is to provide a monitoring and security system of the type indicated above, which is capable of giving timely warning of any malfunction of its main components and/or connections within the system itself.

In accordance with the invention, these objects are attained by a mains-wired monitoring and security system comprising an electric supply mains network to which

there are connected at least one central control unit, a plurality of peripheral detector units, and a plurality of peripheral actuating units. This system is principally characterized in that each unit comprises counter means adapted to cyclically count up to a count of M under the control of synchronizing means. Each peripheral detector unit is adapted to transmit via said mains network a code signal, when an associated sensor detects an alarm condition and the associated counter means arrive at a specific count N at the same time. At least one peripheral actuating unit is adapted to activate an associated actuator in response to the coded signal if the counter means associated therewith is simultaneously at the count N, this specific count N being common to at least one detector unit and at least one actuating unit. The central control unit is adapted to visually display the counted number N in response to said coded signal.

The number N is preferably smaller than or equal to M/2, each of the peripheral detector units being further adapted to transmit the said coded signal via the mains network whenever the associated counter means reach a specific count of N + M/2. The central control unit comprises memory means for storing the specific numbers N + M/2 for each of the peripheral detector units, said memory means being controlled by said synchronizing means for cyclically reading these specific numbers and for actuating a display device if, on reading one of the specific numbers N + M/2, the central unit detects the absence of the corresponding coded signal.

The characteristics and advantages of the invention will become more clearly evident from the following description of an exemplary embodiment with reference to the accompanying drawings, wherein:

figs. 1 to 3 show block diagrams of individual units connected to each other through an electric supply mains network in a preferred embodiment of a monitoring and security system according to the invention.

With reference to fig. 1, the system comprises a central control unit preferably provided with an independent power supply (not shown). The central unit includes a carrier wave transmitter 9 comprising an oscillator and a comparator (known and therefore not shown). Transmitter 9 is adapted to continuously generate a synchronizing signal having a frequency f1 (for instance 100 kc), which is applied to output terminal 38. In a per se known manner, transmitter 9 is adapted to apply the synchronizing signal also to a further output terminal 39 as long as a logic enable signal is present at its input terminal 40.

Output terminal 39 of transmitter 9 is connected to an electric supply mains network 10 of a building through an interface 11 adapted to stay the mains voltage.

Output 38 of transmitter 9 controls a frequency divider 4 having adividing proportion of D = f1/f0 (for instance equal to 1000 in the example described), wherein f0 (equal to 100 c/sec) is the frequency of the output signal of frequency divider 4, said output signal being employed for the timing control of the system as will be described hereinafter.

The output of frequency divider 4 is applied to a counter stage 5 comprising for instance two four-bit counters in the form for instance of respective integrated circuits CD 4029 made by RCA. Counter stage 5 is adapted to cyclically count up to a maximum number M (for instance M = 128) and is in a per se known manner designed so as to present two successive counting sequences from 0 to

M/2 to its main output 6 during each counting cycle T = 1.28 seconds. Counter stage 5 has a further output 8 to which it applies a logic enable signal (level "1") for the duration of one counting step (i.e. 10 msec in the example described) whenever the maximum count M is attained. Output 8 of counter stage 5 is connected to input 40 of transmitter 9, while counter outputs 6 are applied to respective inputs of a display device for instance of the luminous diode (LED) type.

The central unit further comprises a signal receiver 12, the input of which is connected to mains network 10 through interface 11, while its output in the form of a logic signal controls a corresponding input of a logic control stage 42. In particular, receiver 12 normally generates a logic level "0" at its output, said output changing to logic level "1" when receiver 12 detects a coded signal at its input which, as will be explained in detail later, has a fequency f2 (e.g. 80 Kc).

Logic stage 42 has a further input connected to the output of a configuration memory 13 consisting for example of two integrated circuits CD 4031 made by RCA and constituting a shift register having a total of M memory locations. In a per se known manner, shift register 13 is initially programmed by storing the presence or absence of individual peripheral units of the system to be described later at corresponding memory locations. In the described example, the absence of peripheral units will be stored at the first sixty-four locations, while the presence of peripheral units will be stored in corresponding ones of the second group of sixty-four locations. The control input 41 of register 13 is connected to the output of frequency divider 4, so that the 128 locations of the register will be cyclically scanned with the frequency f0 in synchronism with counter stage 5. Register 13 is adapted to generate a logic level "1" at its output only on the scanning of

memory locations having stored therein the presence of at least one peripheral detecing unit.

Logic control stage 42 may be composed of a plurality of commercially available logic elements and is provided with two outputs 46 and 47 alternatingly activated by successive counts of M/2. Output 46 is activated during the count from 0 to M/2 for generating the same logic level as present at the output of receiver 12. Output 47 is activated during the count from M/2 to M to generate a logic level "1" only if there is a difference between the logic levels at the outputs of receiver 12 and register 13. Output 47 of stage 42 is additionally adapted to activate an indicator device 45 when at level "1".

An enable input 43 of display device 7 is selectively activated via a manually operable switch 44 or via one of the outputs 46 or 47 of stage 42. In every case that a logic level "1" is present at input 43, display device 7 is activated to display the count (between 0 and M/2) actually present at the outputs of counter stage 5.

The monitoring and security system according to the invention further includes a plurality of peripheral detector units, preferably provided with independent power supply (not shown), each one of which having the construction as shown in fig. 2 and being located at any point of the building to be monitored. As will be explained in the following, each peripheral detector unit is identified by a specific number $N \leq M/2$ which may also be common to a group of such units.

With reference to fig. 2, each peripheral detector unit comprises a detecting device 14 including a sensor (not shown) which may be of a per se known type and/or of different type for each such unit as required. The sensor may thus for example be a gas leak sensor, a break-in

sensor, an inundation sensor, an incendiary sensor or the like. The output of detector 14 is normally at the logic level "0" and is adapted to change to level "1" whenever the sensor is activated by detecting an alarm condition. Each peripheral detector unit further comprises a counter stage 15 which may be composed of three four-bit counters of the type CD 4029 made by RCA. Conter stage 15 is programmed in a per se known manner to cyclically count up to the number M = 128 and to generate a logic enable signal (logic level "1") at an output 16 (normally at logic level "0") whenever the count of $N \leq M/2$ is reached. Counter stage 15 is in addition programmed to generate a logic command signal (logic level "1") at an output 17 (normally at logic level "0"), whenever the count of $N + M/2$ is reached. The said enable and command signals are generated at the respective outputs 16 and 17 of counter stage 15 for the duration of one counting step, i.e. for 10 msec in the example described. As already explained above, each peripheral unit may be identified by a different number N.

The output of detector 14 and the output 16 of conter stage 15 are connected to respective inputs of a comparator stage 18, consisting for instance of an AND gate, arranged to generate an output command signal (logic level "1") in response to the simultaneous presence of logic level "1" at its inputs. Output 17 of counter stage 15 and the output of comparator 18 are applied to the command input of a per se known carrier wave transmitter 19, comprising for instance an oscillator for generating a coded signal having, as already explained above, a frequency f2 = 80 Kc/sec in response to the presence of logic level "1" at its command input. The output of transmitter 19 is connected to mains network 10 through an interface unit 20 adapted to stay the mains voltage.

Each peripheral detecting unit further includes a carrier wave receiver 21 the input of which is connected to mains network 10 through interface unit 20.

Receiver 21 is substantially composed of a phase-locked loop circuit (PLL) which may be in the form of an integrated circuit of the type CD 4046 made by RCA. In a per se known manner receiver 21 is adapted to generate at its output 22 a reset signal which is applied to a reset input of counter stage 15 in response to receiving the already mentioned synchronization signal having the frequency f1 at its input. Also in a known manner, the phase-locked loop circuit of receiver 21 is controlled by the periodically received synchronization signal (received for each counting cycle T) for continuously generating a signal having the synchronization frequency f1 at a further output 23. The latter is applied to a counting input 25 of counter stage 15 through a frequency divider 24 having a dividing coefficient D = f1/f0, i.e. 1000 in the example described. The counting input 25 of counter stage 15 is thus controlled with the frequency f0 and thus in synchronism with the counter 5 of the central unit shown in fig. 1.

The monitoring and security system according to the invention further includes a plurality of peripheral actuating units, preferably provided with independent power supply (not shown), each of which is designed as shown in fig. 3 and located at any suitable point of a building to be monitored. As will be explained in the following, each actuating unit is identified by a specific number N which may be common to a plurality of actuating units and/or to one or a plurality of peripheral detecting units. One or several detecting units may be associated with one or several actuating units as required.

With reference to fig. 3, each peripheral actuating unit is provided with a carrier wave receiver 26, the input of

which is connected to mains network 10 through an interface unit 27 adapted to stay the mains voltage.

Receiver 26 is identical to receiver 21 of fig. 2 and may thus be comprised of an integrated circuit of the type CD 4046 made by RCA.

In particular, receiver 26 is adapted to generate at its output 28 a reset signal which is applied to a corresponding input of a counter stage 29 in response to receiving the synchronization signal having the frequency f1 at its input. In addition, the phase-locked loop circuit of receiver 26 is controlled by the periodically received synchronization signal (received once for each counting cycle T, as already explained) to continuously generate a synchronization signal having the frequency f1 at a further output 30. Output 30 of receiver 26 is applied to a counting input 31 of counter stage 29 through a frwquency divider 34 having the same dividing coefficient $D = f1/f0$ as frequency divider 24 of fig. 2. Thus the counting input 31 of counter stage 29 is also controlled with the frequency f0, i.e. in synchronism with the counter stage 5 of the central control unit.

Counter stage 29 may be constituted by two four-bit counters of the type CD 4029 made by RCA, analogous to counter stage 5 of fig. 1.

In a per se known manner, counter stage 29 is programmed to cyclically count up to the number M and to generate at an output 32 a logic enable signal (logic level "1") each time it reached the count N.

As already said, the number $N - M/2$ may be different for each peripheral unit.

The peripheral actuating units each include a further carrier wave receiver 33, the input of which is connected

to mains network 10 through interface 27. Receiver 33 may likewise be formed, analogously to receiver 12 of fig. 1, by an integrated circuit of the type CD 4046 made by RCA, and is adapted to generate at its output 35 a command signal (for example logic level "1") which is applied to a corresponding input of a comparator and integrator stage 36 in response to receiving the coded signal having the frequency f2 at its input.

Stage 36 is of a per se known type and adapted to store (for instance by means of a load capacitor (not shown)) the command signal received from receiver 33 whenever the enable signal is simultaneously present at the output of counter 29.

In addition, stage 36 is adapted to generate an activating output signal for an associated actuator 37 whenever it has stored the above mentioned command signal for a predetermined number of times (for instance three times) within a predetermined period of time.

Actuator 37 may be of any type adapted to the specific purpose corresponding to the number N identifying the respective actuating unit and thus the type of the sensor provided in the at least one peripheral detecting unit indentified by the same number N. Actuator 37 may thus for instance comprise a solenoid valve adapted to interrupt the supply of a combustible gas or to activate an anti-incendiary sprinkler system, apparatus for closing fireproof doors, an alarm siren or the like.

In operation of the system, counter 5 of the central Unit (fig. 1) counts progressively with the frequency f0 determined by frequency divider 4. On attaining the count of M, output 8 of counter 5 enables transmitter 9 to generate at irs output the synchronization signal having the frequency f1 for a duration of 10 msec. This signal is applied to mains network 10 through interface 11 and thus

to all of the peripheral detecting and actuating units shown in figs. 2 and 3, resepctively.

In each peripheral detecting unit the synchronization signal is received, through interface unit 20, by the respective receiver 21, causing the latter to reset counter 15 by way of its output 22 and to generate at its output 23 a timing signal in synchronism with the frequency f1, as already explained. Receiver 21 thus controls counter 15 with the frequency f0 through frequency divider 24; after each reset operation (carried out each time the count of M is attained, as already explained, and effective to periodically eliminate any irregularity in the function of counter 15) counter 15 is in step with the timing signal generated by frequency divider 4 of the central unit.

As counter stage 15 attains the count of N, it generates at its output 16 the logic level "1" which, only in case that sensor 14 be activated by an alarm condition, enables comparator 18 to activate transmitter 19. This means that if sensor 14 is active at the time that the count of N is attained, transmitter 19 applies the coded signal with the frequency f2 to mains network 10 for the duration of one counting step.

In an analogous manner, transmitter 19 generates the same coded signal at its output, irrespective of the condition of sensor 14 and unter the control of output 17 of counter 15, each time the said counter attains the count of $N + M/2$, it being supposed that each peripheral detecting unit provided within the system is identified by a different number $N \leq M/2$.

Each complete counting cycle from 0 to M (having a duration T of 1.28 sec in the example described) is divided into two periods of equal duration: a first counting period from 0 to M/2, and a second period for counting

from M/2 to M, said periods being designates T1 and T2, respectively.

During the period T1, coded signals having the frequency f2 are transmitted along mains network 10 only if at least one detecting unit is activated by an alarm condition; in this case the code signal is transmitted along the mains network at the instant at which the count of N identifying the activated detecting unit is attained.

During the period T2 (which, as will become more clearly evident in the following, is employed for carrying out an auto-diagnosis of the system), a plurality of code signals having the frequency f2 are transmitted along mains network 10 in timed succession. Each of these code signals is generated by a different detecting unit at the instance at which the count of N identifying the respective unit is attained.

With reference to fig. 1, it is now supposed that switch 44 normally connects input 43 of display device 7 with output 46 of logic stage 42.

If during the period T1 the central control unit receives a coded signal having the frequency f2 (indicative of an alarm condition of a detecting unit N), receiver 12 generates a logic signal "1" which is applied to the input 43 of display device 7 through output 46 of stage 42 and switch 44. Display device 7 is thereby caused to display, for repetitive periods of 10 msec each, the counted number present at outputs 6 of counter 5, which corresponds to the number N indentifying the activated detecting unit. This periodic display continues until the cause for the alarm condition has been remedied, and allows the cause of the alarm to be immediately recognized.

During the period T2, and as long as the entire system

functions correctly, the central control unit receives coded signals having the frequency f2 each time register 13 generates at its output the logic level "1", while at output 47 of stage 42 there is normally present a logic level "0".

If, at the time that register 13 generates the logic output level "1", receiver 12 does not receive a coded signal, the absence of this signal is indicative of a malfunction existing in the components and/or connections of a corresponding peripheral detecting unit. Under these conditions, the output of receiver 12 is at logic level "0", while output 47 of stage 42 is at logic level "1", thereby activating signalling or indicating device 45. The user is thus warned of the existing condition of malfunction and may now actuate switch 44 for connecting input 43 of display device 7 with output 47 of logic stage 42, causing display device 7 to display, for repetitive periods of 10 msec each, the count appearing at the outputs 6 of counter 5 and corresponding to the number N identifying the peripheral detecting unit beset by the malfunction. This enables the user to intervene in good time for remedying the cause of the malfunction.

As regards the peripheral actuating units (fig. 3), the synchronizing signal having the frequency f1 is received through interface unit 27 by receiver 26, causing the latter to reset counter 29 through its output 28 and to generate at its output 30 a signal in step with the frequency f1, as already said. Receiver 26 thus controls counter 29 through frequency divider 34 with the frequency f0; after each reset operation (carried out each time the count of M is attained and employed for periodically eliminating any irregularity in the function of counter 29), the counter 29 is in step with the timing signal generated by frequency divider 4 of the central unit.

If during the counting period T1 receiver 33 detects the

presence of a coded signal having the frequency f2 in the mains network 10, it generates a command signal at its output, as already indicated.

This command signal, however, is able to activate comparator 36 only if counter 29 simultaneously generates an enable signal at its output 32. This means that only the peripheral actuating unit, or units, respectively, identified by the same number N as the detecting unit generating the coded signal, is or are able to store the command signal in its or their comparator-integrator 36. Only if the command signal repeats itself over the above noted period of time for a predetermined number of complete counting cycles (three in the example described), does comparator 36 activate actuator 37 as already described above. This permits unnecessary and unwanted activation of actuator 37 caused for instance by faults in the mains network to be avoided and ensures such activation to take place only under genuine alarm conditions, thus contributing to the reliability of the entire system.

If receiver 33 detects command signal during the autodiagnosis period T2, comparator 36 can obviously not be activated, as output 32 of counter 29 is at logic level "0" as already stated. In every case, the entire system functions also in the absence of voltage in the mains network 10, thanks to its independent power supply.

The above description clearly shows the structural simplicity and operational reliability of the monitoring and security system according to the invention, in which the central unit and the peripheral units operate in synchronism, and in which the peripheral units are cyclically scanned during alternating alarm signal periods and autodiagnosis periods.

The described system may obviously varied in any suitable

manner within the scope and spirit of the invention. It is thus obvious to the skilled artisan that with slight modifications of the circuitry the peripheral actuating units may also be provided with means for carrying out an autodiagnosis analogous to those provided for the detecting units (transmitter 19 and associated connections in fig. 2).

In addition, the timing control of the monitoring and security system may be directly derived from mains network 10; in this case, frequency dividers 4, 24 and 34 are simply replaced by per se known mains voltage zero passage detectors.

Mains-Wired Monitoring and Security System

Patent Claims

1. Mains-wired monitoring and security system, comprising an electric supply mains network having connected thereto at least one central control unit, a plurality of peripheral detecting units, and a plurality of peripheral actuating units, characterized in that each said unit includes associated counter means adapted to cyclically count up to a number M under the control of synchronization means,, each peripheral detecting unit (fig. 2) being adapted to transmit a coded signal (f2) along said mains network (10) when an associated sensor (14) detects an alarm condition and the associated counter means (15) simultaneously count an associated number N. at least one peripheral actuating unit (fig.3) being adapted to activate an associated actuator (37)

in response to said coded signal when its associated counter means (29) simultaneously count the same specific number N, said number N being common to at least one detecting unit and at least one actuating unit, said central unit (fig. 1) being adapted to visually display said number N in response to said coded signal.

2. Monitoring and security system according to claim 1, characterized in that said synchronization means comprise a transmitter (9) in said central unit, adapted to control the associated counter means (5) with a synchronization signal (f1) and to transmit said synchronization signal along said mains network (10) at each count of said number M, each said peripheral detecting unit and actuating unit comprising a carrier wave receiver (21, 26) adapted to reset the associated counter means (15, 29) in response to said synchronization signal (f1) and to control said counter means with said synchronization signal.

3. Monitoring and security system according to claim 1, characterized in that the actuator (37) of each peripheral actuating unit is adapted to be activated through comparator-integrator means (36) having a first input (35) controlled by a command signal of an alarm receiver (33) in response to said coded signal (f2), and a second input (32) controlled by said associated counter means (29) at each count of the respective number N, with an enable signal permitting said command signal to be stored.

4. Monitoring and security system according to claim 1, characterized in that said number N is smaller than or equal to M/2, each peripheral detecting unit being adapted to transmit said coded signal (f2) along said mains network (10) each time the associated counter means (15) count a specific number N + M/2, said central unit being provided with memory means (13) for storing said numbers

N + M/2 of all peripheral detecting units, said memory means being controlled by said synchronization means for cyclically reading said numbers and for actuating a warning device (45) if the central unit detects the absence of said coded signal (f2) at the instant of reading one of said numbers N +M/2.

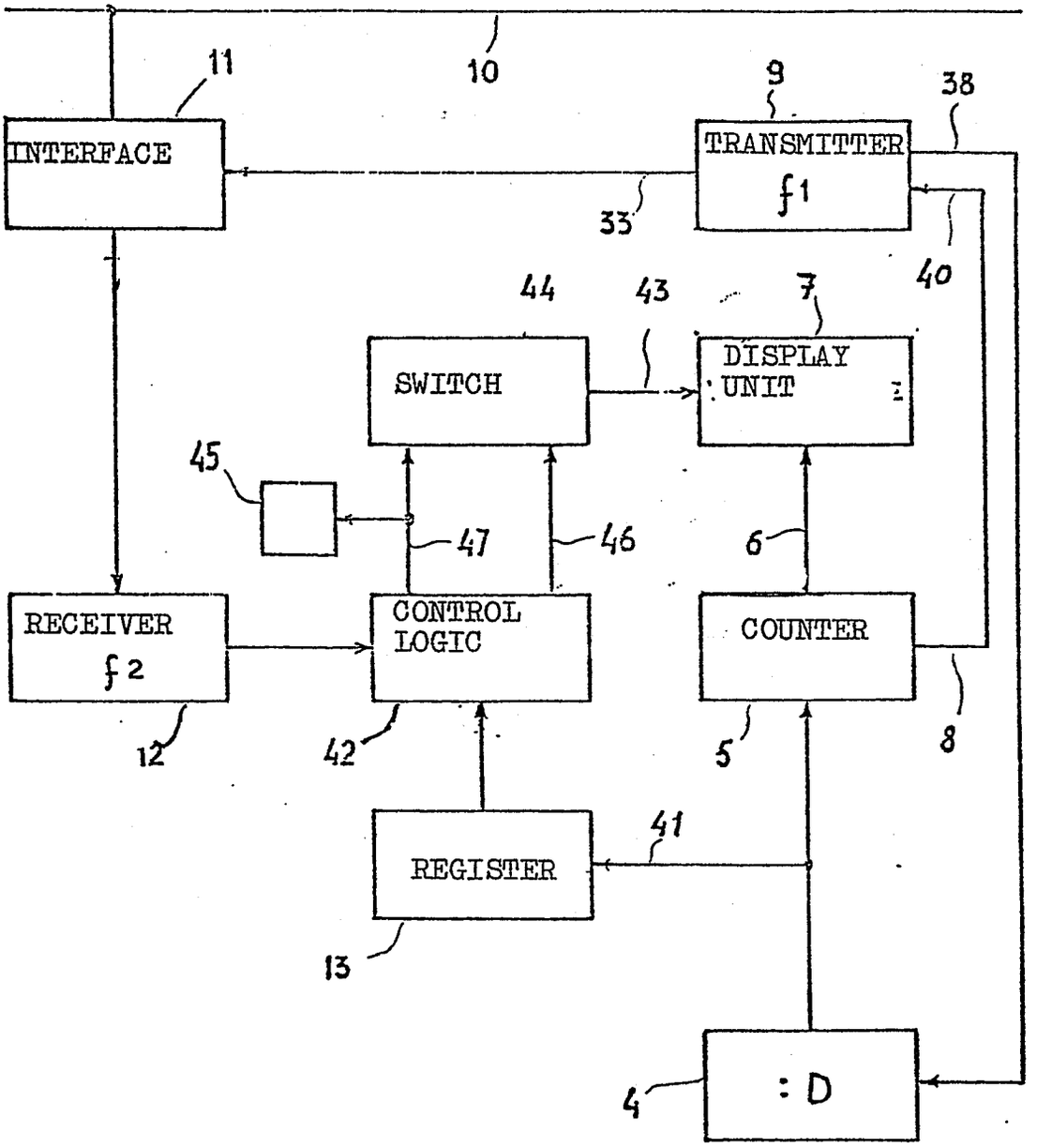
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Fig. 1

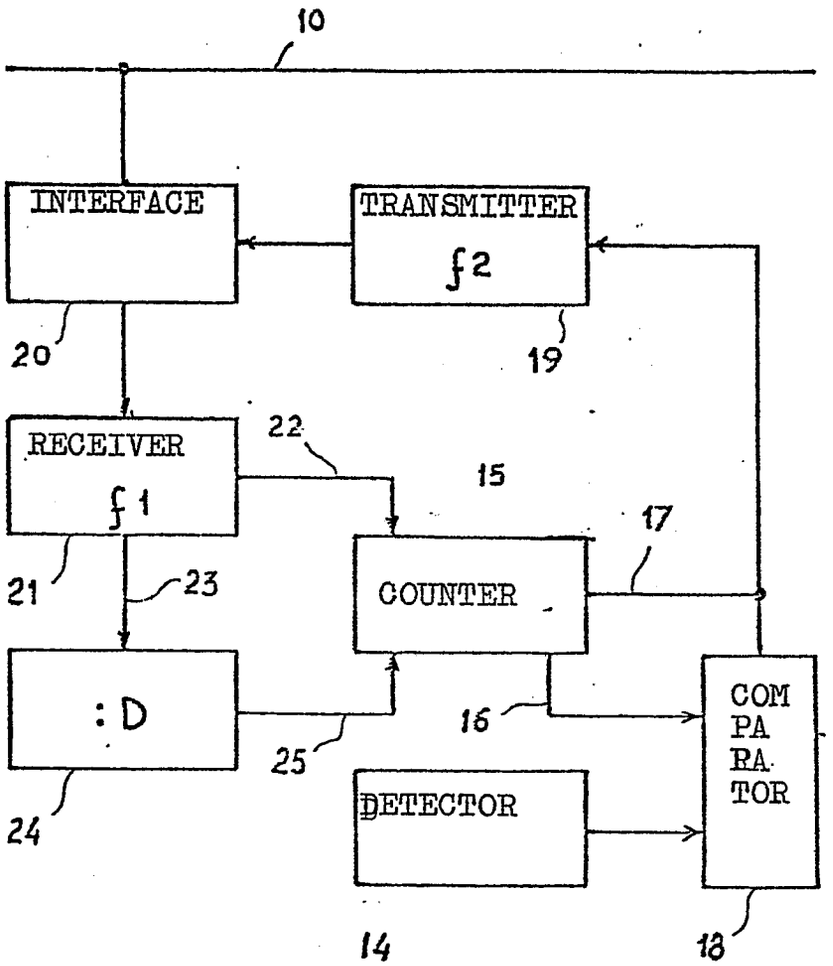
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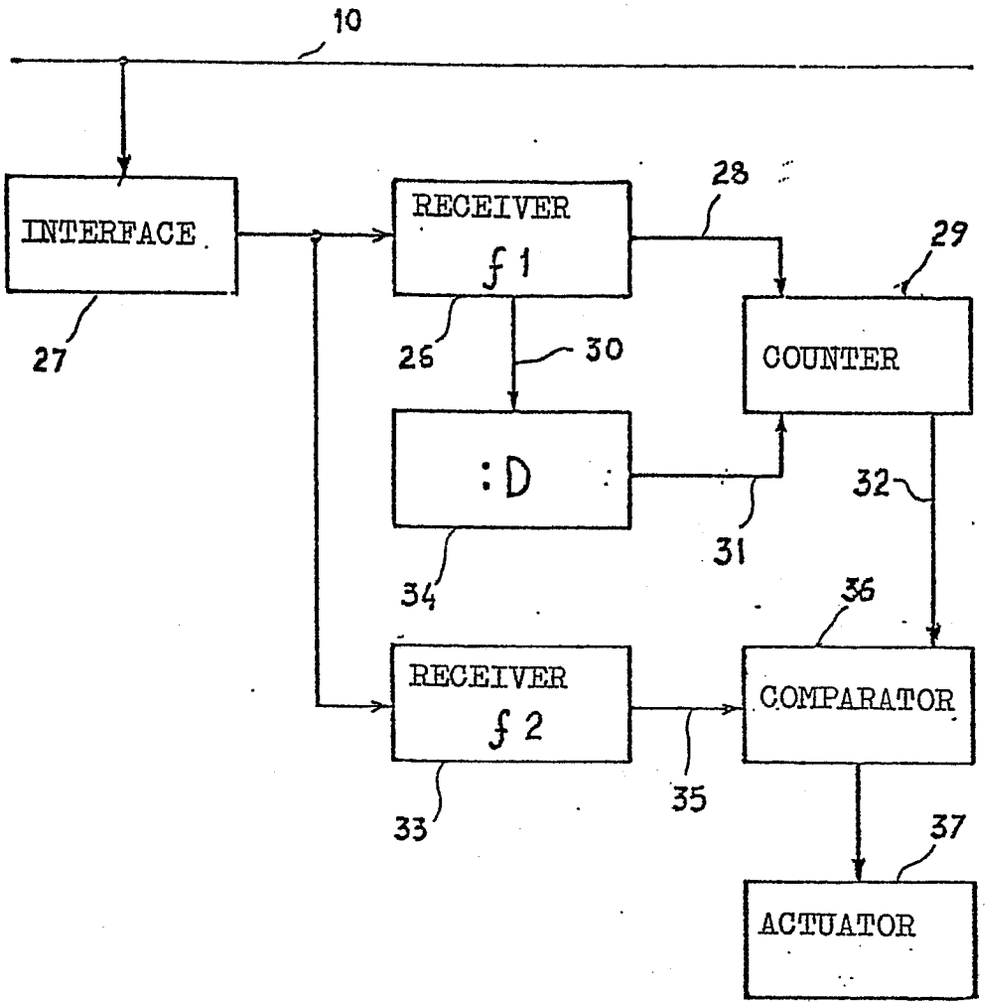
Fig. 2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36
RECEIVER
f 2
33
35
COMPARATOR
37
ACTUATOR

Fig. 3

European Patent Office

EUROPEAN SEARCH REPORT

0089607
Application number

EP 83 10 2557

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
A	GB-A-2 023 896 (MOLLER) * Page 2, line 16 - page 3, line 28; figure 1 *	1-2	G 08 B 25/00 G 08 B 26/00
A	US-A-3 482 243 (BUCHSBAUM) * Column 2, line 50 - column 5, line 29; figures 1,2 *	1-2	
A	GB-A-1 414 574 (AMP) * Page 2, lines 33-64; claim 1; figure 1 *	1	
A	US-A-4 156 112 (MORELAND) * Abstract *	1	
A	EP-A-0 032 135 (RAVENINGHAM ELECT. RES.) * Abstract *		

TECHNICAL FIELDS SEARCHED (Int. Cl. ³)

G 08 B
G 08 C
H 04 Q

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	24-06-1983	SGURA S.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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