(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 104 865**
A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 83305506.4

(22) Date of filing: 20.09.83

(51) Int. Cl.³: E 05 B 49/00

(30) Priority: 28.09.82 GB 8227635

(43) Date of publication of application:
04.04.84 Bulletin 84/14

(84) Designated Contracting States:
CH DE FR IT LI SE

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(54) Code confirmation circuit.

(57) A code confirmation circuit includes input means comprising a number of switches (Kl to Kn) each representing a different code value. A counter (CT) has a number of outputs energisable in sequence from a datum state and each representing a different code value. Circuit means interconnect the switches and the outputs of the counter such that the operation of a switch having the same code value as the energised counter output causes an amplifier (A1) to clock the counter (CT) so as to energise the next counter output in sequence. Resetting means comprising a second amplifier (A2) are responsive to the operation of an incorrect switch to cause the counter to be reset. The energisation of the last counter output in the sequence indicates the correct sequence of operation of the switches.

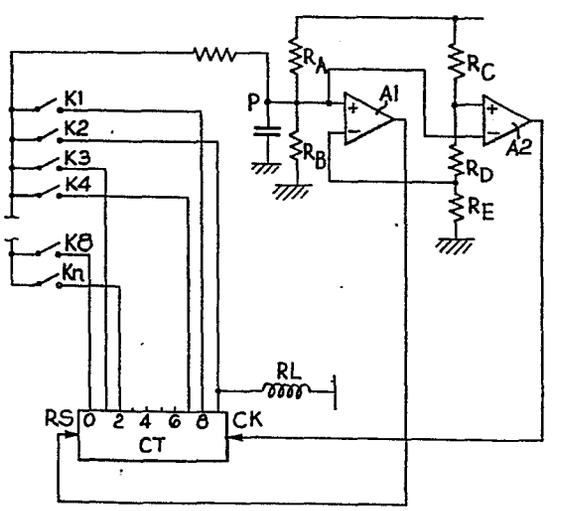


Fig. 1

EP 0 104 865 A2

CODE CONFIRMATION CIRCUIT

This invention relates to a code confirmation circuit, that is to a circuit arranged to confirm, or otherwise, that an input denoted by a sequence of switch operations agrees with a predetermined code sequence. Such a circuit may be used, for example, with a so-called "digital lock" in which the operation of a number of keys in the correct sequence is necessary for the release of the lock. The keys are frequently, though not necessarily, marked with digits, though other symbols are sometimes used,

According to the present invention there is provided a code confirmation circuit which includes input means comprising a number of switches each representing a different code value, a counter having a number of outputs energisable in sequence from a datum state and each corresponding to a different code value, circuit means interconnecting the said switches and the said counter outputs such that the operation of a switch having the same code value as an energised counter output causes the counter to be clocked so as to energise the next counter output in the sequence, and resetting means responsive to the operation of a switch having a code value different from that of an energised counter output to prevent the clocking of the counter to the next output in sequence, the energisation of the last counter output in the sequence indicating the confirmation of the code identified by the sequence in which the switches were operated.

The invention will now be described with reference to the accompanying drawings, in which:-

Figure 1 is a schematic circuit diagram of a first embodiment;

Figure 2 shows a possible modification to the circuit of Figure 1;

Figure 3 is a similar diagram of a second embodiment; and

Figure 4 shows a modification to the embodiment of Figure 3.

Referring now to Figure 1, this shows a simple circuit according to the invention. The switches are in the form of push-button keys of which only six are shown. A counter CT has each of its outputs connected directly through a separate and predetermined one of the keys K1 to Kn to a common point P. A capacitor is connected to point P to remove transients caused by key contact bounce. A first amplifier A1 has its non-inverting input connected to point P and to a potential divider comprising resistors R_A and R_B, and has its non-inverting input connected to a reference voltage V_{R1} derived from a further potential divider comprising resistors R_C, R_D and R_E. The output of amplifier A1 is connected to the reset input RS of the counter CT. A second amplifier A2 has its inverting input connected to the common point P, and has its non-inverting input connected to a second reference voltage V_{R2}, also derived from the further potential divider, which is higher than V_{R1}. The output of amplifier A2 is connected to the clock input CK of the counter CT. The last output of the counter CT is connected to some form of actuator, shown here as a relay RL, to operate whatever mechanism or circuit is controlled by the circuit.

In operation, the counter is normally reset to its '0' state, with the '0' output of the counter in the high state and awaiting operation of the keys. If the key connected to this output, shown in the drawing as key K8, is pressed, then the non-inverting input of amplifier A1 also goes high. This causes no change in the amplfier output. Similarly, the inverting input of the amplifier A2 goes low on key closure. This change does affect the counter, but the subsequent change when the key K8 is released results in the output of amplifier A2 going high and causing the counter CT to clock so as to energise the '1' output of the counter. The above procedure is followed each time that a key is operated in the correct sequence, this sequence being determined purely by the interconnections between the keys and the counter outputs.

If, at any time, an incorrect key is pressed, then the non-inverting inputs of the two amplifiers go low. The output of amplifier A1 also goes low, and on the subsequent release of

the key the change in output from amplifier A1 resets the counter CT.

It will be seen that the circuit arrangement described above allows each key to be used only once in a sequence. Hence with ten keys and a ten-stage counter CT a maximum of 10! or 3.63×10^6 different combinations is possible. Clearly a smaller or larger number of keys may be used, with the appropriate counter, to provide sequences of different length. However, every key connected to a counter output must be used to obtain a complete sequence, though some keys could be "dummy" keys, with no actual connection to the counter.

Figure 2 shows a modification of the circuit of Figure 1 to include a second counter CT1 arranged to render the circuit inoperative, or give an alarm, after a predetermined number of errors. This second counter is clocked by the "reset" signals from amplifier A1 of Figure 1, and an output from the counter CT2 after a predetermined number of input signals operates a lock-out or alarm circuit AM.

Figure 3 shows a second embodiment which allows for a larger number of possible code combinations by allowing each key to be used as many times as required. Such an arrangement having ten keys will provide 10^{10} possible combinations.

Referring now to Figure 3, the counter CT is still used, and each output except the '0' state output is connected to the common point P through a separate resistor R1 to R9 of predetermined value. Also connected to the common point P are four resistors R10 to R13 connected to a voltage source $-V_s$ by way of a conventional binary-coded decimal keyboard K. The keyboard is arranged to connect one or more of the resistors R10 to R13 to the voltage source, depending on which key is operated. Each output from the keyboard K is also connected through resistors to a transistor inverter Q_1 connected to the clock input CK of the counter CT. The clock input CK is also connected to the control input of a switch Q_2.

The common point P is also connected by switch Q_2 to the inverting input of an amplifier A1 having its non-inverting input connected to a reference voltage V_R, preferably zero.

The output of amplifier A1 is connected to the inverting input of a second amplifier A2, again having its non-inverting input connected to the same reference voltage V_R. The outputs of the two amplifiers A1 and A2 are connected through diodes D1 and D2 to the reset input RS of the counter CT. As in the previous embodiment the output of the last stage of the counter is connected to an actuator, such as a relay RL, or to another circuit or circuit element.

The values of the resistor R1 to R9 and R10 to R13 are determined as follows:- each successive output of the counter CT from the datum or '0' state, represents a different successive code value. If, for example, nine keys provide nine decimal digits, and the counter CT is a ten stage counter, then the code will have nine digits, each being represented by a different output from the counter. When the counter is in any particular state, then current from the counter output will flow through the energised one of the resistors R1 to R9, causing a voltage to exist at the common point P. Equally, when one of the keys of the keyboard is pressed, a particular voltage will be developed across the selected one or ones of the resistors R10 to R13 and applied to the common point P.

If the two voltages are arranged to be of opposite polarity, then when they are equal there will be no resultant voltage at point P. The resistors R1 to R9 are thus chosen so that the voltage developed across the nth one is equal and opposite to the voltage developed at point P resulting from the operation of the key representing the nth digit in the code sequence.

The operation of the circuit is as follows:-

The counter CT is initially in the reset state, with only the '0' input high and with no output resistor energised. The operation of the key representing the first digit in the code sequence, results in current flowing through one or more of resistors R10 to R13. At the same time, the operation of the key causes the counter to be clocked via switch Q_1 so that the '1' output is energised. The voltage developed across resistor R1 is arranged to be equal and opposite to that developed across

the selected ones of resistors R10 to R13, and hence the voltage at point P does not change. Switch Q_2 is also closed, connecting point P to the inverting inputs of amplifiers A1 and A2, and since the voltage at P does not change there is no output from either of amplifiers A1 and A2. Hence the counter CT is not reset. When the key is released, switch Q_2 opens, thus preventing amplifiers A1 and A2 from responding to the resulting imbalance at point P.

When the next key is pressed, the counter is again clocked, to energise resistor R2. Again, if the voltage developed across them is arranged to be equal and opposite to that developed across resistor R10 then the counter CT will not be reset.

The process may be repeated throughout the code sequence, until the output from the last stage of the counter shows that the required number of keys have been pressed in the correct sequence, and the actuator RL is energised.

If, at any stage, a wrong key is pressed, then the voltage at point P will not be zero. If it is either substantially positive or negative then there will be an output from one of the two amplifiers A1 and A2, and the counter will be reset.

It will be seen that the circuit described above gives the full range of 9^9 possible combinations. Simpler or shorter sequences may obviously be used by using codes having a shorter sequence of digits. Each digit may be used in the sequence as often as required, or not used at all.

In some situations the circuit of Figure 3 is not suitable, particularly because it requires five connections from the keyboard to the resistor and the remaining circuitry. In a system, such as an alarm system, having a single wire loop, some other arrangement has to be used. Figure 4 shows such an arrangement which may be connected into such a loop system.

The main difference from the circuit of Figure 3 is the modified connection of the keyboard and the inclusion of an analog-to-digital converter AD, and a constant current generator CC.

The switches may be in the form of push-button keys, of which only six are shown, labelled K1 to K6. These switches are connected across four resistors R14 to R17 connected in series with one another. The values of the resistors are such that any series connection of one or more of the resistors will give an unique total resistance value. Conveniently, though not necessarily, the resistors may have resistance values related by a binary sequence, such as N, 2N, 4N and 8N. With the appropriate connection of the switches K, these resistors would give up to sixteen unique resistance values on the operation of a single one of the switches. The series-connected resistors are connected across the output of the constant current generator CC.

The voltage generated across the series-connected resistors R14 to R17, or any of those resistors, is applied to the input of a four-bit analog-to-digital converter AD. The four outputs of the converter are each connected through separate resistors R10 to R13 to the common point P.

The counter CT and amplifiers A1 and A2 are connected as shown in Figure 3, and the circuit operates in a similar manner. A voltage developed across one or more of resistors R14 to R17 produce a particular combination of outputs from the converter AD, resulting in a voltage at point P unique to the code value of the depressed key. As before, for correct operation this voltage is offset by the voltage developed across the resistor connected to the energised counter output.

As before, the lock-out or alarm circuit may be added to this embodiment.

It will be appreciated that whilst it is convenient for the two voltages appearing at point P to offset one another, it is possible for these to be combined additively, with suitable arrangement of the reference voltages on the two amplifiers A1 and A2. The final "code confirmed" output from the last stage of the counter may be used for any desired purpose. In the case of a digital lock this may operate a locking or unlocking mechanism, but in other applications the output may be used for other purposes.

CLAIMS

1. A code confirmation circuit which includes input means comprising a number of switches each representing a different code value, a counter having a number of outputs energisable in sequence from a datum state and each corresponding to a different code value, circuit means interconnecting the said switches and the said counter outputs such that the operation of a switch having the same code value as an energised counter output causes the counter to be clocked so as to energise the next counter output in the sequence, and resetting means reponsive to the operation of a switch having a code value different to that of an energised counter output to prevent the clocking of the counter to the next output in sequence, the energisation of the last counter output in the sequence indicating the confirmation of the code identified by the sequence in which the switches were operated.

2. A circuit as claimed in Claim 1 in which the circuit means include a separate direct connection from each one of said switches to a selected and different one of the counter outputs, and a common connection from each one of said switches to a comparator operable to clock the counter.

3. A circuit as claimed in Claim 2 in which the resetting means includes a further comparator connected to the said common connection and operable to reset the counter to its datum state.

4. A circuit as claimed in Claim 1 in which the circuit means incudes a separate resistor connected between each counter output and a common point, and a number of further resistors connected between said switches and said common point, the switches being arranged such that the operation of any one switch causes the energisation of an unique combination of said further resistors, the values of the separate resistors and of the further resistors being such that the energisation of a correct key in the sequence results in no change in the potential of the said common point.

5. A circuit as claimed in Claim 4 in which the operation of any one of said switches causes the counter to clock to its next output.

6. A circuit as claimed in Claim 1 which includes a chain of series-connected resistors having the switches connected thereto

in such a manner that the operation of any one switch results in a total resistance which is different from that resulting from the operation of any other switch, a constant-current generator arranged to cause a constant current to pass through said chain of series-connected resistors, an analog-to-digital converter responsive to the voltage developed across said chain to produce an output at one or more of its output terminals, a separate first resistor connected between each output of the said converter and a common point, and separate second resistors connected between selected ones of the counter outputs and said common point, the arrangement being such that the energisation of a correct key in sequence results in no change in the potential of the said common point.

7. A circuit as claimed in Claim 6 in which the operation of any one of said switches causes the counter to clock to its next output.

8. A circuit as claimed in any one fo the preceding claims which includes an actuator which is energised on the confirmation of the code.

9. A circuit as claimed in any one of Claims 1 to 8 which includes an alarm operable if the counter is reset by the incorrect operation of a switch.

10. A circuit as claimed in any one of Claim 1 to 9 in which the switches are in the form of push-button keys.

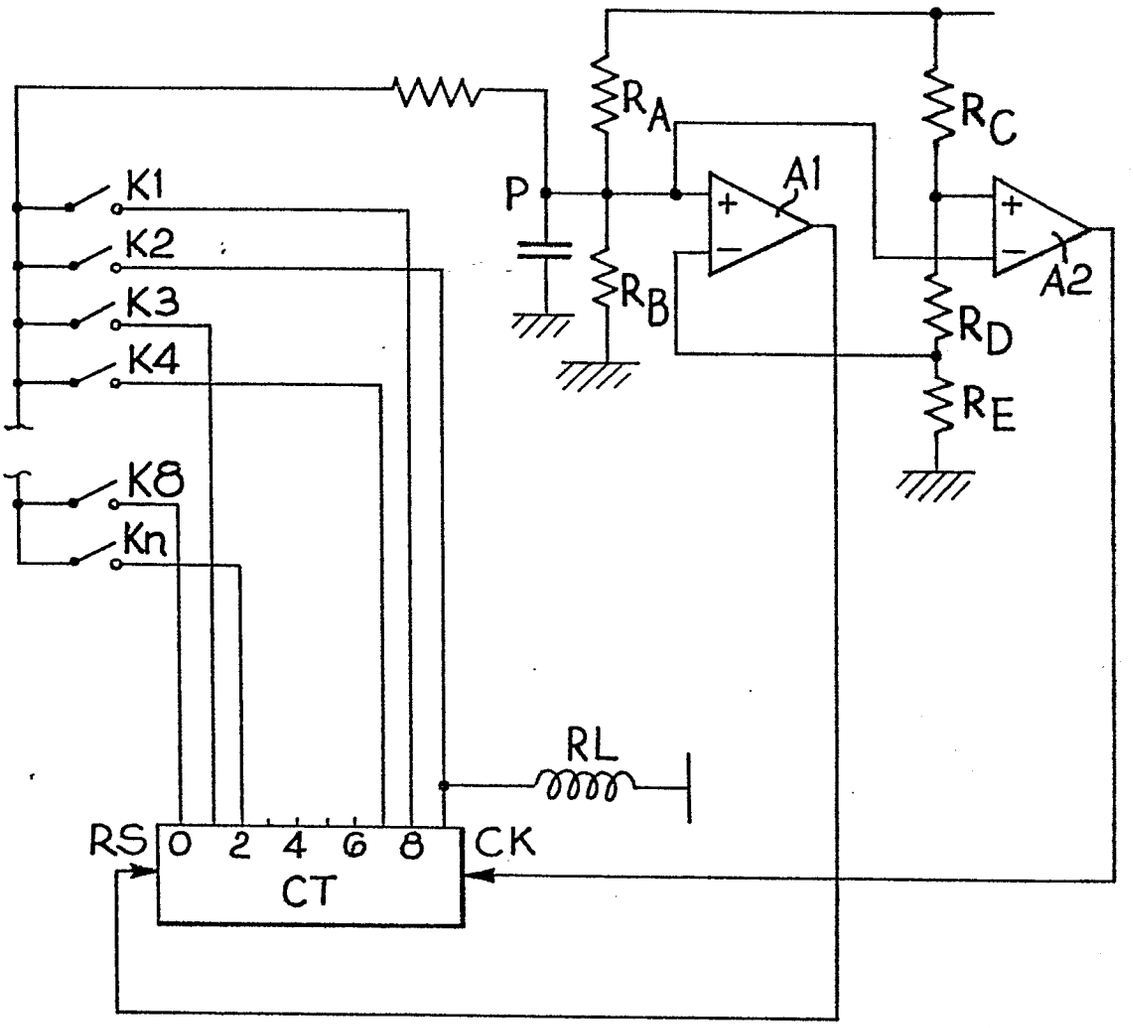

K1
K2
K3
K4
K8
Kn
P
RA
RB
RC
RD
RE
A1
A2
RL
RS
0 2 4 6 8
CT
CK

Fig. 1

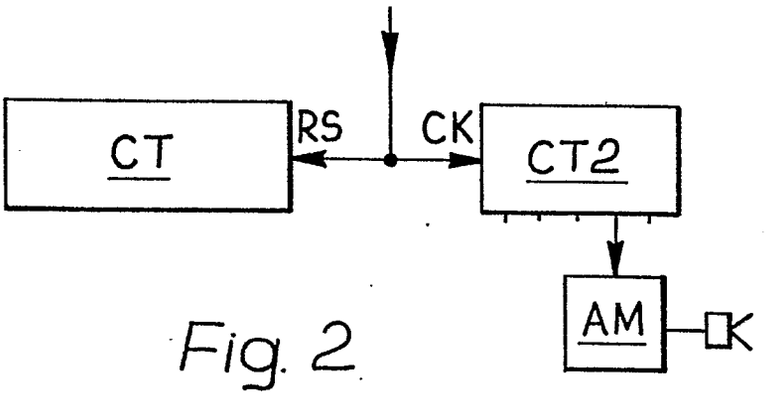
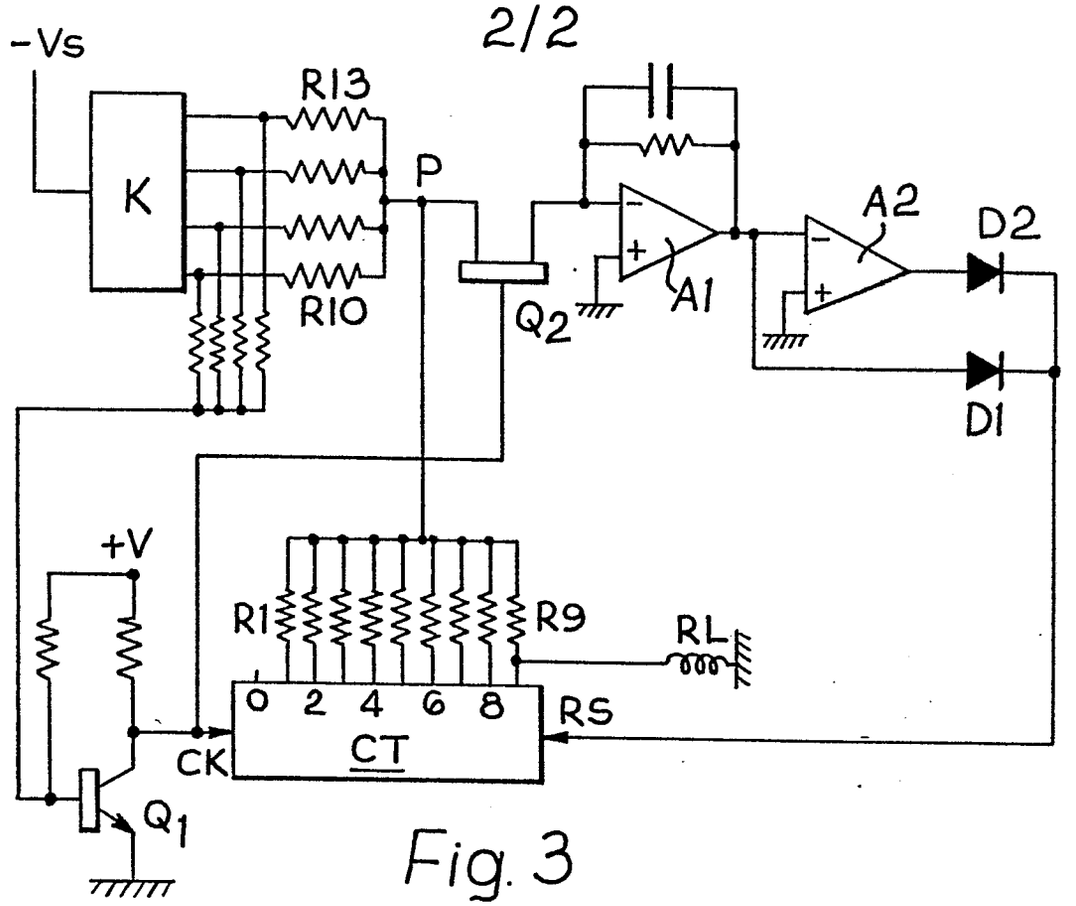

CT
RS
CK
CT2
AM
K

Fig. 2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K
R13
R10
P
Q2
A1
A2
D2
D1
+V
R1
R9
RL
0 2 4 6 8
CT
RS
CK
Q1

Fig. 3

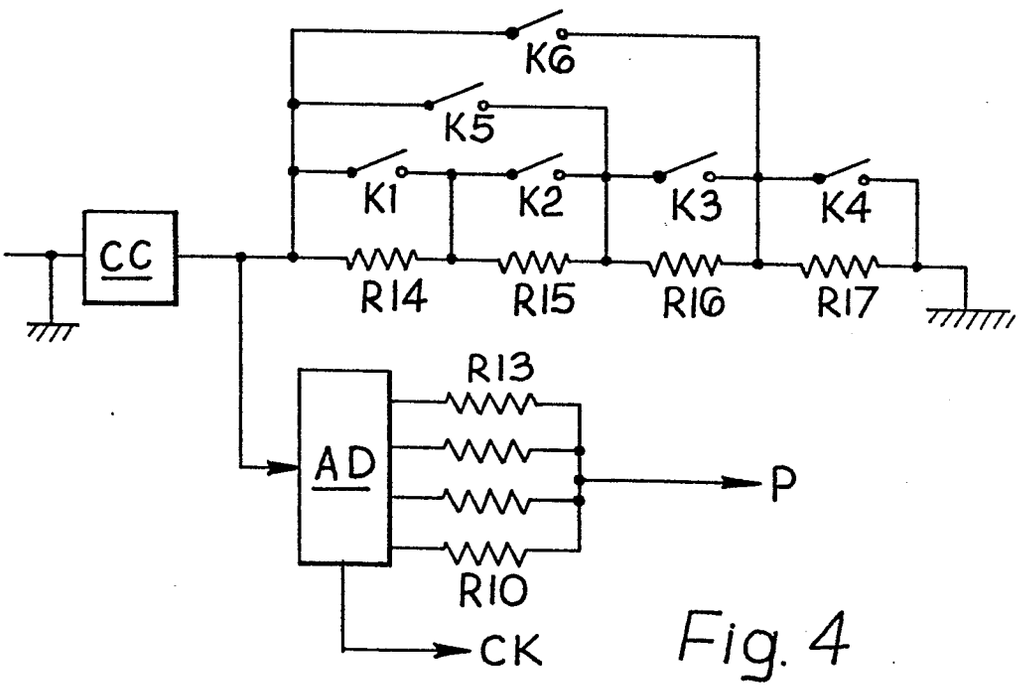
K6
K5
K1
K2
K3
K4
CC
R14
R15
R16
R17
R13
AD
P
R10
CK

Fig. 4