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(54) **Data write arrangement for color graphic display unit.**

(57) A plurality of color graphic memories (41,51,61) are assigned the same address space, and are connected to a common data bus (X_1). It is determined by a separately output memory select data which one of the color graphic memories (41,51,61) is to be written into. In the case of writing the same data into two or more of the color graphic memories (41,51,61) at the same address, the color graphic memories to be written into are selected by the memory select data first and then the same data is written into the selected colour graphic memories in the same write cycle.

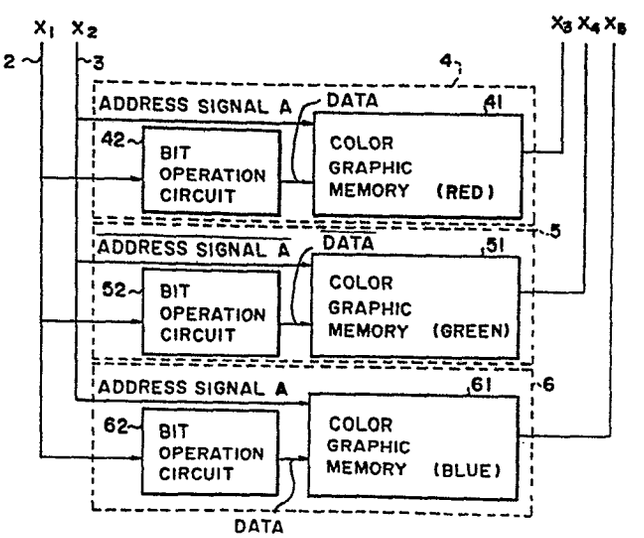

FIG. 1 B

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DATA WRITE ARRANGEMENT FOR COLOR GRAPHIC DISPLAY UNIT

The present invention relates to a data write arrangement for a color graphic display unit.

A color graphic display unit is provided with a plurality of color graphic memories, each having storage areas corresponding to respective parts of a display screen, and the color or colors to be displayed are specified by a combination of data written into the memories at the same address. For example, in an ordinary color graphic display unit having red, green and blue color graphic memories, an area written into the red-color memory alone is displayed in red, and an area written into all the three memories is displayed in white. Therefore, according to a color it is desired to display, it may be necessary to write exactly the same data into two or more color graphic memories at the same address. With the conventional color graphic display unit, however, the plurality of color graphic memories have different address spaces and they are selected by decoding an address output of a microcomputer, so that only one color graphic memory can be accessed in one operation cycle of the microcomputer. This leads to the

defect that much time is needed for writing the same data into two or more color graphic memories at the same address.

According to the present invention there is provided a data write arrangement for a color graphic display unit, comprising a plurality of color graphic memories assigned the same address space, addressing means for addressing the space in the color graphic memories, data write means for outputting data to be written into the addressed space of at least one of the color graphic memories, and memory select means for selecting which one or more of the color graphic memories will receive said data.

An embodiment of the present invention provides a data write arrangement which permits data to be quickly written into color graphic memories.

In accordance with the present invention, a plurality of color graphic memories are assigned the same address space, and separately output data controls which one or more of the color graphic memories is or are to be written into.

A preferred embodiment of data write arrangement of the present invention is provided with a plurality of color graphic memories assigned the same address space, data write means for outputting an address signal specifying each address of the color graphic memories, a chip select address signal, data on the content to be written into and memory select data for selecting at least one of the color graphic memories into which the data is written, a latch circuit for latching the memory select data, an address decoder for decoding the chip select address signal, and a chip select circuit for generating a chip select signal by logical processing of the outputs of the address decoder and latch circuit. The data write means outputs the memory select data first and then the address signal and the data.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and B are block diagrams illustrating the

principal part of an embodiment of a data write arrangement of the present invention;

Fig. 2 is a timing chart showing, by way of example, signal waveforms occurring at respective parts of the arrangement of Figs. 1A and B while in operation; and

Fig. 3 is a flowchart showing an example of processing of the microcomputer 1 in Figs. 1A and B.

In Figs. 1A and B reference numeral 1 indicates a microcomputer; 2 and 3 designate its data and address buses; 4 to 6 identify memory parts; 41, 51 and 61 denote color graphic memories; 42, 52 and 62 represent bit operation circuits; 7 shows an address decoder; 8 refers to a memory selecting data latch circuit; 81 to 83 signify latch elements; 9 indicates a chip select circuit; and 91 to 93 designate AND circuits.

The color graphic memories 41, 51 and 61 each have storage areas corresponding to respective parts of a display surface, and data written in each memory is cyclically read out with a scanning address from a CRT controller (not shown) for input into a display (not shown). The memories 41, 51 and 61 are usually formed by readable/writable semiconductor memories. In the present invention, the three color graphic memories 41, 51 and 61 are assigned the same address space. An address signal A which is applied to each memory is to specify each address therein. Further, chip select signals CS1 to CS3 are selectively provided from the chip select circuit 9 to the color graphic memories 41 to 51, permitting data to be written into

the memory selected by the chip select signal.

The bit operation circuits 42, 52 and 62 each decide , by a signal from the microcomputer 1, whether data is written into the corresponding color graphic memory in units of bits or bytes; in the case of writing the data in units of bytes, the bit operation circuit writes, for example 8-bit data of the microcomputer 1 directly into the corresponding color graphic memory and, in the case of writing the data in units of bits, the bit operation circuit reads out 1-byte data from the corresponding color graphic memory at the concerned address thereof, modifies the data with 1-bit information from the microcomputer 1 and rewrites the modified data into the memory. Since this bit operation processing is completed in one operation cycle of the microcomputer in terms of software, even a minute modification of a picture can be quickly effected.

The microcomputer 1 constitutes data write means for the color graphic memories 41, 51 and 61, and it is connected to the memory parts 4 to 5 via the data bus 2 and the address bus 3. The microcomputer 1 provides a chip select address signal to the address decoder 7 and a memory select data to the latch circuit 8. The memory select data is one that specifies which one of the color graphic memories 41, 51 and 61 is written into. For instance, 1-bit information is assigned to each memory; when the information is a "1", data is written into the memory and when the information is a "0", the data is

not written thereinto. The latch elements 81, 82 and 83 set therein information on the memories 41, 51 and 61, respectively.

The address decoder 7 decodes address signals from the microcomputer 1 other than the address signal A. In the present embodiment, since the color graphic memories 41, 51 and 61 have the same address space, the address decoder 7 outputs a "1" even if any one of the color graphic memories 41, 51 and 61 is selected.

The chip select circuit 9 generates a chip select signal by logical processing of the outputs of the address decoder 7 and the memory select data latch circuit 8. The chip select circuit 9 has such an arrangement, for example, as shown in Fig. 1, in which the AND circuits 91, 92 and 93 are provided respectively corresponding to the color graphic memories 41, 51 and 61, which are supplied at one input terminal with the outputs of the latch elements 81, 82 and 83, respectively, and at the other input terminals with the output of the address decoder 7.

With the arrangement of Fig. 1, for instance, in the case of writing the same data into the color graphic memories 41 and 61 at the same address, the microcomputer 1 provides memory select data of the content (101) to the latch circuit 8 prior to data write, causing the latch elements 81 and 83 to have "1" outputs and the latch element 82 to have a "0" output. Then the microcomputer 1 generates an address signal which

specifies the address to be written into, the data to be written into and a write cycle. In this case, since only the AND circuits 91 and 93 are held open, the chip select signals CS1 and CS3 are applied to the color graphic memories 41 and 61, and the color graphic memory 51 is not selected. Consequently, the same data is written into the color graphic memories 41 and 61 at the same address at the same time. Fig. 2 shows, by way of example, signal waveforms occurring at respective parts of the arrangement in the case of the above write being performed in units of bits. Because of the bitwise write, the bit operation circuits 41 and 51 generate a read cycle and a write cycle in the address effective period of the microcomputer 1. Incidentally, the data from the microcomputer 1 includes information indicating how each bit is to be written into the color graphic memory, and the bit operation circuit write the data in accordance with the information.

In the above example data is written into the color graphic memories 41 and 61 but, by modifying the memory select data, the data can simultaneously be written into a plurality of memories of other combination thereof and it can also be written into one of them. That is, as shown in the flowchart of Fig. 3, the microcomputer 1 decides the color of the graphic form to be displayed and, according to the decision result, writes a "1" or "0" into each of the latch elements 81 to 83, thereafter accessing the color graphic memories 41, 51 and 61.

While the present invention has been described as being applied to the case of employing three color graphic memories, the invention is similarly applicable to the case of using two or more than three color graphic memories.

As has been described in the foregoing, according to the present embodiment, the same address space is assigned to each of a plurality of color graphic memories, and one controls by separately output memory select data which one of the memories is to be written into. Accordingly, by outputting the memory select data prior to the transfer of the data to be written into, it is possible that, in the subsequent write cycles, the data is written into a plurality of color graphic memories in the same cycle. Thus the processing of writing the same data into a plurality of color graphic memories at the same address can be achieved in a shorter time than in the prior art.

It will be apparent that many modifications and variations may be effected without departing from the scope of the novel concepts of the present invention.

A plurality of color graphic memories (41,51,61) are assigned the same address space, and are connected to a common data bus (X_1). It is determined by a separately output memory select data which one of the color graphic memories (41,51,61) is to be written into. In the case of writing the same data into two or more of the color graphic memories (41,51,61) at the same address, the color graphic memories to be written into are selected by the memory select data first and then the same data is written into the selected color graphic memories in the same write cycle.

CLAIMS

1. A data write arrangement for a color graphic display unit, comprising a plurality of color graphic memories assigned the same address space, addressing means for addressing the space in the color graphic memories, data write means for outputting data to be written into the addressed space of at least one of the color graphic memories, and memory select means for selecting which one or more of the color graphic memories will receive said data.

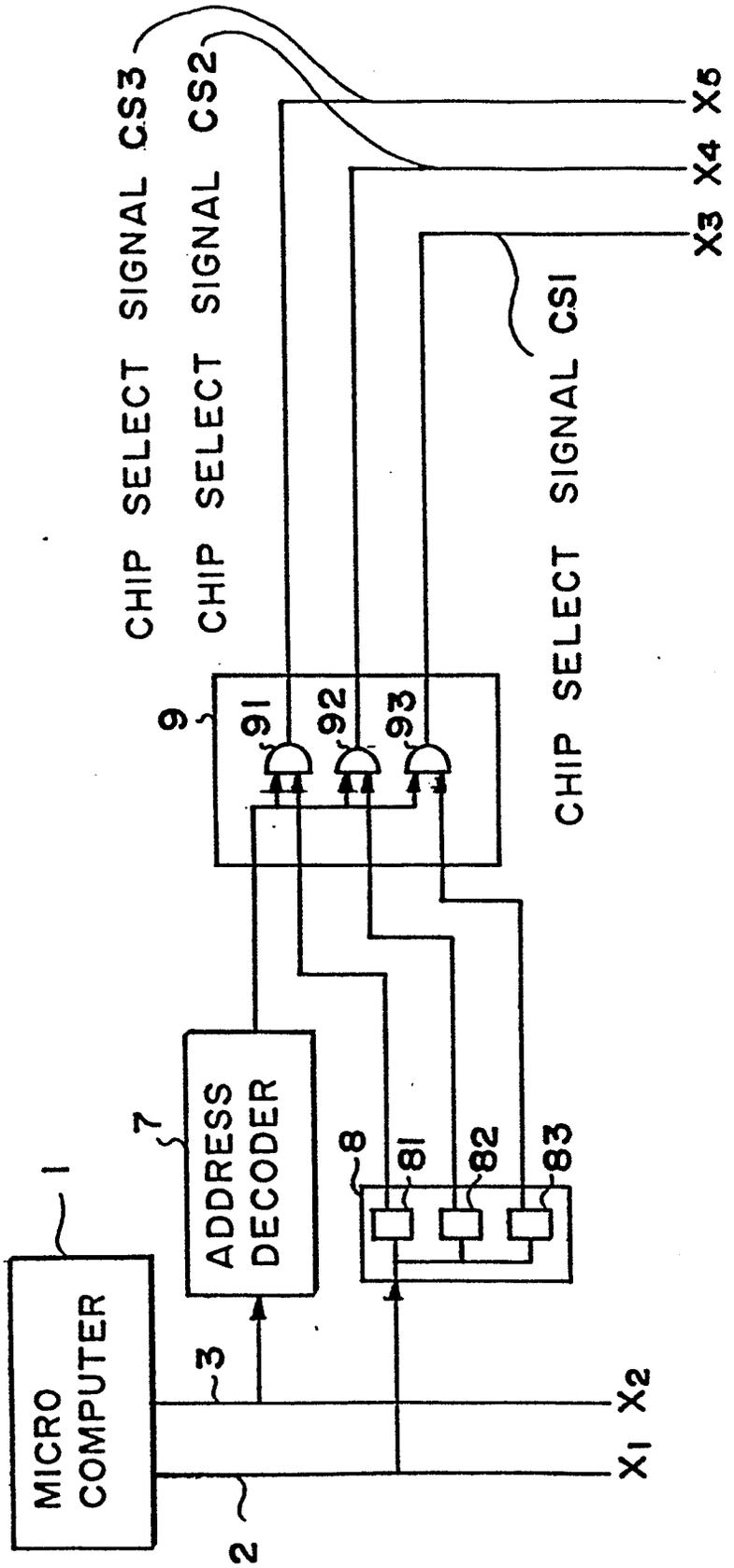
2. A data write arrangement according to claim 1, which is adapted and arranged such that in operation of the arrangement the memory select means outputs memory select data and then the addressing means and the data write means output an address signal and data respectively for the color graphic memories.

3. A data write arrangement according to claim 1 or 2, wherein the memory select means comprises a chip select circuit for generating a chip select signal by logical processing of outputs from a latch circuit for latching memory select data, and from an address decoder for decoding a chip select address signal.

4. A data write arrangement according to claims 1, 2 and 3 combined, wherein when the arrangement is in operation the memory select data, the memory address signal, the memory data and the chip select address signal are all generated from the same source.

5. A data write arrangement according to claim 4, wherein said source is a microcomputer.

FIG. 1A


CHIP SELECT SIGNAL CS3
CHIP SELECT SIGNAL CS2
CHIP SELECT SIGNAL CS1
X5
X4
X3
X2
X1
MICRO COMPUTER
ADDRESS DECODER
1
2
3
7
8
9
81
82
83
91
92
93

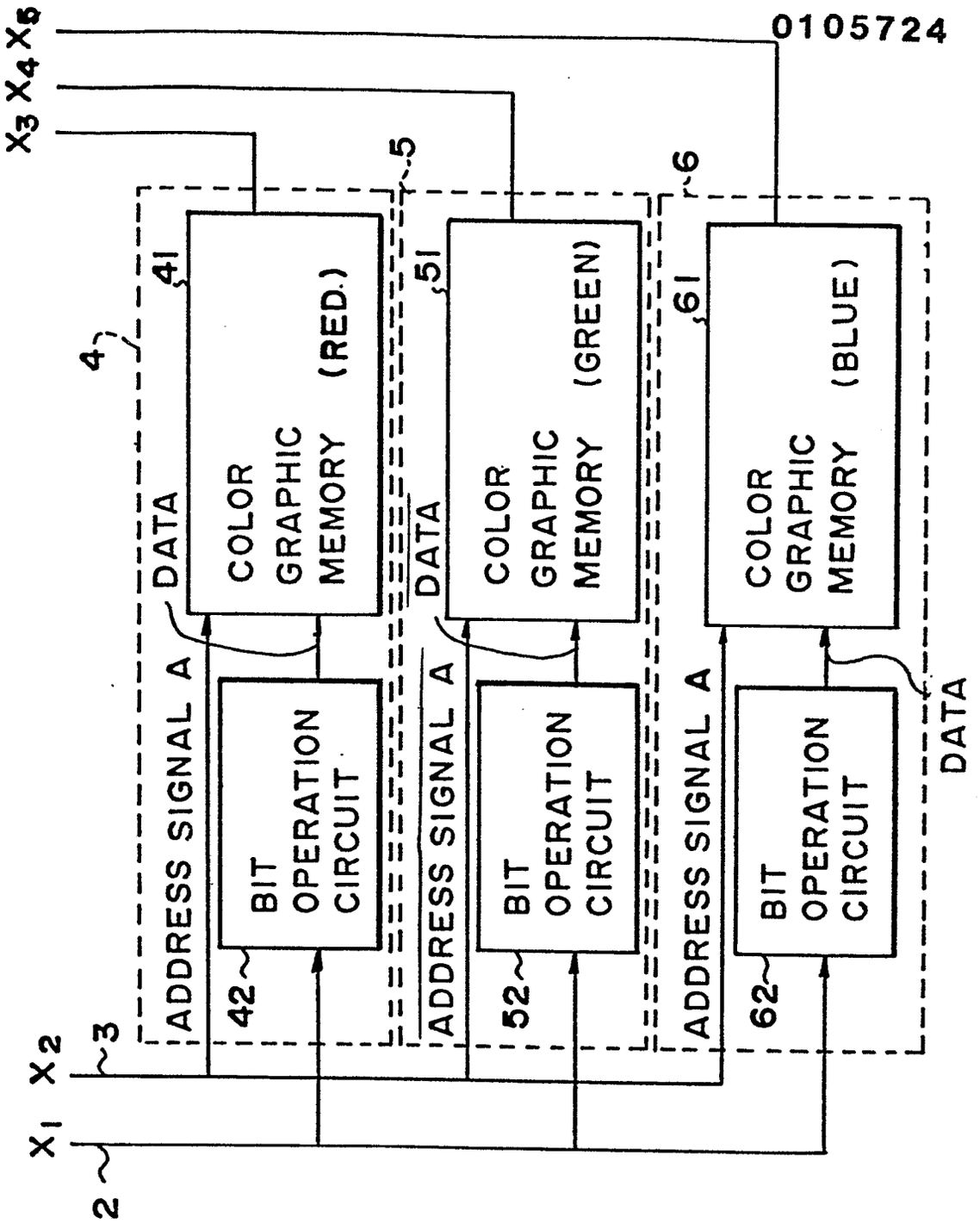

X1 X2 X3 X4 X5
2
3
4
5
6
41
42
51
52
61
62
COLOR GRAPHIC MEMORY (RED.)
COLOR GRAPHIC MEMORY (GREEN)
COLOR GRAPHIC MEMORY (BLUE)
BIT OPERATION CIRCUIT
BIT OPERATION CIRCUIT
BIT OPERATION CIRCUIT
ADDRESS SIGNAL A
ADDRESS SIGNAL A
ADDRESS SIGNAL A
DATA
DATA
DATA

FIG. 1 B

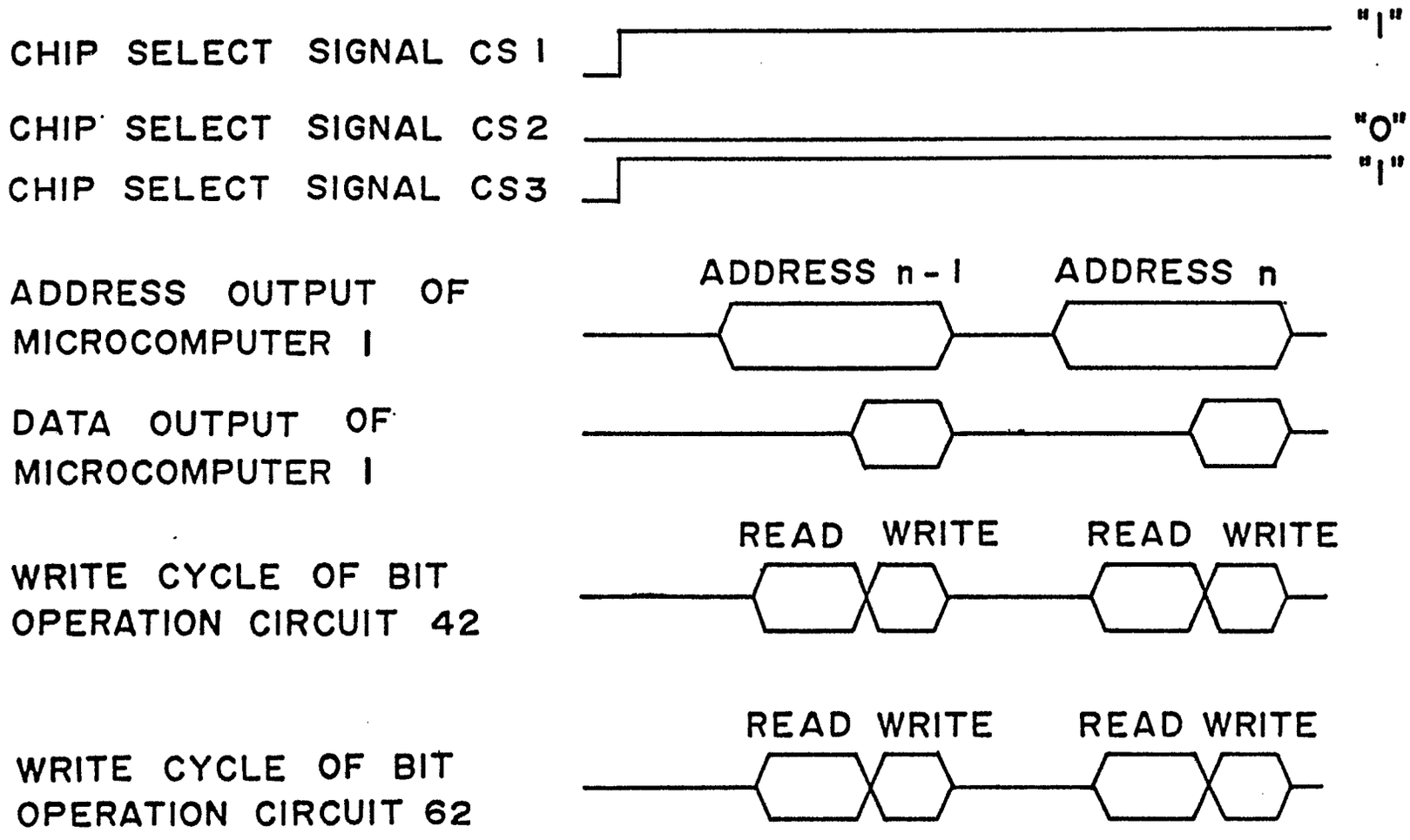


FIG. 2

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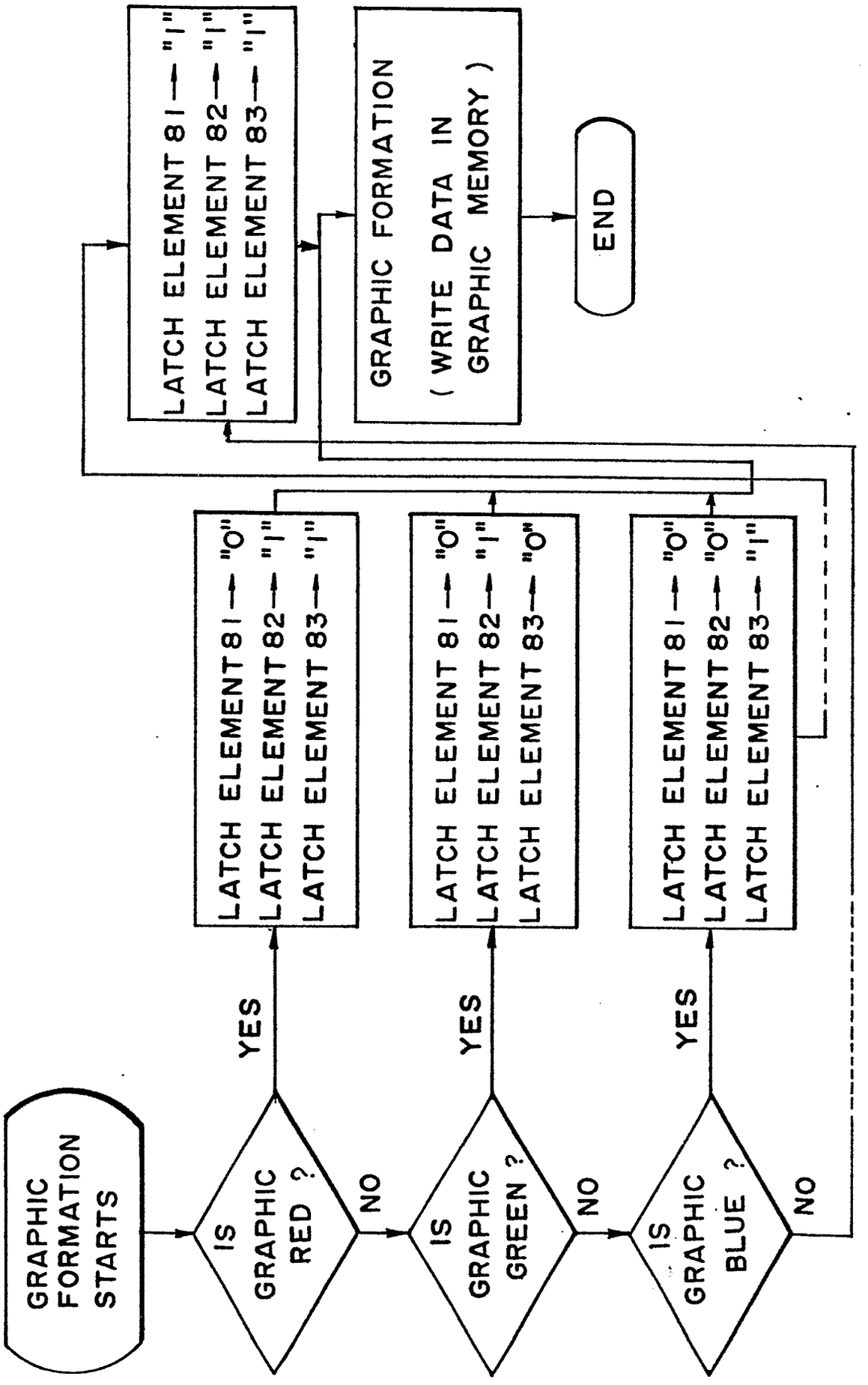
FIG. 3


GRAPHIC FORMATION STARTS
IS GRAPHIC RED ?
YES
NO
LATCH ELEMENT 81 — "0"
LATCH ELEMENT 82 — "1"
LATCH ELEMENT 83 — "1"
IS GRAPHIC GREEN ?
YES
NO
LATCH ELEMENT 81 — "0"
LATCH ELEMENT 82 — "1"
LATCH ELEMENT 83 — "0"
IS GRAPHIC BLUE ?
YES
NO
LATCH ELEMENT 81 — "0"
LATCH ELEMENT 82 — "0"
LATCH ELEMENT 83 — "1"
LATCH ELEMENT 81 — "1"
LATCH ELEMENT 82 — "1"
LATCH ELEMENT 83 — "1"
GRAPHIC FORMATION
(WRITE DATA IN GRAPHIC MEMORY)
END