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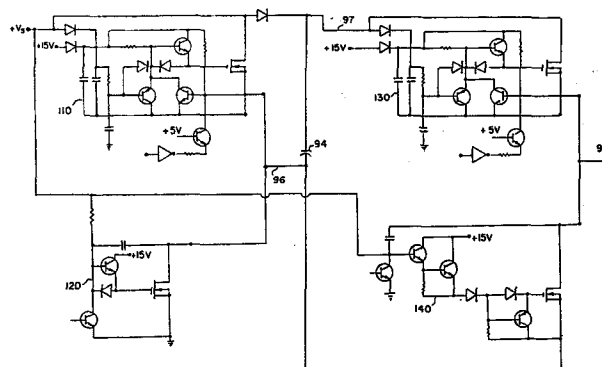
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54 **Driving system for plasma panel display system.**

57 A driving system for a plasma panel display which uses VFETs for output switches controls the transition time of an output waveform 95 to a constant time. Transformerless circuitry (110, 130) for communicating low voltage digital logic signals across a floating boundary to VFET control circuitry is provided. Low voltage control circuitry (120, 140) is isolated from high voltage sources by semiconductor circuitry which eliminates the need for transformer isolation techniques. In an alternative embodiment, the transition of an output waveform is controlled at a constant slew rate.



DRIVING SYSTEM FOR PLASMA PANEL DISPLAY SYSTEM

This invention relates to circuits for driving conductor arrays in a plasma display system.

In conventional AC plasma display systems, arrays of parallel conductors are disposed orthogonally to each other on opposite sides of a gas filled panel, the intersections of the conductor arrays forming gas cells. The gas cells may be selectively ionized by application of discharge voltages in order to produce a visual display having a specific configuration and information content. When discharged, the cells produce a wall charge voltage which combines with a lower level sustain signal.

Plasma display systems are provided with circuitry for producing the sustain signal, composed of a periodic voltage, which is used to continuously discharge the gas cells at a frequency sufficient to maintain the discharge. By so doing, the specific configuration and information content of the visual display is maintained in its then present state. The sustain signal is also used to normalize a write or an erase operation. The peak sustain voltage is typically on the order of 200 volts.

The generation of the high voltage sustain signals is controlled by low voltage circuitry which is responsive to digital logic signals from an external processor or controller, the content of the digital logic signals being dependent on the operation required of the plasma system. Since the sustain signals and the digital logic signals are at different voltage levels, means must be provided for communicating between these signals in order to operate the plasma system. One method of providing such communication is shown in US Patents A-3,973,253 and A-4,097,856 which employ pulse transformers for

communicating a low voltage signal to a high voltage signal while simultaneously providing isolation between the high and low voltage circuitry. It would be desirable to eliminate the use of pulse transformers and replace them with low cost semiconductor circuitry.

One problem associated with the use of plasma display systems is controlling the transition times of a switched waveform such as the sustain voltage. Techniques are available for controlling the transition times at low slew rates; however, it becomes increasingly difficult to do so as the slew rates and operating voltages required to drive an AC plasma panel display system increase. The problem becomes particularly pronounced when high power vertical field effect transistors (VFETs) are employed in the plasma panel driving circuits. High power VFETs exhibit wide bandwidth characteristics making them prone to oscillation if their gate drive circuitry does not have an even higher frequency response. VFETs also have a very high input capacitance (typically on the order of 1200 pF) which necessitates the use of low impedance drive circuitry. Additionally, there is a variation in gain from one device to another, thus requiring a different gate to source input from one device to another in order to obtain the same output slew rate.

Previous plasma panel driving circuits have made little attempt to control the transition times, i.e. rise and fall times, of a switched waveform such as the sustain voltage. Instead, these circuits have been designed to provide a transition time that is as fast as possible. In large plasma panels, very fast transition times cause high currents to flow through the system components.

It is an object of this invention to provide driving circuitry for a plasma panel display system which permits such transition times to be controlled to avoid unnecessarily high currents.

According to the invention we provide a system for driving a plasma panel display device having a plurality of discharge cells, comprising a sustain voltage source operable selectively to provide to each of said plurality of discharge cells a pulsating voltage, characterised in that said sustain voltage source includes a field effect transistor (FET) switch having an associated control circuit for controlling the transition time of said pulsating voltage to a constant time, said control circuit floating with the source potential of said FET switch, and in that a switching circuit is provided for receiving digital logic signals from an external source and for communicating said digital logic signals to said control circuit so as to energize said control circuit in response thereto, whereby a pulsating voltage having a constant transition time is provided to said plurality of discharge cells in response to the input of said digital logic signals.

We further provide a system as claimed in Claim 1 wherein said control circuit means comprises a current source, said current source comprising a resistor connected at one terminal to a source of D.C. voltage and connected at the other terminal to the reference point of said source of D.C. voltage.

In an embodiment of the invention, to be described below, the transition of the sustain waveform is controlled to a constant time. The transition time is set to a constant time independent of the varying voltage through which the circuitry might transit. Vertical Field Effect Transistors (VFETs) are used as the output switches for providing the periodic sustain voltage to the gas cells in the plasma panel display system. The source of some of the VFETs can float up and down when the VFETs are not in use, and the gate of these VFETs remains connected with its source when the VFET is not in use. The low voltage circuitry used to drive the VFETs also floats with the source potential.

The transformers conventionally used to communicate digital logic signals from an external controller or processor to the floating low voltage drive circuitry are replaced with low cost semiconductor circuitry. In this manner, the digital logic signals are communicated directly to the low voltage drive circuitry across a high voltage boundary without the need for transformers.

In an alternative embodiment, the transition time of the sustain waveform is controlled to a constant slew rate.

The invention, and the manner in which it may be put into effect, will be clearly understood from the following description of the embodiments referred to above, when read in conjunction with the drawings, in which :-

Fig. 1 is a block diagram of a driving system for a plasma panel display system constructed in accordance with the present invention.

Fig. 2 is a diagram of a switched waveform such as one produced by the instant invention.

Fig. 3 is a schematic of a ground referenced circuit which controls the fall time of the output waveform to a constant time according to the present invention.

Fig. 4 is a schematic of a floating reference circuit which controls the rise time of the output waveform to a constant time and which provides isolation between the input switching circuit and the floating low voltage circuitry according to the present invention.

Fig. 5 is a schematic of a circuit which controls the falling edge of the output waveform to a constant slew rate according to the present invention.

Fig. 6 is a schematic of a circuit which controls the rising edge of the output waveform to a constant slew rate and which provides isolation between the input switching circuit and the floating low voltage circuitry according to the present invention.

Fig. 7 is a schematic of a circuit according to the instant invention which incorporates isolation between the low voltage driving circuitry and the high voltage output circuitry.

Fig. 8 is a schematic of a complete driving system for a plasma panel display system which uses the circuits of the present invention.

Best Mode for Carrying Out the Invention:

Referring to Fig. 1, the driving system 20 of the present invention contains switching circuitry 12 for receiving digital logic signals (typically TTL levels are used) from an external controller 11 or an external processor (not shown). These logic signals are used only for control purposes; i.e., to control the sustain operation of the plasma panel. They do not provide information which is to be displayed on the screen of the plasma panel.

Switching circuitry 12 receives the incoming digital logic signals and then communicates the information provided by these signals to control circuitry 13. It is control circuitry 13 which sets the transition time of the sustain waveform which is provided by VFET output 14 to gas cells 16. Control circuitry 13 comprises low voltage gate drive circuitry for driving the gate of VFET 14, a current source, and gate isolation circuitry for isolating high voltage source 15 from the low voltage gate drive circuitry. These functions will be explained in more detail with relation to Figs. 3-7.

An example of the sustain waveform which is provided by VFET output 14 to gas cells 16 is shown in Fig. 2. As described more fully in U.S. Patent 4,263,534 (IBM Docket KI9-79-005), 200 volt VFETs having characteristics which make the devices useable in plasma panels are not readily available. Thus, to obtain a 200 volt peak-to-peak waveform, circuitry must be designed containing two stages with each stage employing 100 volt VFETs. The first stage provides a 0-100 volt peak-to-peak swing as shown by points 17 and 18 in the sustain waveform shown in Fig. 2. The output of the first stage is then input to the second stage so that the second stage will provide a voltage swing from 100 to 200 volts as shown by points 18 and 19 in Fig. 2. Taken together, the two stage circuitry provides a 200 volt peak-to-peak waveform.

The term "transition time" as defined herein refers to either the rise time or the fall time. The rise times that are controlled by the present invention are the rise times of the individual stages, i.e., the circuits disclosed herein control

the rise time of the sustain waveform from 0-100 volts, corresponding to the first stage of a 0-200 volt circuit and from 100-200 volts, corresponding to the second stage of a 0-200 volt circuit. Rise time, as defined herein, is the time it takes for a waveform to rise from 10% of its maximum value to 90% of its maximum value. Likewise, the fall times that are controlled by the present invention are the fall times of the individual stages. Fall time, as defined herein, is the time it takes for a waveform to fall from 90% of its maximum value to 10% of its maximum value.

Two other terms, "rising edge" and "falling edge", refer to the leading and trailing edges of the signals which rise and fall respectively. The rising edge is that part of the waveform that begins at the lowest point on the waveform and ends at the highest point; the falling edge is that part of the waveform that begins at the highest point on the waveform and ends at the lowest point. The rising edge has a positive slope while the falling edge has a negative slope.

Fig. 3 is a schematic of a circuit which enables the fall time of a switched waveform to be controlled to a constant time. The source of VFET 26 is connected to ground potential, while the drain is connected to the output terminal 28. When the base of transistor 25 is held low, transistor 23 turns on and drives the gate of VFET 26, thus turning the device ON. When the base of transistor 25 goes high, it is turned ON. By so doing, the base of transistor 23 is pulled down to approximately ground potential turning transistor 23 OFF, thus removing the drive current to the gate of VFET 26, whereby VFET 26 is turned OFF. Switch 27 represents a connection to

another circuit which will be discussed in detail in relation to Fig. 8.

The current used to drive the gate of VFET 26 is provided from a current source consisting of resistor 21 connected between the high voltage supply V_s (typically 100 volts) and approximately ground potential. Since the value of high voltage supply V_s will typically fluctuate, the current source will likewise vary as the value of V_s . The second terminal of resistor 21 is connected to the base of transistor 23 whereby this terminal will thus be above ground potential by an amount equal to the base-emitter voltage of transistor 23 plus an amount dependent on the transconductance, g_m , of VFET 26. As the transconductance of VFET 26 changes, the gate to source voltage changes. Note that the transconductance, g_m may be approximated as the gain of VFET 26 containing a term dependent on the gate to source voltage. As the gate to source voltage changes, the voltage across resistor 21 changes and likewise the current through resistor 21. Compared to the value of the high voltage supply; i.e., 100 volts, this change in voltage is negligible.

The current supplied by this current source will be split between the base of transistor 23 and capacitor 22. As output node 28 moves toward ground potential, capacitor 22 begins to draw more current from the base of transistor 23. In this manner, the current through capacitor 22 acts as a feedback control to regulate the amount of drive current supplied to the gate of VFET 26. The feedback current used to control drive current to the gate of VFET 26 is equal to the value of capacitor 22 multiplied by the change in voltage with time, i.e., $I = C \frac{dv}{dt}$. The value of capacitor 22 is a constant. As noted above, the supply current is a function of

supply voltage V_s , namely V_s/R , where R is the value of resistor 21. Since the gain of transistor 23 is chosen to be quite high, the value of the base current supplied to transistor 23 will be small compared to the current drawn by capacitor 22. As a good approximation, the current through resistor 21 will be equal to the current through capacitor 22. Substituting the value of the current through resistor 21 into the above equation gives $V_s/R = C \frac{dv}{dt}$. If dv now represents a transition through the entire V_s range, then $dv = V_s$ and thus $dt = R \times C$, where C is the value of capacitor 22. Thus the rise time of the output voltage is set to a constant time which is independent of the varying voltage through which the circuit might transit.

Fig. 4 is a modified version of the fall time control circuitry of Fig. 3, which also incorporates switching circuitry 12 for receiving digital logic signals from an external controller or processor via terminal 31. Transistors 34 and 35 perform the same functions as transistors 23 and 25 in Fig 3, while resistor 46 and capacitor 42 perform the same functions as resistor 21 and capacitor 22 in Fig. 3. The gain of transistor 34 tends to be small, so transistor 36 is added to boost the gain of transistor 34. In this manner, sufficient current is supplied to the gate of VFET 30 to turn that device ON. In this circuit, the source of VFET 30 is output terminal 45. Capacitor 44, which has approximately the supply voltage V_s across it and resistor 46, provides a current source equal to V_s volts divided by the value of resistor 46. In actuality, resistor 46 has one terminal connected to a first terminal of capacitor 44 and the other terminal connected to the base of transistor 36 whereby the base of transistor 36

serves as the reference point with respect to the voltage across resistor 46. Switch 29 represents a connection to another circuit which will be explained in more detail in relation to Fig. 8.

Switching circuitry 12 in Fig. 4 comprises inverter 32 and transistor 33 which is connected in the common base configuration such that the source of VFET 30 floats when the device is not being used. The source voltage floats up and down between 0 and V_s volts when the device is not in use whereby the control circuitry which drives VFET 30 must also float. Therefore, digital logic signals must be communicated across a floating boundary. Although shown here as an inverter in the preferred embodiment, any type of logic gate may be used to receive the digital logic signals at input node 31.

Transistor 33 functions as a switched current source to communicate the digital logic signals (typically, TTL referenced to ground) up to the floating rise time control circuitry. When an up level signal is applied to inverter 32 at terminal 31, transistor 33 turns ON. This, in turn, holds transistor 35 OFF, allowing enough of the current through resistor 39 to be directed to the base of transistor 34 so as to turn that device ON. By so doing, sufficient drive current is provided to the gate of VFET 30 to turn the device ON.

Fig. 5 is a schematic of a circuit that enables the falling edge of a switched waveform to be controlled to a constant slew rate. The source of VFET 51 is connected to ground potential, while the drain serves as output terminal 57. When the base of transistor 55 is held low, transistor 54 turns on and drives the gate of VFET 51, thus turning that device ON. When the base of transistor 55 goes

high, it is turned ON. By so doing, the base of transistor 54 is pulled down to approximately ground potential turning transistor 54 OFF, thus providing no drive current to the gate of VFET 51.

The slew rate $\frac{dv}{dt}$, i.e., the change in the output voltage at terminal 57 with time, is equal to the feedback current used to drive the gate drive circuitry of VFET 51 divided by the value of capacitor 53. The current used to drive VFET 51 is provided from a constant current source 52. The value of capacitor 53 is fixed. Since the value of the current supplied to the gate control circuitry of VFET 51 is constant, then the slew rate $\frac{dv}{dt}$ will be constant. This means that the falling edge of the output voltage, i.e., the sustain waveform, is controlled at a constant slew rate. Thus the falling edge of the sustain waveform will be fixed to a constant slew rate, i.e., have a constant slope even when the output voltage changes value. An incremental change in dv will be offset by an incremental change in dt so as to maintain a constant dv/dt value.

Fig. 6 is a modified version of the falling edge control circuitry of Fig. 5 which also incorporates switching circuitry 12 for receiving digital logic signals from an external controller or processor. Transistors 73 and 78 perform the same functions as transistors 54 and 55 in Fig. 5 to supply sufficient current to the gate of VFET 61 to turn that device ON. In this circuit, the source of VFET 61 is the output terminal 62. The operation of the switching circuitry 12 in Fig. 6 is identical to that explained heretofore in relation to Fig. 4.

The circuit of Fig. 6 has a constant current source different than the current source used in Fig. 4. When transistor 78 is turned ON (holding

VFET 61 OFF) and the source of VFET 61 is at ground, capacitor 68 is charged from V_{CC} through diodes 67 and 72 to a D.C. voltage level equal to V_{CC} minus the voltage drops across diodes 67 and 72 and the saturation voltage of transistor 78. When transistor 73 is turned ON, the charge on capacitor 68 is driven up by the emitter of transistor 73 whereby the current through resistor 69 is equal to the voltage across capacitor 68 minus the base-emitter voltage of transistor 77 plus the base-emitter voltage of transistor 73, divided by the value of resistor 69. Since the base-emitter voltages of transistors 73 and 77 are approximately equal, the current through resistor 69 is equal to the voltage across capacitor 68 divided by the value of resistor 69. In this manner, a constant current source is created.

The circuit shown in Fig. 7 is a modification of the circuit in Fig. 3 which additionally encompasses gate control isolation circuitry for isolating the low voltage gate control circuitry from a high voltage source. The drain of VFET 82 is the output terminal 93. When switch 92 is in the V_S position, diode 87 is reverse biased and provides isolation between the high voltage V_S and the low voltage gate drive circuitry which comprises transistors 83, 84, and 85 as well as the current source formed by the connection of resistor 81 between voltage supply V_S and the base of transistor 84. At this time, it is desired to hold VFET 82 OFF which requires keeping the gate of VFET 82 from reaching a voltage level sufficient to turn the device ON. The gate voltage of VFET 82 equals the sum of the source voltage of VFET 82, the base-emitter voltage of transistor 89, and the voltage across resistor 91. The only one of

these terms that is controllable is the voltage across resistor 91. It would be prohibitively difficult to make a resistor with such a low resistance that the voltage developed across it would be small enough to hold VFET 82 OFF. Since diode 88 is reverse biased, the current through resistor 91 consists entirely of the base current of transistor 89. Since the emitter current of a transistor is equal to the gain of the transistor times the base current of the transistor, the voltage developed across resistor 91 is equal to the emitter current of transistor 89 times the value of resistor 91 divided by the gain of transistor 89. By choosing a large enough gain for transistor 89, the voltage across resistor 91 can be kept at a low level without requiring the value of resistor 91 to be prohibitively small.

When switch 92 is in the ground position, both diodes 87 and 88 are forward biased so transistor 89 is held off. At this time, the circuit functions the same as the one described in relation to Fig. 3.

Fig. 8 shows a complete embodiment of a driving system for providing a constant rise time of a 200 volt peak-to-peak sustain voltage. The driving system shown in Fig. 8 encompasses the circuits in Figs. 3, 4, and 7, the details of which have been described supra.

Initially, circuits 110 and 130 are OFF and circuits 120 and 140 are ON. At this time, line 96 is pulled down to ground. Thus capacitor 94 has 100 volts across it and line 97 is at 100 volts. Line 95 which is output to the plasma cells is now at ground potential. When circuit 120 turns OFF and circuit 110 turns ON, line 96 is pulled up to 100 volts causing line 97 connected to the top terminal

of capacitor 94 to be pulled up to 200 volts. Capacitor 94 still has 100 volts across it. Line 97 thus provides a 200 volt source to circuit 130. By so doing, line 95 outputs 100 volts to the gas cells. When circuit 140 turns off and circuit 130 turns on, line 95 outputs 200 volts to the gas cells. Thus, the circuitry shown in Fig. 8 provides a 0-200 volt output signal comprising a first stage which generates a 0-100 volt output signal, and a second stage which generates a 0-100 volt signal referenced to the output of the first stage such that output line 95 provides a 0-200 volt ground referenced signal to the gas cells.

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and detail may be made therein without departing from the spirit and scope of the invention.

CLAIMS

1 According to the invention we provide a system for driving a plasma panel display device having a plurality of discharge cells, comprising a sustain voltage source operable selectively to provide to each of said plurality of discharge cells a pulsating voltage, characterised in that said sustain voltage source includes a field effect transistor (FET) switch having an associated control circuit for controlling the transition time of said pulsating voltage to a constant time, said control circuit floating with the source potential of said FET switch, and in that a switching circuit is provided for receiving digital logic signals from an external source and for communicating said digital logic signals to said control circuit so as to energize said control circuit in response thereto, whereby a pulsating voltage having a constant transition time is provided to said plurality of discharge cells in response to the input of said digital logic signals.

2 A system as claimed in Claim 1 wherein said control circuit means comprises a current source, said current source comprising a resistor connected at one terminal to a source of D.C. voltage and connected at the other terminal to the reference point of said source of D.C. voltage.

3 A system for driving a plasma panel display device having a plurality of discharge cells, comprising in combination a sustain voltage source operable selectively to provide to each of said plurality of discharge cells a pulsating voltage, characterised in that said sustain voltage source includes a field effect transistor (FET) switch having an associated control circuit for controlling the

transition time of said pulsating voltage at a constant slew rate, said control circuit floating with the source potential of said VFET switch, and in that a switching circuit is provided for receiving digital logic signals from an external source and for communicating said digital logic signals to said control circuit so as to energize said control circuit in response thereto, whereby a pulsating voltage having a constant slew rate is provided to said plurality of discharge cells in response to the input of said digital logic signals.

4 A system for driving a plasma panel display device according to Claim 3 wherein said control circuit means comprises a constant current source, said constant current source comprising a resistor connected at one terminal to the first terminal of a capacitor and connected at the other terminal to a point which is substantially at the same potential as the second terminal of said capacitor, said capacitor being charged to a substantially fixed potential by a voltage source.

5 A system as claimed in any of Claims 1 to 4 wherein said switching circuit comprises a logic gate having an input for receiving digital logic signals, and a switched current source for receiving logic signals from the output of said logic gate and for communicating said logic signals to said control circuit means.

6 A system as claimed in Claim 5 wherein said switched current source comprises a bipolar transistor connected in the common base configuration, the emitter of said bipolar transistor connected to the output of said logic gate and the collector of said bipolar transistor connected to said control circuit means.

7 A system device as claimed in Claim 6 wherein said control circuit means further comprises low voltage gate drive circuitry for

driving the gate of said FET switch and gate control isolation means for isolating said low voltage gate drive circuitry from a high voltage source when the source of said VFET switch is floating above ground potential.

8 A system as claimed in Claim 7 wherein said gate control isolation means comprises a transistor, the emitter of which is connected to the gate of said FET switch and the collector of which is connected to the source of said FET switch and to said high voltage source, a resistor having one terminal connected to the base of said high gain transistor and having the other terminal connected to the collector of said high gain transistor, a first diode having its cathode connected to the emitter of said high gain transistor and having its anode connected to the base of said high gain transistor, and a second diode having its cathode connected to the anode of said first diode and having its anode connected to the output of said low voltage gate drive circuitry.

9 A system as claimed in any preceding claim in which said FET switch includes a vertical field effect transistor (VFET).

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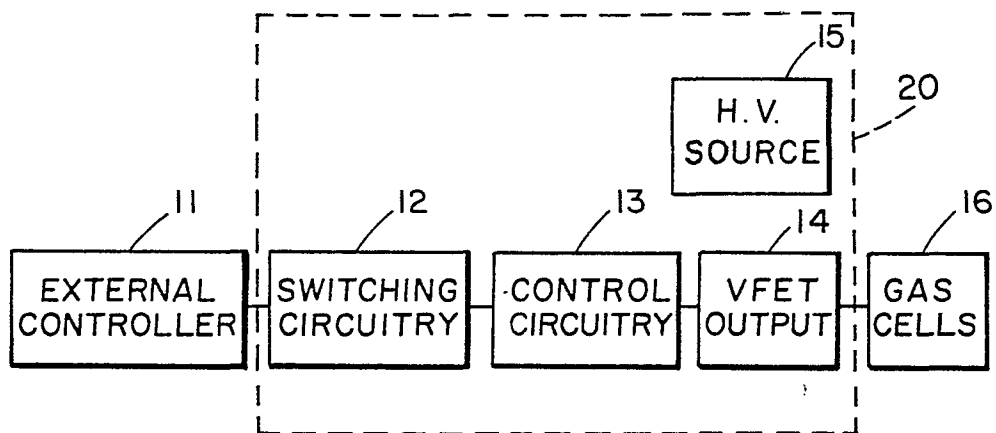


FIG. 1

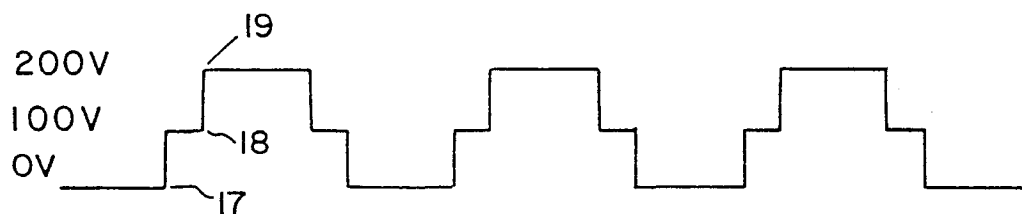


FIG. 2

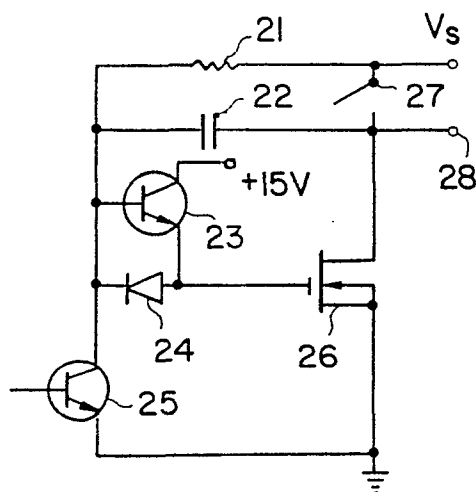


FIG. 3

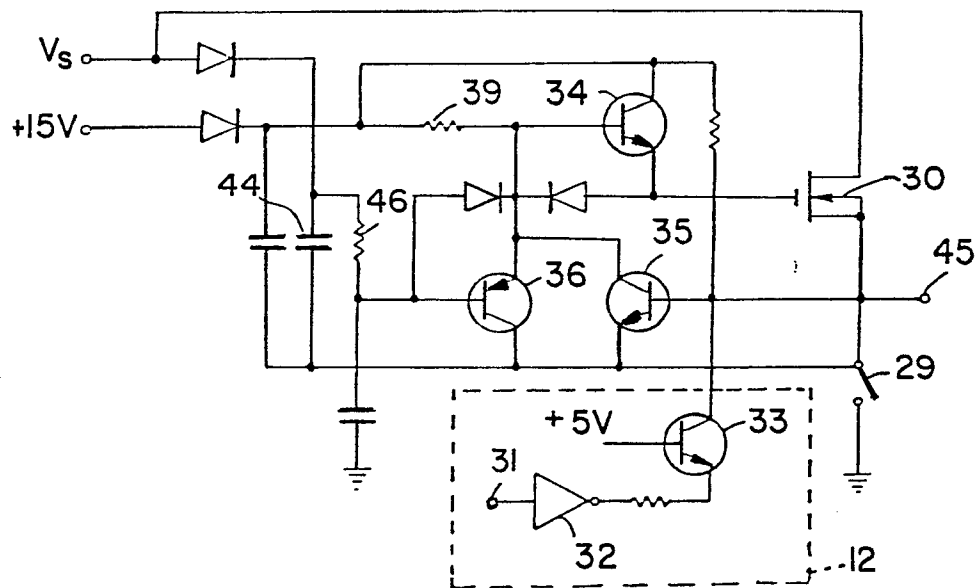


FIG. 4

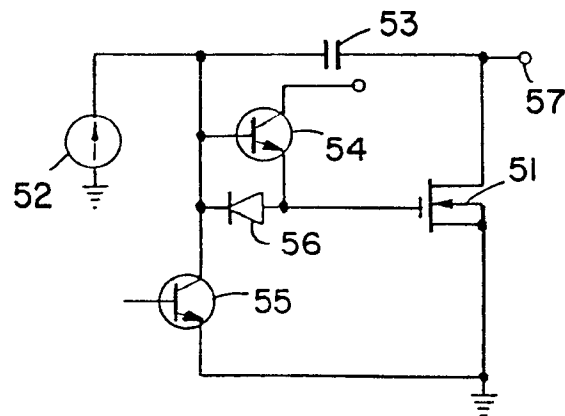


FIG. 5

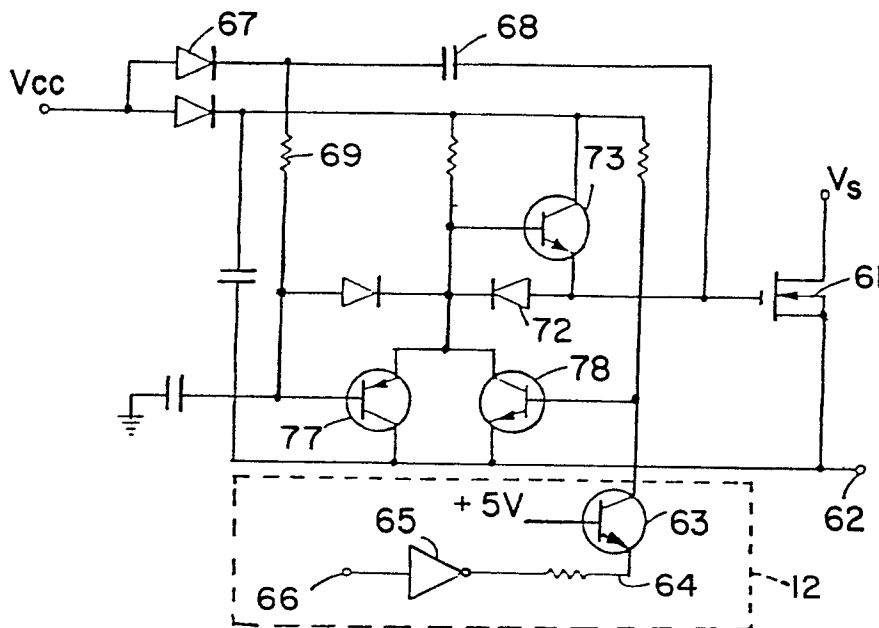


FIG. 6

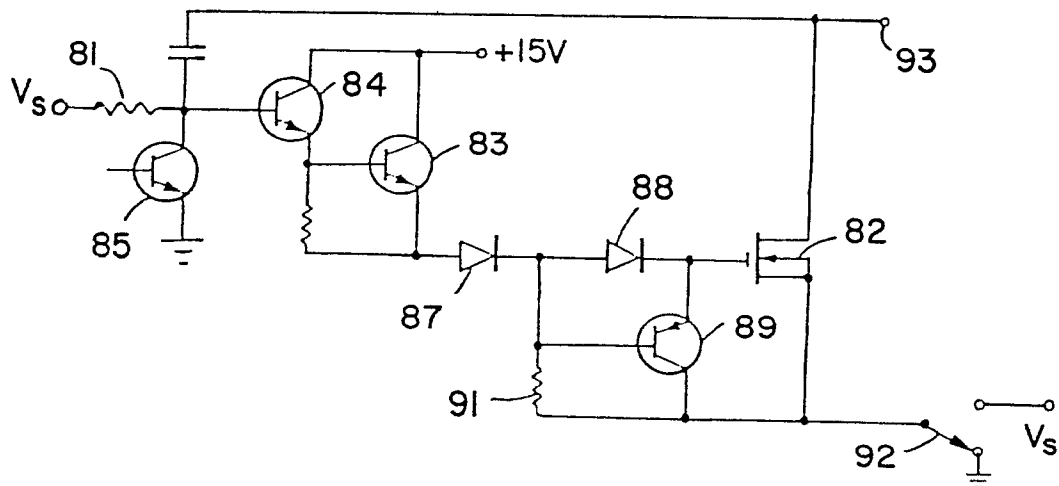


FIG. 7

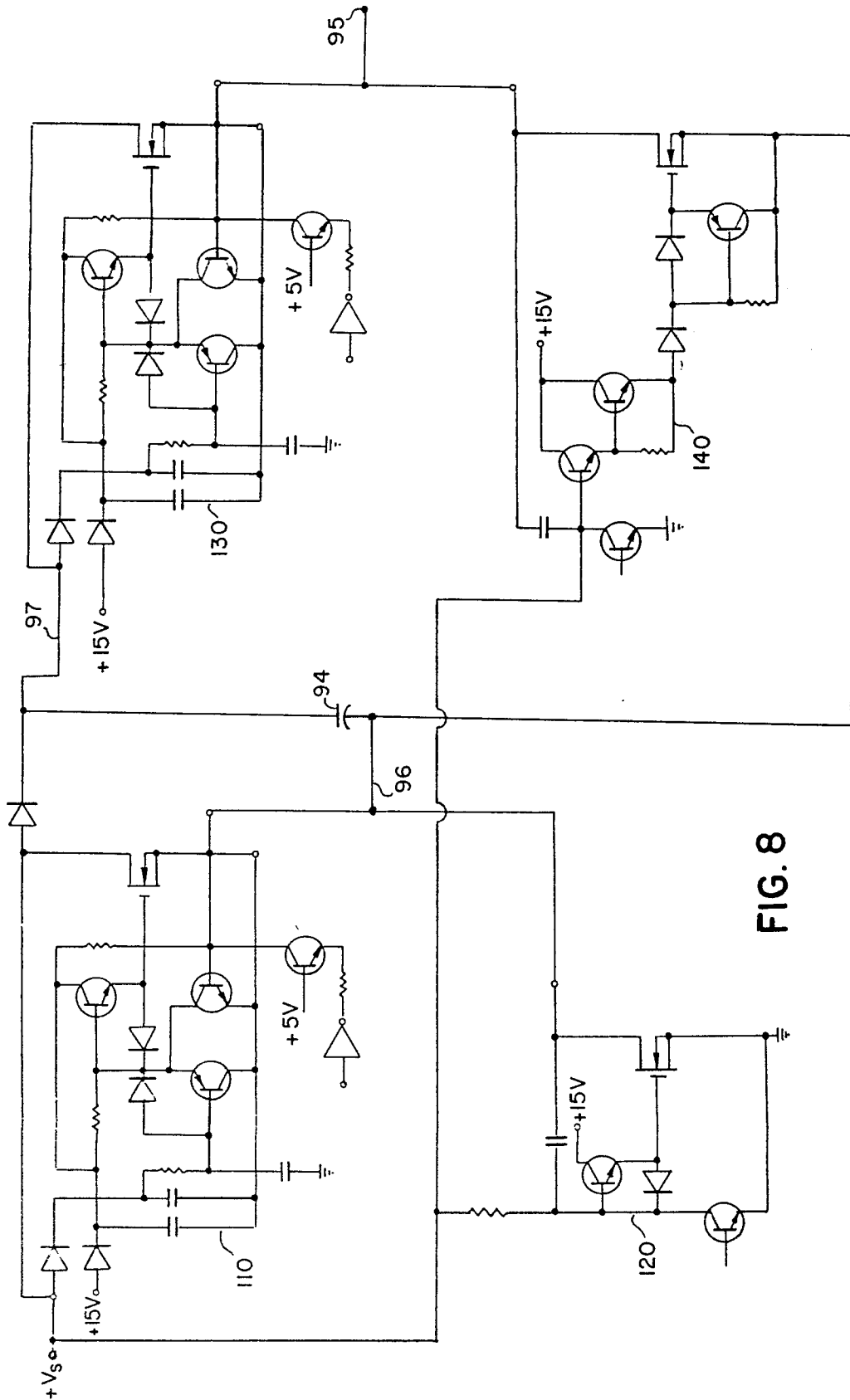


FIG. 8