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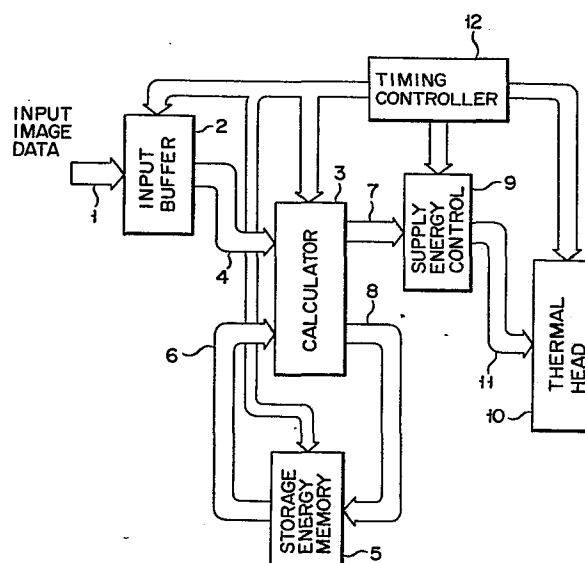
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**Thermal recording system.**

A recording system has a thermal head (10) having a plurality of thermal heating resistive elements aligned in line and a drive circuit for selectively energizing the thermal heating resistive elements to record image data for one line. The recording system also has a calculator (3) for calculating supply energy data supplied to each resistive element for recording one-line image data in accordance with the one-line image data and the storage energy stored in each of the resistive elements after the immediately preceding line is recorded. A control circuit (9) controls the supply energy supplied to each resistive element through drive circuits in response to the supply energy data.



- 1 -

Thermal recording system

The present invention relates to a thermal recording system.

Along with the development and popularity of data processing apparatus such as personal computers and word processors, recording apparatus have increased in importance as output terminal devices. Various types of recording or printing apparatus such as wire-dot, ink-jet and thermosensitive recording apparatus have been developed. Among these, a thermal recording apparatus is receiving most attention these days. The thermal recording apparatus has advantages in that a normal paper sheet can be used for recording, a noise level at the time of recording is low, a recording mechanism is simple, easy maintenance can be performed, and alteration of recorded data is impossible. Furthermore, along with the development of color output terminal devices such as a color CRT display, there arises a demand for a color recording apparatus. A color thermal recording apparatus can be easily arranged to perform good color reproduction. The color thermal recording apparatus is the most promising apparatus among various types of color recording apparatus.

In the conventional thermal recording apparatus, a number of thermal heating resistive elements are aligned in line, and the thermal heating resistive

elements are selectively supplied with current in accordance with a recording signal. This energizing cycle is then repeated to heat the resistive elements, so that an ink carried on an ink ribbon is melted by the heated resistive element. The ink is then transferred to the paper sheet so as to record an image on the sheet. Although the thermal recording apparatus has the above advantages, it has a drawback in that the recorded image becomes poor due to a heat retention or storage effect of the resistive elements as the recording speed increases. In order to increase the recording speed, an interval between energizing cycles is shortened. When a resistive element which was energized in the immediately preceding energizing cycle is reenergized after a short time interval, heat cannot be sufficiently lost. Therefore, when the same resistive element is successively energized at a short interval after the immediately preceding energizing cycle, the temperature of this resistive element continues to increase. In this manner, when the energizing cycles are repeated at short intervals, the present temperatures of the individual resistive elements differ due to their thermal history. When resistive elements having different temperatures are simultaneously energized, areas at which inks are melted differ, thereby resulting in an image having a nonuniform density. In particular, when characters are recorded, the ink is often transferred to a narrow space which does not correspond to the image data, thus degrading legibility.

In order to solve the above problem, a system is proposed in Japanese Patent Publication No. 55-48631, wherein an energizing time of each thermal heating resistive element when mark data as recording data are continuously supplied is set to be shorter than that when the mark data follows space data. The energizing time of the subsequent energizing cycle of a given

thermal heating resistive element is switched in a two-step manner in accordance with whether or not the given resistive element was energized in the immediately preceding energizing cycle. According to this system, the above drawback can be eliminated to some extent.

However, in fact, this system cannot eliminate the nonuniform density of the recorded image since the thermal histories of the resistive elements still differ from each other, especially in high speed recording, due to insufficient controllability.

It is an object of the present invention to provide a thermal recording system capable of recording an image at a stable recording density.

It is another object of the present invention to provide a thermal recording system arranged to control supply energy to be supplied to thermal heating resistive elements for recording image data at the present time in consideration of a previous thermal history thereof.

A thermal recording system according to the present invention comprises a thermal head having a number of thermal heating resistive elements aligned in line, and drive circuit means for selectively energizing the thermal heating resistive elements, by current supply, in accordance with image data to print the image data on a line. The thermal recording apparatus has a calculation circuit means for calculating, from storage energy which would be stored in each thermal heating resistive element after image data of one line has been recorded and image data of the next line, supply energy to be supplied to each resistive element to record the image data of the next line and storage energy stored in each resistive element after the image data of the next line has been recorded. A control circuit means causes the drive circuit means of the thermal head to control energy supplied to each thermal heating resistive element in response to the

supply energy data from the calculation circuit means. The storage energy data is stored in a memory and is used for calculating the next supply and storage energy.

5 This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram of a thermal recording system embodying the present invention;

10 Fig. 2 is a data format used for calculating the storage energy of the *i*th thermal heating resistive element of the thermal head;

Fig. 3 is a block diagram of a storage energy memory shown in Fig. 1;

15 Figs. 4A and 4B are respectively timing charts for explaining the operation of the storage energy memory shown in Fig. 3;

Fig. 5 is a block diagram of a supply energy control section shown in Fig. 1;

20 Figs. 6A and 6B are diagrams for explaining the control of the supply energy;

Fig. 7 is a block diagram of drive circuits of the thermal head; and

Fig. 8 is a detailed diagram of one of the drive circuits shown in Fig. 7.

25 Fig. 1 shows the schematic configuration of a thermal recording or printing system embodying the present invention. Input image data or recording data 1 is supplied to an input buffer 2 and is properly processed therein. An output signal of the input  
30 buffer becomes an input signal 4 of a calculator 3 for calculating supply energy and storage energy of each thermal heat resistive element. The calculator 3 calculates the supply energy to each thermal heating resistive element and storage energy which would be  
35 stored therein after energization, in accordance with output data 4 of the input buffer 2 and output data 6 of a storage energy memory 5, and outputs calculated

supply energy data 7 and storage energy data 8 to a supply energy control 9 and the storage energy memory 5, respectively. The storage energy memory 5 stores storage energy data of each resistive element calculated from the beginning of printing up to the present moment. Storage energy data 6 read out from the storage energy memory 5 is supplied as the input signal 6 to the calculator 3. The storage energy data stored in the storage energy memory 5 are sequentially updated in units of thermal heating resistive elements every time new storage energy data are calculated by the calculator 3, so that the memory 5 holds the present storage energy data of the resistive elements. The supply energy control 9 temporarily stores supply energy data 7. The supply energy data 7 is read out in response to a readout signal and is supplied as input data 11 to a thermal head 10. The circuits of the thermal recording apparatus are controlled by a timing controller 12. The above description illustrates the overall configuration of the thermal recording apparatus of the present invention. The functions of the individual parts will be described in detail below.

In this embodiment, the supply energy to be supplied to each resistive element and the storage energy stored in each resistive element after energization are calculated in accordance with the input image data and the storage energy data stored in the memory 5. The relationship between the input image data and the storage energy data is shown in Fig. 2.

Assume that supply energy data and corresponding storage energy data are calculated for the  $i$ th thermal heating resistive element of the thermal head, that the thermal heating resistive elements aligned to the right of the  $i$ th element are the  $(i-1)$ th,  $(i-2)$ th, ..., elements, and that the thermal heating resistive elements aligned to the left of the  $i$ th element are the  $(i+1)$ th,  $(i+2)$ th, ..., elements. In this embodiment,

the thermal head has an A4 width and comprises a line head of 12 dots/mm. Therefore,  $1 \leq i \leq 2592$ . The supply energy to be supplied to the  $i$ th resistive element is calculated from the input image data  $D_i$ ,  $D_{i\pm 1}$ , and  $D_{i\pm 2}$  respectively to the  $i$ th,  $(i\pm 1)$ th and  $(i\pm 2)$ th resistive elements, and storage energy data  $Q_i$ ,  $Q_{i\pm 1}$  and  $Q_{i\pm 2}$  thereof. Similarly, the storage energy of the  $i$ th resistive element after energization is calculated from the input image data  $D_i$ ,  $D_{i\pm 1}$ , and  $D_{i\pm 2}$  respectively supplied to the  $i$ th,  $(i\pm 1)$ th and  $(i\pm 2)$ th resistive elements, and storage energy data  $Q_i$ ,  $Q_{i\pm 1}$  and  $Q_{i\pm 2}$  thereof. The energy data for each resistive element is represented by 4-bit data.

Fig. 3 shows the configuration of the input buffer 2 and the storage energy memory 5. In this embodiment, the image data are stored in an image memory 20. The image data is read out as the 8-bit parallel input image signal 1 from an image memory 20 in response to a signal  $\overline{MR}$  generated from the timing controller 12, and is loaded into a shift register 21 in response to a signal  $\overline{LD}$ . The shift register 21 performs parallel-to-serial conversion. The image data 1 is loaded into the next shift register 22 in a serial manner in response to a signal  $\overline{SRCLK}$  generated after loading of image data into the shift register 21. When the 8-bit data is read out from the shift register 21 in response to the signal  $\overline{SRCLK}$ , the timing controller 12 stops generating the signal  $\overline{SRCLK}$  and starts generating the signal  $\overline{MR}$  so that the next image data is read out from the image memory 20. The above operation is repeated until the image data corresponding to one line are read out from the image memory 20. Each bit of the image signal corresponds to a resistive element for one-dot display.

The parallel-to-serial conversion is performed by the shift register 21 to calculate the supply energy and the storage energy in units of resistive elements.

However, where the image data is serially received, it may be directly loaded into the shift register 22. The shift register 22 serves to extract the image data  $D_i$ ,  $D_{i\pm 1}$  and  $D_{i\pm 2}$  (to be supplied to the calculator 3) from the serial image data taken from the shift register 21.

In this embodiment, as shown in Fig. 2, the data 4 supplied to the calculator 3 comprise input image data to the  $i$ th,  $(i\pm 1)$ th and  $(i\pm 2)$ th resistive elements. Therefore, among the outputs of the shift register 22, the 5-bit image data corresponding to the  $i$ th,  $(i\pm 1)$ th and  $(i\pm 2)$ th resistive elements is supplied to the calculator 3.

A random access memory (RAMA) 23, latches 24, 25, 26, 27 and 28, adders 29 and 30, a write address counter 31, a read address counter 32 and a selector 33 constitute the storage energy memory 5 shown in Fig. 1. The RAMA 23 stores storage energy data of the resistive elements. Addresses of the RAMA 23 correspond to the respective resistive elements of the thermal head. In this embodiment, the address counters 31 and 32 designate 2592 addresses. The storage energy data 8 calculated by the calculator 3 has four bits. The 4-bit storage energy data 8 is supplied to a terminal  $D_{IN}$  of the RAMA 23 and is written at an address specified by the write address counter 31 in response to a signal  $\overline{WR}$  generated from the timing controller 12. When the signal  $\overline{WR}$  is not supplied to a terminal  $\overline{WR}$  of the RAMA 23, the 4-bit storage energy data stored at the address designated by the read address counter 32 is read out to a terminal  $D_{OUT}$  of the RAMA 23. Each of the latches 24 to 28 comprises a 4-bit latch which latches a 4-bit input signal in response to a signal  $\overline{LATCH}$  generated by the timing controller 12, and holds the latched data until the next signal  $\overline{LATCH}$  is supplied thereto. The latches 24 to 28 are connected in cascade to constitute a shift register so that 4-bit data is



sequentially shifted toward the output stage every time the signal LATCH is supplied thereto.

The storage energy data of a first resistive element which is specified by the read address counter 32 is read out from the terminal  $D_{OUT}$  of the RAMA 23 and is latched by the latch 24 in response to a first LATCH signal. The count of the read address counter 32 is incremented by one in response to the first LATCH signal, so that the storage energy data of a second resistive element is read out from the terminal  $D_{OUT}$ . In response to the next LATCH signal, the storage energy data of the second resistive element is latched by the latch 24. At the same time, the storage energy data of the first resistive element is latched by the latch 25.

In this manner, each time the LATCH signal is issued, the storage energy data from the RAMA are sequentially shifted. When the storage energy data  $Q_i$  of the  $i$ th resistive element is latched by the latch 26, storage energy data of the  $(i+1)$ th,  $(i+2)$ th,  $(i-1)$ th and  $(i-2)$ th resistive elements are latched by the latches 25, 24, 27 and 28, respectively.

As previously described, the supply energy data of the  $i$ th resistive element and the storage energy data after energization thereof are calculated in accordance with the input image data to the  $i$ th,  $(i\pm 1)$ th and  $(i\pm 2)$ th resistive elements, and with storage energy data thereof obtained to date. In other words, the supply energy data and the storage energy data can be calculated in accordance with data having a total of 25 bits (i.e., 5-bit data from the shift register 22 and the 20-bit ( $4 \text{ bits} \times 5$ ) storage energy data from the latches 24 to 28).

However, a calculation with 25 bits becomes complicated, so that the following simple operation is performed in practice.

The calculation process is based on a well-known

equation of heat conduction as follows:

$$\partial T / \partial t = a(\partial^2 T / \partial x^2 + \partial^2 T / \partial y^2 + \partial^2 T / \partial z^2) + \dot{q} / \rho C \quad \dots (1)$$

5 where

T : temperature

a : heat diffusion ratio

$\dot{q}$  : heat energy per unit volume and unit time

$\rho$  : density

10 C : specific heat

In order to control the supply energy for the thermal head in accordance with a digital calculation, a solution to equation (1) must have a format which is readily applicable to calculation by a digital circuit.

15 Assume that the printing period is defined as a time increment  $\Delta\tau$ , and that the pitch of the array of thermal heating resistive elements, the width of the resistive element along the direction perpendicular to the array, and the thickness of a glass layer immediately under the resistive element are defined as spatial increments  $\Delta x$ ,  $\Delta y$  and  $\Delta z$ . Also assume that the temperature in the vicinity of the  $i$ th resistive element in a given printing period  $n$  is defined as  $T_i^n$ . The energy balance at the point  $i$  is given by the following general equation in the form of a forward difference equation:

$$\sum_{j=1}^5 (T_j^n - T_i^n) / R_j + q_i^n - q_0 = C_i (T_i^{n+1} - T_i^n) / \Delta\tau \quad \dots (2)$$

30

where

$$T_1^n = T_{i-1}^n, \quad R_1 = (\Delta x / \Delta y \Delta z) \cdot (1/k)$$

$$T_2^n = T_{i+1}^n, \quad R_2 = R_1$$

$$T_3^n = T_{Ui}^n, \quad R_3 = (\Delta y / \Delta z \Delta x) \cdot (1/k)$$

35  $T_4^n = T_{Di}^n, \quad R_4 = R_3$

$$T_5^n = T_0, \quad R_5 = (\Delta z / \Delta x \Delta y) \cdot (1/k)$$

$T_0$  is the room temperature,  $k$  is the heat conductivity,

$q_0$  is the energy used for activating a coloring agent, and  $q_i^n$  is the energy supplied from a resistive element.

The energy  $q_0$  must be kept constant to obtain the optimum printing quality by means of the thermal head.

5 The energy  $q_0$  is determined by a time integral of the temperature gradient in the direction toward the coloring agent. If a pulse width  $t_i^n$  of a pulse applied to a thermal heating resistive element to determine the energizing time is a controllable

10 factor, the energy  $q_0$  depends on  $T_i^n$  indicating the storage state and the energy  $q_i^n((V^2/R) \cdot t_i^n)$  which is a function of  $T_i^n$ .

In order to keep the energy  $q_0$  constant, such  $t_i^n$ , a function of  $T_i^n$ , as to keep  $q_0$  constant must

15 be obtained. A distance between the thermal heating resistive element and the coloring agent is shorter than the dimensions of the resistive element, so that the equation can be dealt with as a matter of one-dimensional nonsteady heat conduction. The present

20 inventors obtained the following solution:

$$t_i^n = K_{E1} \cdot D_i^n \{ [1 + K_{E2}(1 - Q_i^n)] / [1 - K_{E3}(1 - Q_i^n)] \}^2 \dots (3)$$

where  $K_{E1}$ ,  $K_{E2}$  and  $K_{E3}$  are constants, respectively,

25  $D_i^n$  is printing data which indicates "1" (mark) or "0" (blank) and  $Q_i^n = T_i^n / (T_C - T_0)$  ( $T_i^n \leq T_C =$  a constant normalized temperature). The supply energy  $q_i^n$  is determined by equation (3). As a result,  $T_i^{n+1}$ , that is, the temperature during the next printing period

30 can be predicted from equation (2).

$T_i^{n+1}$  is in practice a function of not only  $T_i^n$  and  $T_{i+1}^n$  but also  $T_{U_i}^n$  and  $T_{D_i}^n$ . However, the following equation can be obtained in consideration of the heat conduction and the recording or printing

35 speed:

$$\begin{aligned}
Q_i^{n+1} = & K_{Q1}\{Q_i^n + K_{Q2}(1 - Q_i^n)\sqrt{t_i^n}\} \\
& + K_{Q3}\{(Q_{i-1}^n + Q_{i+1}^n)/2\} \\
& + K_{Q2}(\sqrt{t_{i-1}^n} + \sqrt{t_{i+1}^n})\{1 - (Q_{i-1}^n + Q_{i+1}^n)/2\} \\
& \dots (4)
\end{aligned}$$

5

where  $K_{Q1}$ ,  $K_{Q2}$  and  $K_{Q3}$  are constants.

Equations (3) and (4) may be rewritten as follows:

$$t_i^n = f(Q_i^n, D_i^n) \quad \dots (5)$$

$$Q_i^{n+1} = g(Q_i^n, Q_{i\pm 1}^n, D_i^n, D_{i\pm 1}^n) \quad \dots (6)$$

10

The width  $t_i^n$  of the pulse applied to the resistive element can be understood to be calculated from the storage energy  $Q_i^n$  and the input image data  $D_i^n$ . Similarly, the storage energy data  $Q_i^{n+1}$  during the next printing period can be derived from the present storage energy distribution  $Q_{i+m}^n$  and the data stream  $D_{i+m}^n$  (where  $m = -1, 0, +1$ ) in accordance with equation (6).

15

The storage energies of the  $(i\pm 1)$ th resistive elements ( $(R_{i\pm 1})$ ) which influence the  $i$ th resistive element ( $R_i$ ) are assumed to be substantially identical to each other. Therefore, the arithmetic mean of the storage energy of the  $(i-1)$ th and  $(i+1)$ th resistive elements is used in equation (4).

20

In order that the solution of the difference equation (2) converges, the printing period must be shorter than about 3.8 msec when the resolution of the thermal head is 12 dots/mm; and the printing period must be shorter than about 2.1 msec when the resolution is 16 dots/mm. As the resolution is increased, heat tends to be conducted further than the adjacent volume unit consisting of one resistive element and glass layer immediately thereunder within a printing period. In view of such a phenomenon, the heat conduction from the volume units associated with the two adjacent resistive elements ( $R_{i\pm 1}$ ,  $R_{i\pm 2}$ ) on the right and left sides of the volume unit associated with the  $i$ th

30

35

resistive element ( $R_i$ ) is considered.

Equation (3) is of a form which can be easily handled in this embodiment. Various types of equations can be derived in accordance with: physical conditions  
5 such as the printing period, the head resolution, the head construction and the head material; the properties of the material; and an approximation method to obtain a solution.

The adders 29 and 30 are provided in Fig. 3 in  
10 consideration of thermal conduction from the adjacent volume units.

The adder 29 serves to calculate an average of 4-bit storage energy data of the  $(i+1)$ th and  $(i-1)$ th resistive elements obtained from the latches 25 and 27.  
15 Namely, the four more significant bits of the adder 29 are used as the storage energy data to be supplied to the calculator 3. Similarly, the adder 30 calculates the average value of the 4-bit storage energy data of the  $(i+2)$ th and  $(i-2)$ th resistive elements which  
20 are respectively obtained from the latches 24 and 28. The three more significant bits of the adder 30 are used as the storage energy data of the  $(i\pm 2)$ th resistive elements to be supplied to the calculator 3.

The 5-bit image data from the shift register 22,  
25 the 4-bit data of the  $i$ th resistive element from the latch 26, the 4-bit storage data of the  $(i\pm 1)$ th resistive elements from the adder 29, and the 3-bit storage energy data of the  $(i\pm 2)$ th resistive elements from the adder 30 are applied to the calculator 3.  
30 In other words, 16 bits in total are used.

The calculator 3 calculates the supply energy  $E_i^n$  to be injected in the  $i$ th resistive element, and the storage energy  $Q_i^{n+1}$  which will be stored in the  $i$ th resistive element until the  $i$ th element is  
35 again energized after the supply energy  $E_i^n$  has been injected in the  $i$ th element, in accordance with the input image data  $D_{i-2}$ ,  $D_{i-1}$ ,  $D_i$ ,  $D_{i+1}$  and  $D_{i+2}$  and

the storage energy data  $Q_{i+2}^n$ ,  $Q_{i+1}^n$ , and  $Q_i^n$  obtained to date.

5 The calculator 3 simulates the equation of heat conduction in accordance with equations (3) and (4) to provide prediction values of the proper supply energy, and storage energy in the next printing period. The supply energy data is applied to the thermal head 10 through the supply energy control 9. The storage energy prediction data is stored in the storage energy memory 5 and is used as input data to the calculator 3 in the next printing period. The contents of the storage energy memory 5 are updated every printing period.

15 In this embodiment, the calculator comprises a ROM. The supply energy data and the storage energy data which have been calculated by a computer in advance are stored in the ROM. The 5-bit image data and the 11-bit storage energy data are used as 16-bit address data of the ROM. The 4-bit supply energy data 20 7 and the 4-bit storage energy data 8 are read out from the ROM. The upper four bits of one-byte output of the ROM are assigned to the supply energy data, and the lower four bits thereof to the storage energy data. Therefore, the capacity of the ROM of the calculator 25 3 is 64 K bytes.

The operation of the circuit shown in Fig. 3 will be described with reference to the timing charts in Figs. 4A and 4B. The 8-bit image data is read out from the image memory 20 in response to the signal  $\overline{MR}$  30 and is loaded in the shift register 21 in response to the falling edge of the signal  $\overline{LD}$ . The 8-bit data loaded in the shift register 21 are serially loaded into the shift register 22 in response to the rising edges of the signal  $\overline{SRCLK}$ . When the 8-bit data shift 35 is completed, the signal  $\overline{MR}$  is issued again from the timing controller 12 to load the next 8-bit data into the shift register 21. Thereafter, the above operation

is repeated until data (324 bytes) on one line are shifted.

5       The timing controller 12 generates the signal  $\overline{\text{LATCH}}$  together with the signal  $\overline{\text{SRCLK}}$  so as to shift the storage energy data from the RAMA 23 from the lower latches to the upper latches. The count of the read address counter 32 is incremented by one every time the signal  $\overline{\text{LATCH}}$  is applied to the latches, so that the storage energy data are sequentially read out from the terminal  $\text{D}_{\text{OUT}}$  of the RAMA 23. The storage energy data calculated by the calculator 12 are sequentially stored in the RAMA 23 in response to the signal  $\overline{\text{WR}}$ . The count of the write address counter 31 is incremented every time the data is stored in the RAMA 23.

15       The read address differs from the write address in Fig. 4A or 4B, since the image data of the first resistive element must be shifted to the 3rd bit from the LSB of the shift register 22 and the storage energy data of the first resistive element must be shifted to the latch 26 in order to calculate the supply energy and the storage energy of the first resistive element. The selector 33 is used to switch between the read address signal and the write address signal. When data calculation for one line is completed, all the signals are made off until a read synchronizing signal for the next line is issued. When the synchronizing signal is issued, data readout is performed for the next line. The above operations are repeated until the data processing of all lines is completed.

20       Fig. 5 shows the detailed configuration of the supply energy control 9 of Fig. 1. In this embodiment, since the thermal head has a resolution of 12 dots/mm and an A4 width, the number of thermal heating resistive elements is 2592. In order to shorten the time of data transfer to the thermal head, the thermal head of this embodiment has nine input data ports  $\text{SIN1}$  to  $\text{SIN9}$

each adapted to receive data in a serial manner. Each data port receives data corresponding to 288 resistive elements.

5 The arrangement of the thermal head 10 will be described with reference to Figs. 7 and 8. In this embodiment, thermal heating resistive element drive ICs are used to drive the elements in units of 32 dots. Each port thus requires 9 drive circuits, so that 81 drive circuits 61<sub>1</sub> to 61<sub>81</sub> are arranged in the  
10 thermal head 10. As shown in Fig. 8, each drive circuit comprises a 32-bit shift register 62, a latch circuit 63, an enable gate circuit 64 and, a driver 65 for driving thermal heating resistive elements R1 to R32.

15 Referring back to Fig. 5, the supply energy data 7 calculated by the calculator 3 are applied to the a RAMB(11) 44 to a RAMB(19) 46 or a RAMB(21) 45 to a RAMB(29) 47 through a buffer(11) 40 to buffer(19) 42 or a buffer(21) 41 to buffer(29) 43, respectively. Nine  
20 buffers (i.e., buffer(1) to buffer(9)) and nine RAMBs (i.e., RAMB(1) to RAMB(9)) respectively correspond to nine ports SIN1 to SIN9. If the thermal head has one input port, one set of a buffer and a RAM suffice. Furthermore, two sets each having nine buffers and  
25 nine RAMBs are prepared for a high speed recording. For example, while data are written in the RAMB(11) to RAMB(19), data are read out from the RAMB(21) to RAMB(29). In this manner, the write and read operations can be simultaneously performed. If no high speed  
30 operation is required, a set of nine buffers and nine RAMBs may be used.

Assume that a timing signal  $\overline{G1}$  is issued from the timing controller 12. The timing signal  $\overline{G1}$  and a timing signal  $\overline{G2}$  are applied to terminals CS1 of the  
35 buffer(11) to buffer(19) and of the buffer(21) to buffer(29), respectively. When the timing signal  $\overline{G1}$  is issued, the timing signal  $\overline{G2}$  is not issued and



vice versa. Each buffer is enabled only when a signal of logic "0" is supplied to the terminals CS1 and CS2 thereof so as to supply the supply energy data from the calculator 3 to the corresponding RAMB. Otherwise,  
5 the data line of the supply energy data is disconnected from the corresponding RAMB.

The data is written at an address of RAMBs which is accessed by an address counter 48 or 49 when a signal is applied to its terminal WR. Otherwise, data is read out  
10 from an address accessed by the corresponding address counter. The address counter 48 is commonly used for RAMB(11) to RAMB(19), and the address counter 49 is commonly used for the RAMB(21) to RAMB(29). The same address data are supplied to the RAMB(11) to RAMB(19)  
15 or RAMB(21) to RAMB(29).

The number of address data is equal to the number of resistive elements for one port, so that the number of address data is 288 in the case of nine ports. Since the timing signal  $\overline{G1}$  is issued from the timing  
20 controller 12, the RAMB(21) to RAMB(29) are disconnected from the supply energy data lines. When the supply energy of the first resistive element is calculated, a signal  $\overline{RAMB(11)WR}$  is generated from the timing controller 12. In this case, the buffer(11) 40 is  
25 enabled, so that the supply energy data is coupled to the data line of the RAMB(11).

The supply energy data is written at an address accessed by the address counter 48. Signals  $\overline{RAMB(11)WR}$  to  $\overline{RAMB(19)WR}$  have a period 288 times the period of  
30 the signal  $\overline{WR}$  shown in Figs. 4A and 4B. The data is written in the RAMB(11) in response to the signal  $\overline{RAMB(11)WR}$ . The next signal  $\overline{RAMB(12)WR}$  is used to write the data in the RAMB(12). Similarly, the data is written in the RAMB(19) in response to the last  
35 signal  $\overline{RAMB(19)WR}$ . Each buffer is enabled only when the signal  $\overline{WR}$  is supplied to the corresponding RAMB so as to write the supply energy data in this RAMB.

When the supply energy data of the first resistive element is written in the RAMB(11), the signal  $\overline{WR1}$  is issued from the timing controller 12, and the count of the address counter 48 is incremented by one. The  
5 signal  $\overline{WR1}$  is issued every time one of the RAMB(11) to RAMB(19) receives the signal  $\overline{WR}$ . The supply energy data of the second resistive element is written in the same manner as in the RAMB(11). The above operation is then repeated to write the first 288 supply energy  
10 data in the RAMB(11).

After the supply energy data of the 288th resistive element is written in the RAMB(11), the address counter 48 designates the same address as in the case wherein the supply energy data of the first  
15 resistive element is written. The supply energy data of the 289th resistive element is written in the RAMB(12) in response to the signal  $\overline{RAMB(12)WR}$  generated from the timing controller 12. The data line of the RAMB(11) is disconnected from the supply energy data  
20 line. In the same manner as in the RAMB(11), after the supply energy data of 289th to 577th resistive elements are written in the RAMB(12), the RAMB(12) is disconnected from the supply energy data line. The above operation is repeated to write the supply energy  
25 data of the 2304th to 2592th resistive elements in the RAMB(19). Thus, the calculation for one line is completed.

While the supply energy data for one line are written in the RAMB(11) 44 to RAMB(19) 46, the previous  
30 supply energy data are read out from the RAMB(21) 45 to RAMB(29) 47 and are supplied to the thermal head through a multiplexer(1) 50 to a multiplexer(9) 51, thereby energizing the resistive elements to record image data. At this time, the RAMB(21) to the RAMB(29)  
35 are disconnected from the supply energy data lines, respectively.

Since the signal  $\overline{G1}$  is generated from the timing

controller 12, the signals  $\overline{\text{RAMB}(21)\text{WR}}$  to  $\overline{\text{RAMB}(29)\text{WR}}$  are not issued. In other words, the RAMB(21) to RAMB(29) are kept in the read mode so that the supply energy data accessed by the address counter 49 is read out onto the data line. In response to control signals 51 from the timing controller 12, one bit of the 4-bit data from each of the RAMB(11) to RAMB(19) or of the RAMB(21) to RAMB(29) is selected by the multiplexer(1) 50 to multiplexer(9) 51 and is supplied to the corresponding port. At the present time, the RAMB(21) to RAMB(29) are set in the read mode, so that the selected one-bit data of data read out from the RAMB(21) to RAMB(29) are issued from the multiplexer(1) to multiplexer(9), respectively. The data supplied to the input ports SIN1 to SIN9 of the thermal head 10 are written in the corresponding shift registers in response to the signal  $\overline{\text{CLK}}$  generated from the timing controller 12. At the same time, the timing controller 12 generates the signal  $\overline{\text{CLK2}}$  to increment the address counter 49 of the RAMB(21) to RAMB(29). As a result, supply energy data corresponding to the next resistive elements in the respective groups are read out from the RAMB(21) to RAMB(29). One-bit data of the same order as the previous one-bit data are supplied to the corresponding terminals SIN through the multiplexer(1) to multiplexer(9). This one-bit data is written in the corresponding shift register in response to the signal  $\overline{\text{CLK}}$ . At this time, the immediately preceding one-bit data is shifted by one bit. This operation is repeated by 288 times, so that the same order bits of all the 4-bit data of the RAMB(21) to RAMB(29) are written in all the eighty-one shift registers 62 in the thermal head 10. The data written in the shift registers 62 is latched by the latch circuits 63 in response to a signal  $\overline{\text{ALATCH}}$ . Output data of the latch circuits 63 is supplied to the drivers 65 through the enable gate

circuits 64 which are enabled by one of enable signals MEN-1 to MEN-4 from the timing controller 12. The resistive elements R1 to R32 are heated or are not heated in accordance with the corresponding data "0" or "1". The enable signals MEN-1 to MEN-4 supplied to the gate circuits 64 have different pulsewidths to be described later.

Fig. 6A shows the relationship between the 4-bit supply energy data 7 and the enable signals MEN-1 to MEN-4. In this embodiment, a voltage applied to the resistive elements of the thermal head is constant, so that a current flowing therethrough is also constant. In order to change the supply energy of the resistive elements, the energizing time must change in accordance with the supply energy. The 4-bit supply energy data generated from the calculator represents an energizing time of a resistive element. However, the energizing time cannot vary in units of resistive elements because of the structural restriction of the thermal head. In practice, the energizing times of the resistive elements have the same length of period. In order to vary the energizing times of the resistive elements, the energization of each resistive element may be repeated several times in accordance with the corresponding supply energy data.

In this embodiment, as shown in Fig. 6, four energizing times T1 to T4 are set in accordance with the four enable signals MEN-1 to MEN-4. The four energizing times and the four bits of the supply energy data have a one-to-one correspondence. For example, the MSB  $E_i^{n1}$  corresponds to energizing time T1;  $E_i^{n2}$ , to T2;  $E_i^{n3}$ , to T3; and  $E_i^{n4}$ , to T4. The energizing time of each resistive element is selected by a bit or bits of "1" of the supply energy data. For example, if  $E_i^{n1} = E_i^{n3} = E_i^{n4} = 1$  and  $E_i^{n2} = 0$ , the energizing times T1, T3 and T4 are selected as shown in Fig. 6B. The corresponding resistive element is energized during

a time of  $T_1 + T_3 + T_4$ . In this embodiment, the energizing time of each resistive element is changed in such a manner as described above.

Furthermore, according to this embodiment, the  
5 times  $T_1$ ,  $T_2$ ,  $T_3$  and  $T_4$  can be freely set in accordance with the enable signals MEN-1 to MEN-4. When  $T_1 = T_2 = T_3 = T_4$ , a maximum of four steps of the energizing time intervals can be obtained. When the pulsewidths of the enable signals MEN-1 to MEN-4  
10 (corresponding to the times  $T_1$  to  $T_4$ ) differ from each other, a maximum of 16 steps of the energizing time intervals can be obtained. Furthermore, if the number of bits of the supply energy data is increased, or the supply order of enable pulses having different  
15 pulsewidths is changed, then the more precise control of the energizing time would be enabled.

The operation of the thermal recording system will be repeated.

The multiplexer(1) to multiplexer(9) select, for  
20 example, the MSB  $E_i^{n1}$  of the 4-bit supply energy data read out from the RAMB(21) to RAMB(29) to feed the thermal head 10. As previously described, when the readout of one-bit data is performed 288 times, all the MSB data  $E_i^{n1}$  of the supply energy for all the  
25 resistive elements are written in the shift registers of the thermal head 10. The MSB data are latched by the latch circuits in response to the signal  $\overline{\text{ALATCH}}$  generated from the timing controller 12. Next, the latched data are supplied to the drivers through the  
30 gate circuits in response to the enable signal MEN-1 for setting the energizing time  $T_1$ . As a result, a current is supplied to the resistive elements corresponding to data of "1" for the energizing time  $T_1$ .

35 When the MSB data  $E_i^{n1}$  are latched by the latch circuits, data readout from the RAMB(21) to RAMB(29) is restarted from address 1. At this time, the

5 multiplexer(1) to multiplexer(9) select the bit  $E_i^{n2}$  (next to the MSB) of the 4-bit supply energy data read out from each of the RAMB(21) to RAMB(29). In the same manner as in the MSB data, the resistive elements are selectively energized in accordance with the data  $E_i^{n2}$  of the 4-bit supply energy data for the time T2 set by the enable signal MEN-2.

10 Data readout from the RAMB(21) to RAMB(29) is restarted from address 1 thereof. In this case, the multiplexer(1) to multiplexer(9) select the one-bit data  $E_i^{n3}$ . The timing controller 12 generates the enable signal MEN-3, so that the resistive elements are selectively energized for the time T3 set by the enable signal MEN-3. Finally, the fourth time data readout operation is performed with respect to the RAMB(21) to RAMB(29). The multiplexer(1) to multiplexer(9) select the LSB data  $E_i^{n4}$  of the 4-bit supply energy data. The timing controller 12 supplies the enable signal MEN-4 to the enable gate circuit 64.

20 As a result, the resistive elements are selectively energized for the time T4 set by the enable signal MEN-4. In this manner, the four-time data readout operations from the RAMBs and the four-time selective energizations of the resistive elements in accordance with the readout data are performed to print the image data corresponding to one line.

The supply energy must be preset to cause the resistive element to reach a predetermined temperature, since the transfer factor of ink to a sheet depends solely on the temperature of the resistive element, as has been found according to experiments.

The features of the present invention described above will be summarized as follows:

35 (1) The storage energies are determined in accordance with input image data to be recorded and the storage energies resulting from the recording operation of the previous image data;

(2) The supply energy is determined in accordance with this storage energy and the input image data; and

(3) Time and space factors are considered with respect to the thermal conduction.

5       The present invention is not limited to the particular embodiment. Various changes and modifications may be made within the spirit and scope of the present invention. For example, the content of the ROM of the calculator 3 may be obtained theoretically  
10       or empirically. Alternatively, the calculator 3 may be comprised of a CPU or the like.

## Claims:

1. A thermal recording system comprising:
  - a thermal head (10) having a number of thermal heating resistive elements ( $R_1$  to  $R_{32}$ ) and drive circuit means (62 to 65) for selectively energizing said thermal heating resistive elements, with current supply, in accordance with image data to record the image data;
  - memory means for storing data of a storage energy of each of said thermal heating resistive elements after the image data have been recorded;
  - calculating means (3) responsive to storage energy data from said memory means and next image data for calculating a supply energy to be supplied to each of said resistive elements to record the next image data and a storage energy stored in each of said thermal heating resistive elements after the next image data have been recorded; and
  - controlling means (9, 12 ) responsive to the supply energy data of each of said resistive elements from said calculating means for causing said drive circuit means to control the supply energy to be applied to each of said thermal heating resistive elements.
2. A system according to claim 1, characterized in that the storage energy data calculated by said calculating means (3) is stored in said memory means (5), whereby the storage energy data stored in said memory means is updated every time new image data is recorded.
3. A system according to claim 1, characterized in that said calculating means (3) is arranged to calculate the supply energy to an  $i$ th thermal heating resistive element in accordance with image data for said  $i$ th resistive element and adjacent resistive elements arranged on the right and left sides of said  $i$ th thermal heating resistive element, and the storage energy data of said  $i$ th and adjacent resistive elements which are



stored in said memory means.

4. A system according to claim 3, characterized in that said calculating means (3) is connected to receive the storage energy data of said ith thermal heating resistive element and an average value of the storage energy data of at least a pair of corresponding resistive elements arranged on the right and left sides of said ith resistive element.

5. A system according to claim 3, characterized in that said calculating means (3) comprises a read only memory arranged to receive, as address data, the image data and the storage energy data of said thermal heating resistive elements ( $R_1$  to  $R_{32}$ ), and store the supply energy data and the storage energy data for one thermal heating resistive element at an address specified by the address data.

6. A system according to claim 1, characterized in that each of the supply energy data has a plurality of bits, and said control means (9, 12) is arranged to supply the supply energy data of each of said thermal heating resistive elements to said drive circuit means in units of corresponding bits, so that the image data for each of said resistive elements is recorded in a time division manner, the number of time divisions corresponding to the number of bits.

7. A system according to claim 6, characterized in that said drive circuit means comprises: shift register means (62) connected to receive the supply energy data of said thermal heating resistive elements in units of corresponding bits; latch circuit means (63) for latching a plurality of bit outputs of said shift register means; and enable gate circuit means (64) coupled between said bit outputs of said latch circuit means and said thermal heating resistive elements ( $R_1$  to  $R_{32}$ ), said enable gate circuit means (64) being enabled each time corresponding bits of the supply energy data of said resistive elements are recorded.

8. A system according to claim 7, characterized in that enabling times of said enable gate circuit means (64) vary with bits of the supply energy data.

5 9. A system according to claim 1, characterized in that the supply energy data has a plurality of bits; and said control means (9, 12) comprises

temporary memory means (RAMB) for temporarily storing the supply energy data of said thermal heating resistive elements ( $R_1$  to  $R_{32}$ ) which are generated from  
10 said calculating means (3),

multiplexer means (MPX) for sequentially supplying to said drive circuit means corresponding bits of the supply energy data which are sequentially read out from said temporary memory means, and

15 means for causing said temporary memory means (RAMB) to read out the supply energy data for the number of times corresponding to the number of the bits of the supply energy data and for causing said multiplexer means (MPX) to supply the supply energy data to said  
20 drive circuit means in units of corresponding bits, thereby recording the image data in a time division manner for each bit of the supply energy data.

10. A system according to claim 1, characterized in that

25 said thermal heating resistive elements ( $R_1$  to  $R_{32}$ ) of said thermal head (10) are divided into a plurality of groups,

said drive circuit means (62 to 65) is divided into sub-drive circuit means corresponding to said plurality  
30 of groups, and

said control means (9, 12) comprises a plurality of memory means (RAMB(11) to RAMB(19)) for temporarily storing the supply energy data supplied from said calculating means (3) in units of groups, and means (48,  
35 49) for reading out the supply energy data from said plurality of memory means to supply readout data to corresponding sub-drive circuit means of said drive

circuit means in a parallel manner.

11. A method of recording image data using a thermal head having a number of thermal heating resistive elements aligned in line and drive circuit  
5 means for selectively energizing said thermal heating resistive elements, with current supply, in accordance with the image data to record the image data of one line, comprising of the steps of:

providing, as data having a plurality of bits,  
10 supply energy to be supplied to each of said thermal heating resistive elements to record the image data of one line in accordance with the image data of one line to be recorded and storage energy stored in each thermal heating resistive element after image data of  
15 an immediately preceding line has been recorded;

supplying to drive circuit means the supply energy data for said thermal heating resistive elements in units of corresponding bits; and

energizing said thermal heating resistive elements  
20 every time corresponding bits of the supply energy data is supplied to said drive circuit means.

12. A method according to claim 11, characterized in that energizing times of said thermal heating resistive elements vary with bits of the supply energy  
25 data.

FIG. 1

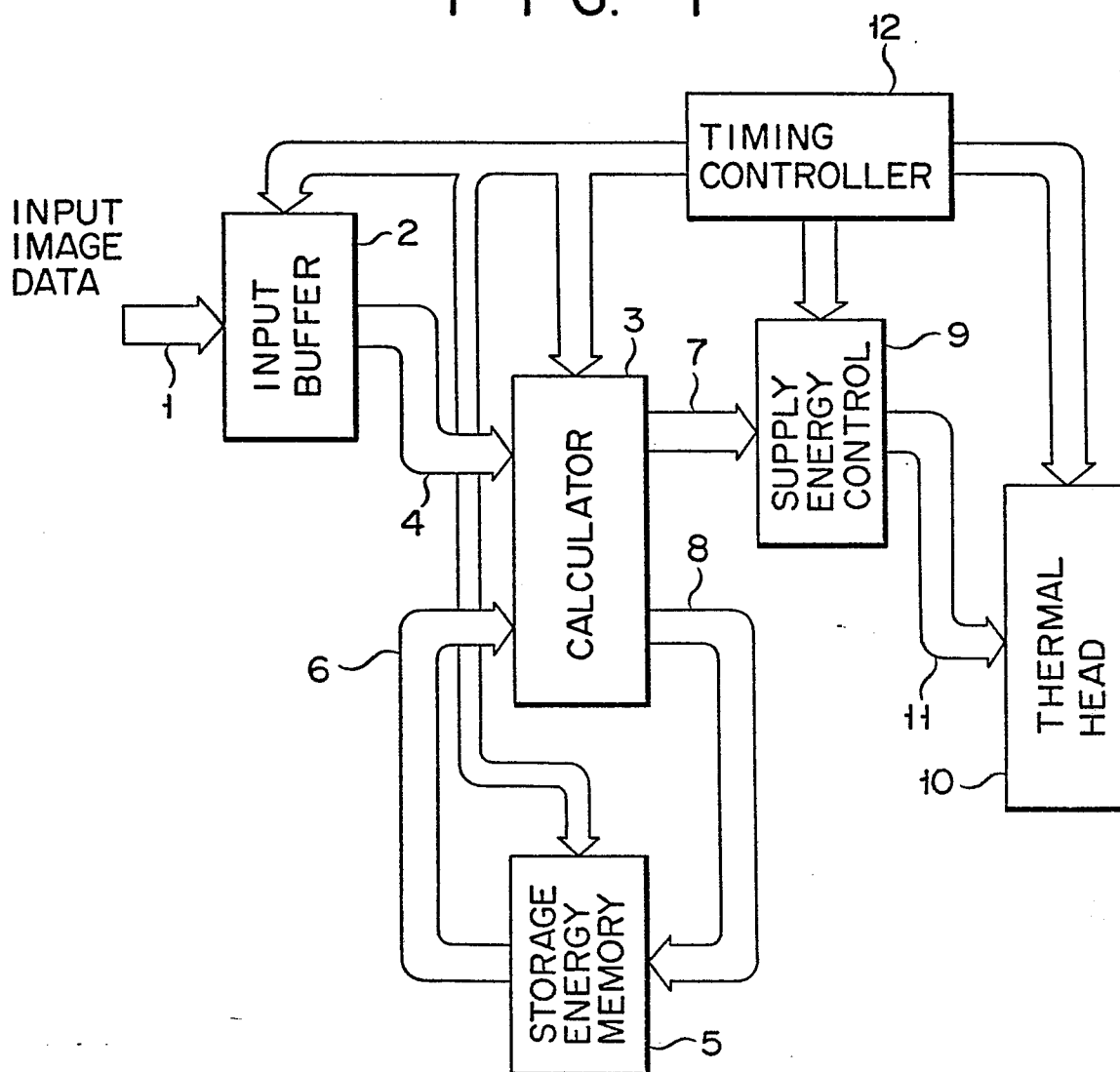


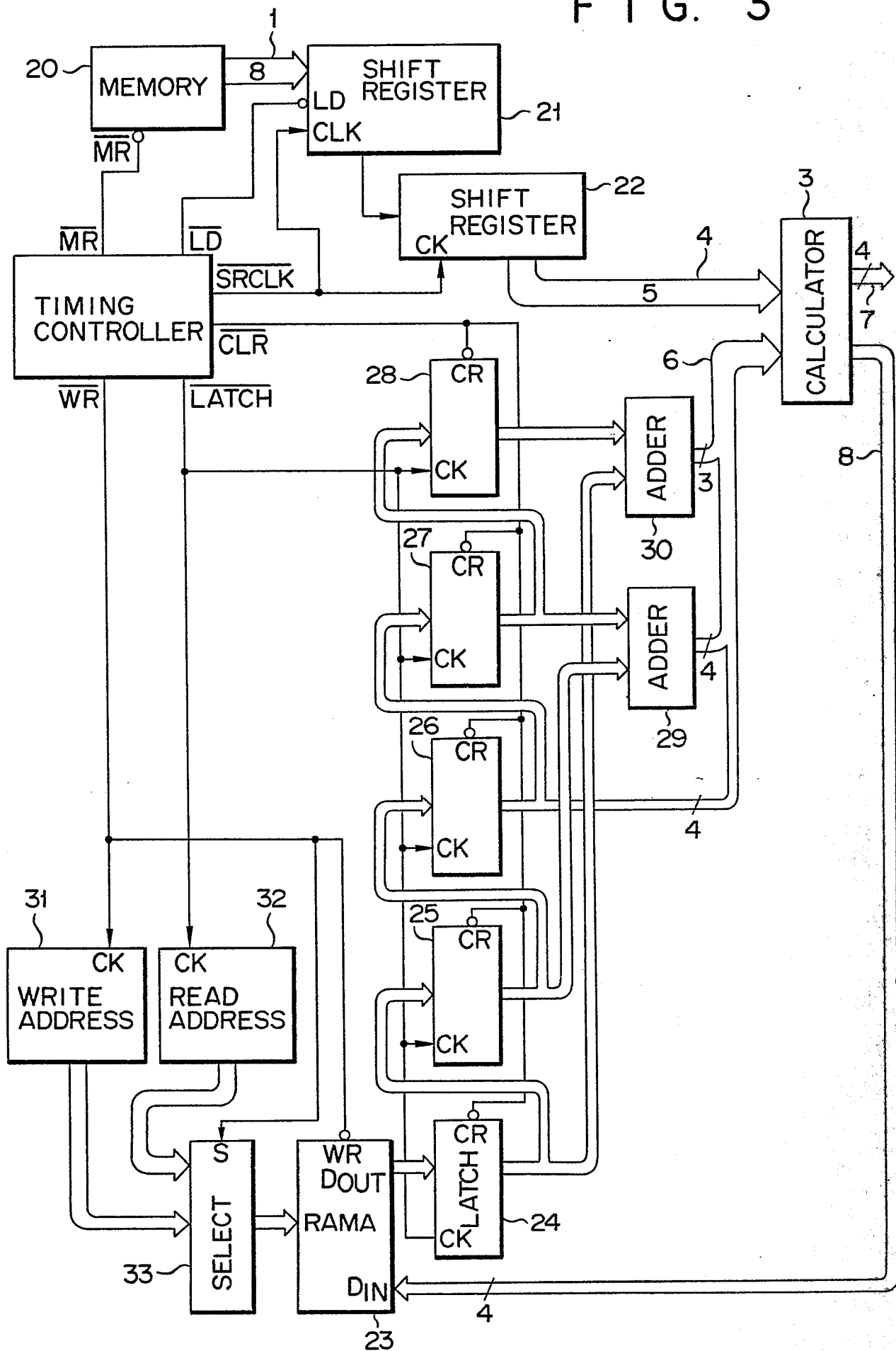
FIG. 2

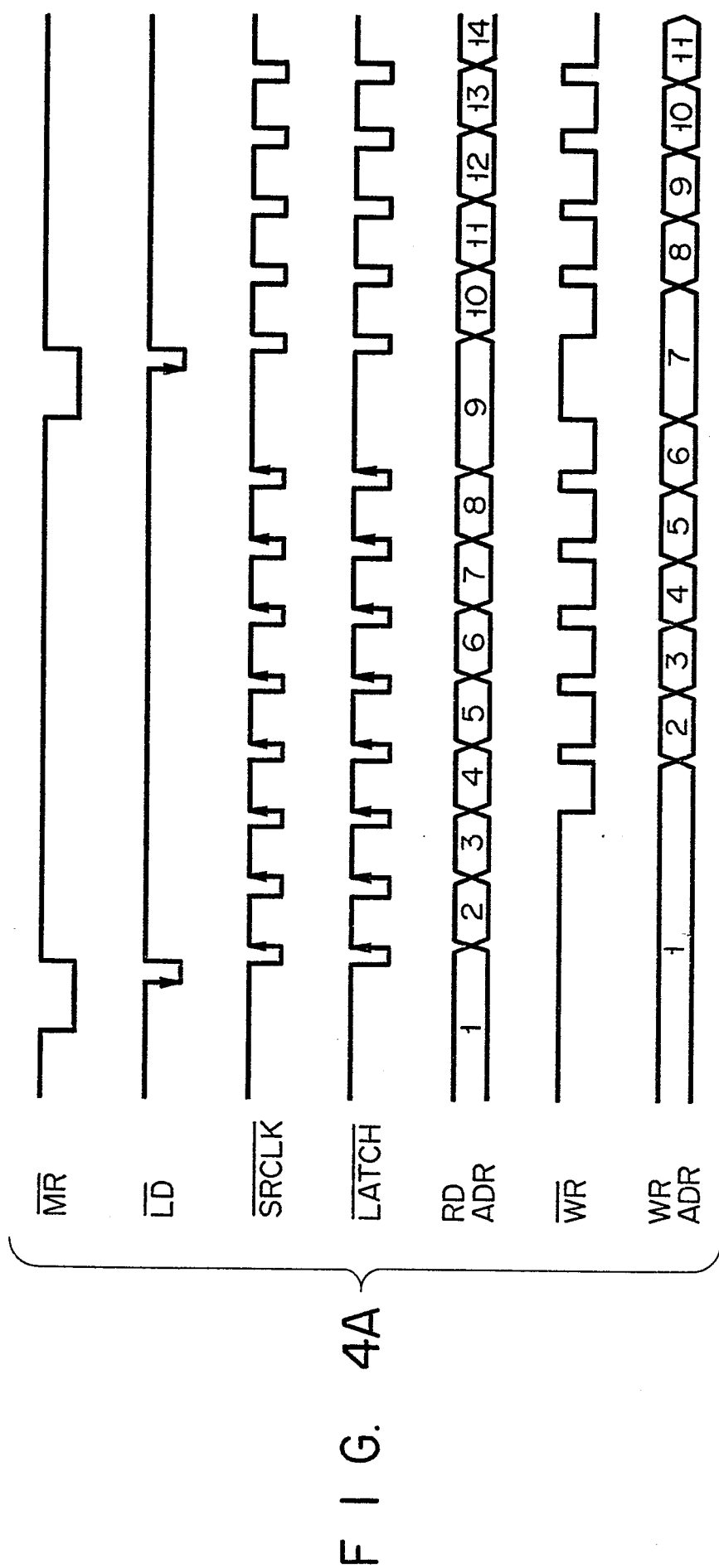
$i-2$	$i-1$	$i$	$i+1$	$i+2$
$Q_{i-2}$	$Q_{i-1}$	$Q_i$	$Q_{i+1}$	$Q_{i+2}$
$D_{i-2}$	$D_{i-1}$	$D_i$	$D_{i+1}$	$D_{i+2}$

2/7

0110675

FIG. 3





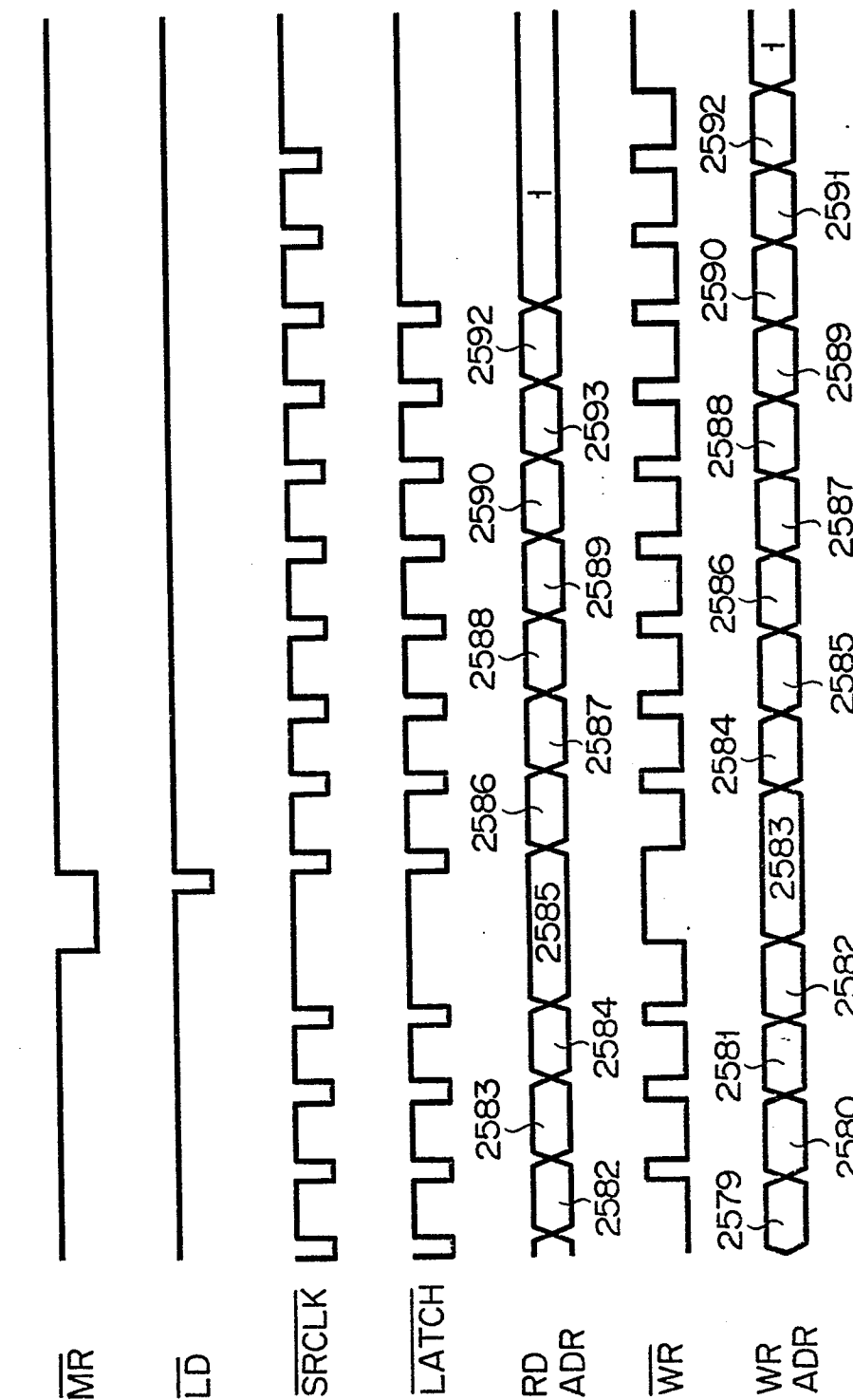


FIG. 4B

5/7

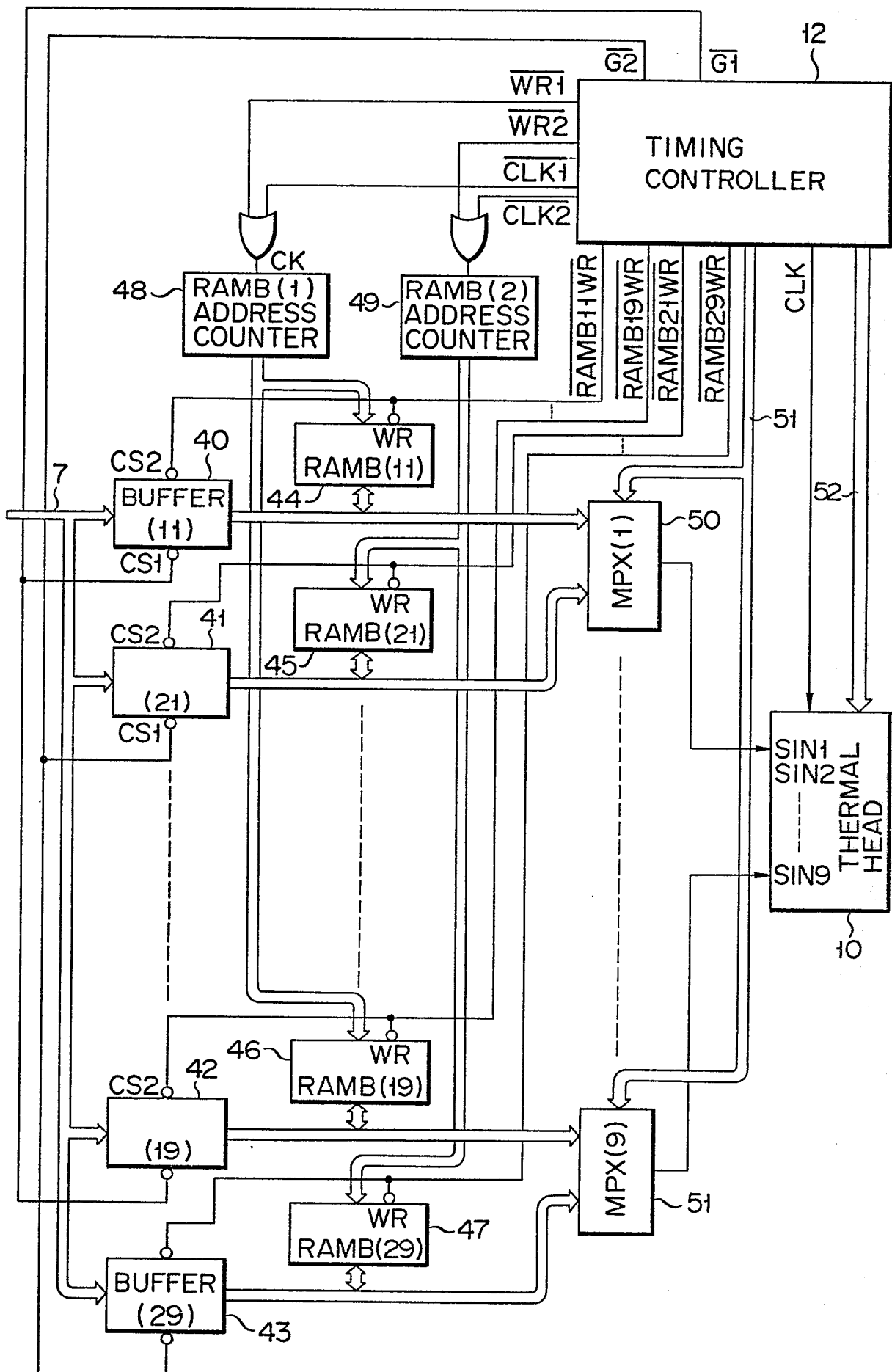
0110675  
FIG. 5



FIG. 6A

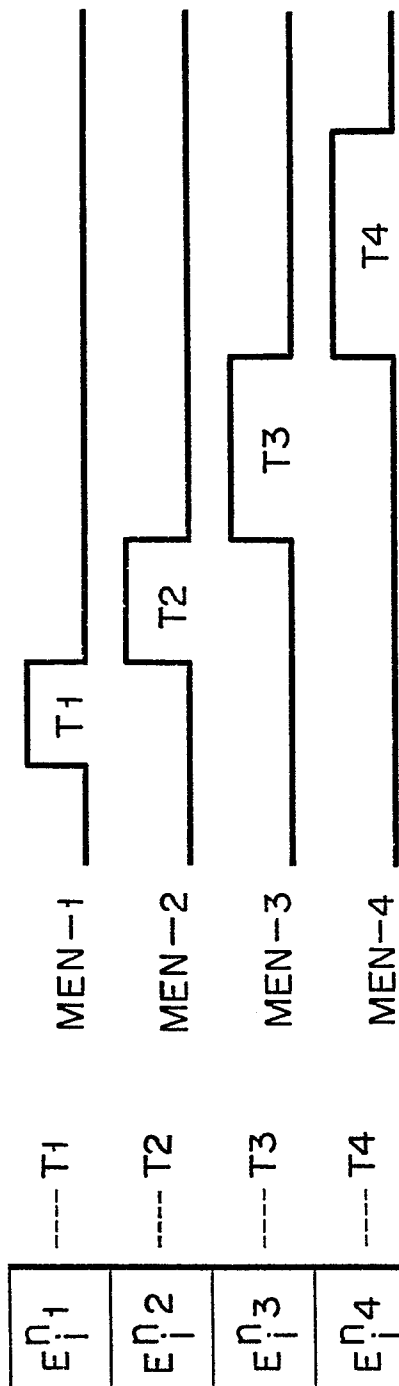


FIG. 6B



7/2

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FIG. 7

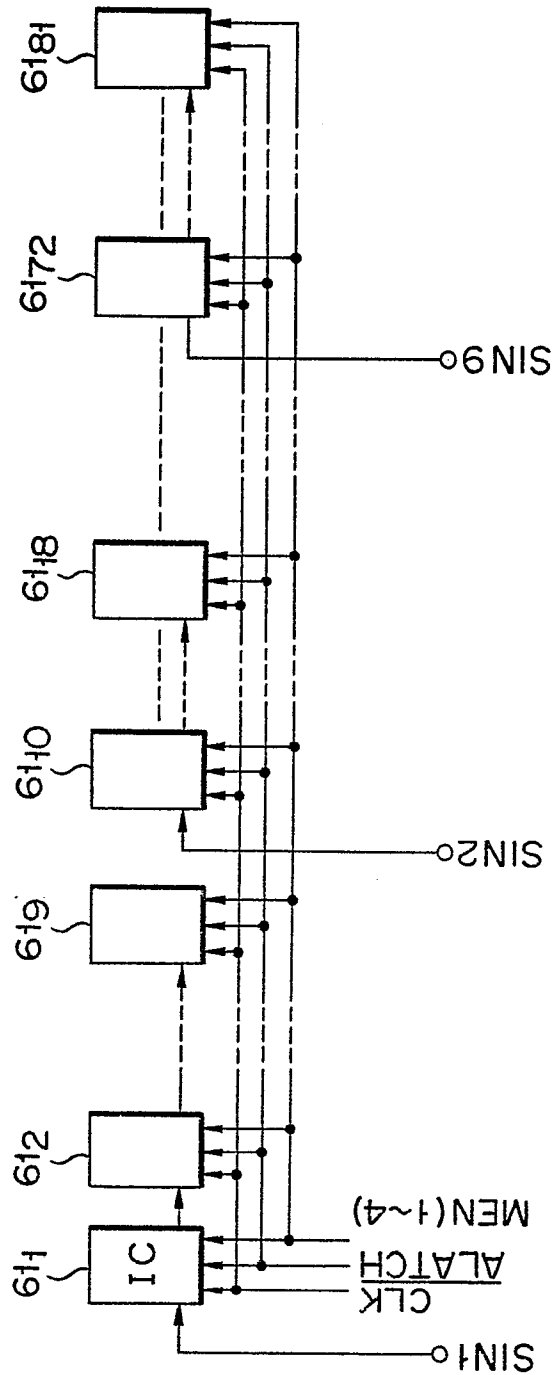


FIG. 8

