(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 113 935**
A2

(12) # EUROPEAN PATENT APPLICATION

(21) Application number: **83201794.1**

(22) Date of filing: **15.12.83**

(51) Int. Cl.³: **G 04 F 10/04**

(30) Priority: **22.12.82 GB 8236371**

(43) Date of publication of application: **25.07.84**
Bulletin 84/30

(84) Designated Contracting States: **DE FR GB IT NL SE**

(71) Applicant: **PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, Arundel Great Court 8 Arundel Street, London WC2R 3DT (GB)**
(84) Designated Contracting States: **GB**

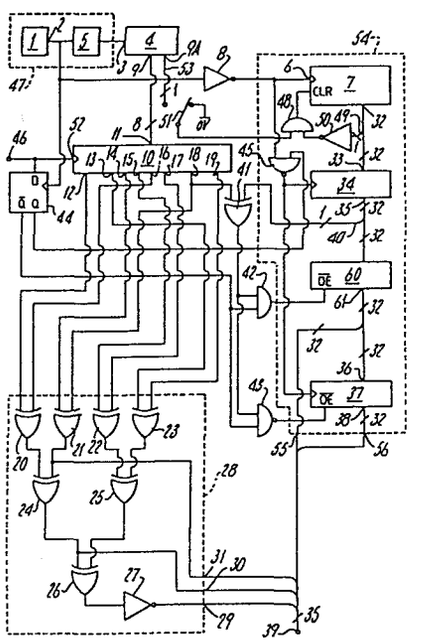
(71) Applicant: **N.V. Philips' Gloeilampenfabrieken, Groenewoudseweg 1, NL-5621 BA Eindhoven (NL)**
(84) Designated Contracting States: **DE FR IT NL SE**

(72) Inventor: **Dadds, Alan Frederick, C/O PHILIPS RESEARCH LABORATORIES, Redhill Surrey RH1 5HA (GB)**

(74) Representative: **Osborne, David Ernest et al, Philips Electronic and Associated Industries Limited Patent Department Mullard House Torrington Place, London WC1E 7HD (GB)**

(54) **Timer circuit.**

(57) In order to obtain a high time resolution a timer circuit comprises a clock pulse generator arrangement (47) an output of which feeds the input (3) of a delay line (4) which is provided with n taps (9) the positions of which correspond to substantially equal increments T of delay. The mark-to-space ratio of the pulses fed to the delay line is unity and their period such that exactly one can be accommodated in the delay line. The taps are connected to a latch (10) which is clocked from an input (46) when an event occurs the time of occurrence of which it is required to record. The Johnson code appearing at the latch output (12–19) is converted to binary by means of a decoder (28) and fed to an output (39). The arrangement also includes a coarse counter (7) the least significant bit of which has the same significance as, and is nominally synchronised with, the most significant bit of the binary code. In order to resolve ambiguities which might otherwise occur when the event occurs near to an all-1s to 0s transition of the binary code the current count and the previous count of the coarse counter are held in a pair of registers (34, 37). Which of these counts is appropriate at any given time is determined by comparing the same-significance bits of the coarse and fine counts in an exclusive-or gate (41) the output of which gates the output (35 or 38) of the appropriate register to the circuit output (39).



EP 0 113 935 A2

"TIMER CIRCUIT"

This invention relates to a timer circuit including a clock pulse generator arrangement, a delay device to which an output of the clock pulse generator arrangement is coupled and which is provided with n taps the positions of which correspond to substantially equal increments T of delay where nT is greater than both the length of the output pulses of the clock pulse generator arrangement applied thereto in operation and the length of the intervals therebetween, and a coupling from said taps to an output of the circuit.

A known such timer circuit is disclosed in U.S. patent specification 2,831,162. The presence of the delay device enables the time elapse between two events to be determined with a resolution which is less than the period of the output signal of the clock pulse generator arrangement. To this end, in the known circuit each tap is coupled to the clock input of a respective counter via a respective gate, the data outputs of the counters constituting the output of the circuit. Because in the known circuit nT is equal to the period of the output pulses of the clock pulse generator arrangement, when the gates are transmissive the counters are clocked in succession during each clock pulse period, with the result that each such clock pulse period is effectively divided into n parts. The counters are started from zero by unblocking the gates when the first of two events the time elapse between which it is required to determine occurs, and their current counts are held therein by blocking the gates when the second event occurs. The average of the held counts is then determined to give the magnitude of the time elapse with a resolution of 1/n times the clock pulse period.

A disadvantage with the known circuit is that it tends to be rather complex, particularly if the desired resolution requires the provision of a large number of taps (e.g. $\geq$ 8) together with their associated counters. Moreover the calculation of the average tends to take a significant amount of time.

It is an object of the invention to mitigate these disadvantages.

The invention provides a timer circuit including a clock pulse generator arrangement, a delay device to which an output of the clock pulse generator arrangement is coupled and which is provided with n taps the positions of which correspond to substantially equal increments T of delay where nT is greater than both the length of the output pulses of the clock pulse generator arrangement applied thereto in operation and the length of the intervals therebetween, and a coupling from said taps to an output of the circuit, characterized in that said coupling includes a latch circuit to respective data bit inputs of which said taps are coupled in such manner that when data presented to said data bit inputs from said taps is latched in said latch circuit the latched data will be the actual binary code currently present on said taps. (One of the taps may be constituted by the input of the delay device and/or one of the taps may be constituted by the output of the delay device if desired. Moreover, the delay device may be a composite one, i.e. be made up from a plurality of delay devices in cascade, if desired. It will be evident furthermore that the latched code may be in inverted or non-inverted form).

It has now been recognized that the successive parallel codes appearing on the taps of a tapped delay line fed from a clock pulse generator arrangement are themselves indicative of successive time instants and may therefore be used directly to indicate the passage of successive periods of time. It can be arranged, for example, that each code is present for a time T and is replaced by a new one at the end of that time. (One requirement for this is that the length of each clock pulse, and the length of each interval between two successive clock pulses, is less than nT, because otherwise the duration of some codes would be an integral number of times T). Moreover, if the length of each clock pulse and the length of each interval between two successive clock pulses are suitably chosen relative to the incremental delay T the resolution obtainable with a given number of taps and a given clock pulse period can be increased, and can even be doubled,

relative to that obtainable with the known circuit. (This is because the signal on each tap responds to the passage of both the leading and the trailing edge of each clock pulse past the relevant tap, whereas in the known arrangement each counter responds to the passage of only the leading edge past the relevant tap).

In order to make optimum use of the n taps in respect of the number of successive parallel codes which are generated thereon before the sequence repeats, preferably the mark-to-space ratio of said output pulses is substantially unity and the period of said output pulses is greater than or equal to 2(n-1)T. If this is the case 2n different codes will be generated in every two periods of the output of the clock pulse generator arrangement, after which the sequence will repeat. The 2n equal time intervals T in the said two periods will each be indicated by a respective so-called Johnson code at the taps, i.e. a code in which only one bit changes from each period T to the next.

If n is an integral power of 2 a decoder may be included in a coupling from the output of the latch circuit to the timer circuit output, which decoder is constructed to convert the successive n-bit codes appearing on said taps in operation to successive members of an m-bit binary code should said successive n-bit codes be supplied thereto. The presence of such a decoder can make the timer output more suitable for processing by conventional binary circuitry.

Obviously if ambiguities are not to occur the circuit as set forth so far cannot be used to measure the time between two events which are separated by more than 2 nT. Rather than merely increase the length of the delay device (and the number of taps correspondingly) when it is required to measure longer times, which lengthening may result in the delay device becoming unwieldly, the circuit may include a synchronous counter arrangement to the input of which an output of said clock pulse generator arrangement is coupled and the output of which is coupled to the

timer circuit output via a latch circuit. Such a counter arrangement can operate within the frequency capabilities of conventional circuitry and be used to produce a "coarse" count, the "fine" count being derived from the taps on the delay device.

If such a counter arrangement is present and if moreover the aforesaid decoder is also provided, the counter arrangement may be a binary counter arrangement and may be used to produce the most significant bits of the circuit output, the decoder producing the least significant bits thereof. However, even if the clock signal is derived from a tap or taps on the delay device rather than directly from the clock pulse generator arrangement, ambiguities would, unless further steps were taken, be liable to occur when the latches are activated near to an instant when the decoder output changes from all-1s to all-0s, due to the effects of differential delays. In order to resolve such ambiguities preferably, when the mark-to-space ratio of the output pulses of the generator arrangement is substantially unity and the period of said output pulses is greater than or equal to $2(n-1)T$, said binary counter arrangement is constructed to produce its current count at a first output thereof and its immediately preceding count at a second output thereof, the coupling from an output of said clock pulse generator arrangement to said counter arrangement circumventing said delay device and being such, relative to the coupling from the clock pulse generator arrangement to the delay device, that the clock pulses applied to said counter arrangement in operation will have twice the repetition rate of those applied to the delay device, resulting in the least significant bit of the outputs of said counter arrangement having the same significance as has the most significant bit of said m-bit binary code, said coupling and said counter arrangement moreover being such that the counts at said first and second outputs will be updated at instants which are offset with respect to each change in said n-bit code which corresponds to a change in the most significant bit of said m-bit binary code, comparison means being provided for comparing the value of the most significant bit of said m-bit binary code

with the value of the least significant bit of the count at a said output and gating the count at one of said first and second outputs to the timer circuit output if the two compared bits have the same value and gating the count at the other of said first and second outputs to the timer circuit output if the two compared bits have opposite values. Because in such a circuit the most significant bit of the decoder output and the least significant bits of the two counter arrangement outputs have the same significance, comparison of said most significant bit with one of said least significant bits when the latches have been activated can determine whether the count at the said first output or the count at the said second output was the one which was actually the correct one at the time the latches were activated. If said counter arrangement and the coupling thereto from the generator arrangement are such that the counts at said first and second outputs will be updated at instants which nominally lie substantially midway between each change in said n-bit code which corresponds to a change in said most significant bit the maximum amount of the aforesaid differential delays can be accommodated.

An embodiment of the invention will be described, by way of example, with reference to the accompanying diagrammatic drawing the single Figure of which is a schematic diagram thereof.

In the drawing a timer circuit comprises a clock pulse generator arrangement 47 which includes a generator 1 which generates clock pulses at its output 2 with a mark-to-space ratio of substantially unity. The output 2 is coupled to the input 3 of a delay device 4 via a negative-edge responsive frequency divider-by-two 5 also included in the arrangement 47, and also to the input 6 of a 32-bit counter 7 via an inverter 8. The delay device is provided with n=8 equally-spaced taps which are signified collectively by a (multiple) output 9 and which are coupled to data inputs of respective stages of an 8-bit storage register or latch 10 which is "transparent" when its clock input 52 is high, these data inputs being signified collectively by a (multiple) input 11. The stages of the register 10 have outputs 12, 13, 14, 15, 16, 17, 18 and 19 respectively, these corresponding, in order, to respective

ones of the successive taps positioned along the delay device 4 from the input 3 thereof. The outputs 12 and 16 are connected to respective inputs of an EXCLUSIVE-OR gate 20, the outputs 14 and 18 are connected to respective inputs of an EXCLUSIVE-OR gate 21, the outputs 15 and 17 are connected to respective inputs of an EXCLUSIVE-OR gate 22, and the outputs 13 and 19 are connected to respective inputs of an EXCLUSIVE-OR gate 23. The outputs of the gates 20 and 21 are connected to respective inputs of an EXCLUSIVE-OR gate 24 and the outputs of the gates 22 and 23 are connected to respective inputs of an EXCLUSIVE-OR gate 25. The outputs of the gates 24 and 25 are connected to respective inputs of an EXCLUSIVE-OR gate 26. The gates 20-26 together with their interconnections and an inverter 27 form a Johnson code to binary code converter or decoder 28 which converts the successive 8-bit codes appearing in operation at the outputs 12-19 of register 10 when its clock input 52 is high into successive members of an m=4-bit binary code which appears in parallel at outputs 29-31 of converter 28 and output 18 of register 10. The outputs 29-31 are fed from the output of gate 26 via inverter 27, from the output of gate 24 and from the output of gate 21 respectively, bits of increasing significance occurring at the outputs 29, 30, 31 and 18 respectively.

The 32-bit output 32 of counter 7 is connected to the 32-bit data input 33 of a first 32-bit storage register or latch 34 the 32-bit data output 35 of which is connected to the 32-bit data input 36 of a second 32-bit storage register or latch 37 via a 3-state buffer 60. The 32-bit data output 38 of register 37 is connected to the thirty-two most significant bit lines of a 35-bit output 39 of the timer circuit, as is the data output 61 of buffer 60. The three least significant bit lines of the output 39 are fed from respective ones of the outputs 29-31 of decoder 28.

The least significant bit line 40 of the output 35 of register 34 is also connected to one input of an EXCLUSIVE-OR gate 41 the other input of which is fed from the output 18 of register 10. The output of gate 41 is connected to one input of

each of an AND gate 42 and a NAND gate 43 the other inputs of which are both fed from the $\overline{Q}$-output of a D-type flip-flop 44. The outputs of the gates 42 and 43 are fed to the (active-low) output-enable inputs $\overline{OE}$ of buffer 60 and register 37 respectively.

The clock inputs of the registers 34 and 37 are fed from the output of inverter 8 via a NAND gate 45 the other input of which is fed from the Q-output of flip-flop 44. Components 7, 34, 37, 60 and 45 thus constitute a synchronous counter arrangement 54 having two outputs 55 and 56 for the counts in registers 34 and 37 respectively. The clock input of flip-flop 44 is fed from the output 2 of generator 1 and its data input D is fed from a stop-pulse input 46, as is the clock or hold input of register or latch 10.

The delay produced by the device 4 between each of its taps and the next is T so that the overall delay between the first tap and the last is $(n-1)T = 7T$. The length of the pulses appearing at the output of divider 5 in operation is less than $nT=8T$, as is therefore the intervals therebetween (their mark-to-space ratio is unity). Moreover the period of these pulses is greater than or equal to $2(n-1)T = 14T$. In other words the length of each pulse, and of each interval between two successive pulses, is at least equal to 7T but is less than 8T. Thus when one of these pulses, and subsequently the interval following it, appears at the output of divider 5, the sixteen 8-bit codes in the left-hand column of the following Table appear in succession at equal intervals on the taps on the device 4.

TABLE

00000000	1000
10000000	0100
11000000	1100
11100000	0010
11110000	1010
11111000	0110
11111100	1110
11111110	0001

11111111	1001
01111111	0101
00111111	1101
00011111	0011
00001111	1011
00000111	0111
00000011	1111
00000001	0000

Thus each period of the output of divider 5 is effectively divided into sixteen equal intervals, each of which is signified by its particular (Johnson) code on the taps of delay device 4. When the clock input 52 of latch 10 is high, i.e. when latch 10 is transparent, these codes are converted into the respective codes shown in the right-hand column of the Table on the points 29, 30, 31, 18.

Because divider 5 is negative-edge-responsive, and counter 7 is positive-edge-responsive, counter 7 is clocked at the beginning and end of each output pulse of divider 5. Registers 34 and 37 are positive-edge-responsive at their clock inputs so that, assuming flip-flop 44 is in the set state and hence that (inverting) gate 45 is enabled, registers 34 and 37 are clocked midway through each output pulse of divider 5 and mid-way through each interval between two successive output pulses, register 34 taking in the current count of counter 7, and register 37 taking in the current contents of register 34 (which correspond to the previous count in counter 7). Thus the least significant bit in the counter 7 and the registers 34 and 37 changes at the same rate as the bit at the output 18 of register 10 when register 10 is transparent (this bit being the right-hand bit in the right-hand column of the Table). In other words these least significant bits have the same significance as the bit at output 18. Moreover the least significant bit in the counter 7 changes at instants which nominally coincide with each change in the 8-bit code at output 9 of delay device 4 which gives rise to a change in the bit at output 18 when register 10 is transparent. (It will be evident from the above Table that the

connections from the decoder 28 and the gate 41 to the outputs 12-19 of register 10 are chosen in such manner that the most significant bit in the right-hand column changes when the code in the left-hand column changes from 11111100 to 11111110 and from 00000011 to 00000001, rather than from 11111110 to 11111111 and from 00000001 to 00000000 as might be expected. This is done in order to compensate for the fact that delay device 4 produces a delay T between its input 3 and the first tap (the tap corresponding to output 12 of latch 10) and ensures that changes in the said most significant bit nominally coincide with the beginnings and ends of the output pulses of divider 5 and hence with the instants at which counter 7 is clocked).

The circuit also includes an AND gate 48 the output of which is connected to the "synchronous clear" input CLR of the counter 7 and the inputs of which are fed with the inverted least significant bit of the output of counter 7 by means of a line 49 and an inverter 50 and, when a changeover switch 51 is in the position other than that shown, with the signal on a further tap 9A on delay device 4 by means of a line 53 respectively. When the switch 50 is in the position shown, on the other hand, gate 48 is disabled, its left-hand input then being fed with zero voltage (logic 0). Items 48-51 are provided to enable the least significant bit in counter 7 to be given the same value as the bit appearing on output 18 of register 10 when register 10 is transparent (which bits are, as previously explained, nominally synchronized one with the other). To this end switch 51 is momentarily switched to its other position when the circuit is initially energised. The tap to which line 53 is connected is chosen so that the signal appearing thereon when counter 7 is clocked corresponds to the present value of the least significant bit in counter 7 if counter 7 is operating in the phase required to give the above-mentioned correspondence between the least significant bit in counter 7 and the bit appearing on output 18 when latch 10 is transparent. Thus, if counter 7 is not working in this phase AND gate 48 produces an output when the least significant bit in counter 7 would otherwise next change

from "0" to "1", thus clearing counter 7 so that the least significant bit in register 34 remains at "0" and only changes when counter 7 is again clocked. After this has occurred switch 51 is returned to the position shown. In a practical embodiment in which the delay device 4 was provided with more than the eight taps making up the output 9 tap 9A was in fact the tenth from the input 3. (Obviously an equivalent result can be obtained using the second tap from the input 3, provided that an inverter is then included in the line 53).

After the above synchronization operation has been carried out by means of the switch 51 the circuit operates as follows. Events the intervals between which are required to be timed are arranged to give rise to a high-to-low transition on input 46, which is normally high (logic "1"). When such a transition occurs the 8-bit code currently at the output 9 of delay device 4 is immediately held in register 10 and, moreover, when the next clock pulse appears at the output 2 of generator 1 registers 34 and 37 are clocked once again and flip-flop 44 is reset. This resetting of flip-flop 44 results in the enabling of the gates 42 and 43 and the disabling of gate 45, this last preventing further clocking of registers 34 and 37 (although counter 7 continues to be clocked). The least significant bit in register 34 is compared in gate 41 with the bit at output 18 of register 10. If these two bits are identical (which means, assuming registers 34 and 37 are clocked at exactly one quarter of the way through and three-quarters of the way through each sixteen-count sequence at outputs 29,30,31,18, that the count at outputs 29,30,31,18 lies in the range 0-3 or 8-11, i.e. the most significant bit thereof had just changed when the event occurred), a logic "0" results at the output of gate 42 and a logic "1" at the output of gate 43, so that output 61 of buffer 60 is enabled and fed to the thirty-two most significant bit lines of output 39. Conversely, if the said two bits are mutually different (which means, with the above assumption, that the count at outputs 29,30,31, 18 lies in the range 4-7 or 12-15, i.e. the most significant bit thereof was about to change when the event occurred) gate 43 produces a logic "0"

and gate 42 a logic "1", so that output 38 of register 37 is fed to output 39. After the 35-bit quantity at output 39 has been recorded input 46 is taken high again to await the next event; obviously it must remain high for a sufficient time to allow both registers 34 and 37 to be reloaded.

Register 37 and the gates 41-43 are provided, and the clocking of registers 34 and 37 is offset by approximately one quarter period relative to each half of each count sequence at the outputs 29,30,31, 18, in order to resolve any ambiguities which might otherwise occur when an event substantially coincides with a change from 1111 to 0000 at the outputs 29,30,31, 18. At such a time it could not be guaranteed, if counter 7 were simply clocked from a suitable tap of delay device 4, or without further measures being taken, direct from the output of generator 1, that counter 7 would contain the correct count, because of differential delays. It is therefore arranged in the manner set forth above that, when flip-flop 44 is reset, the numbers clocked into registers 34 and 37 correspond to the count in counter 7 appropriate to times immediately after and immediately before, respectively, the change (imminent or past) in the bit at output 18 which was closest when the event occurred. Which of these numbers is actually appropriate at the time the event occurred is detected by gate 41 the output of which enables the output of the relevant buffer 60 or register 37 accordingly when flip-flop 44 is reset. (When flip-flop 44 is in the set state the output of buffer 60 is enabled, and the output of register 37 is disabled, all the time).

It will be evident that an inverter may be included in the output of gate 41 if desired, provided that the synchronizing circuit 48-51, 53 is modified to make the least significant bit in counter 7 nominally the same as the bit at output 18, for example by transferring the input of the line 53 direct to the second tap from the input 3 of delay device 4. It will also be evident that, alternatively or in addition, the line 40 may include an inverter and be connected instead to the least significant bit output of register 37 if the output 38 of

register 37 is permanently enabled (this necessitating the provision of a gate or 3-state buffer, controlled by the output of gate 43, in the connection therefrom to the circuit output 39).

The various components of the circuit shown in the drawing may be of the following types:-

Generator arrangement 47:	100 MHz clock pulse generator feeding a ripple counter type 74S197, inverter 8 being fed from the ÷ 8 output thereof and delay device 4 being fed from the ÷ 16 output thereof.
Delay device 4 :	Type DDU-SJ-10100
Counter 7 :	8x Type 74S173 in cascade
Latch 10 :	Type 74S373
Latch 34 :	4x Type 74LS273
Latch 37 :	4x Type 74LS374
Buffer 60 :	4x Type 74LS244
Inverters 8,27,50 :	Type 74S04
Flip-flop 44 :	Type 74S74
EXCLUSIVE-OR gates 20-26,41:	Type 74LS86
AND-gates 42, 48	Type
NAND-gates 43, 45	Type

Although as described the mark-to-space ratio of the output pulses of divider 5 is substantially unity and their period is greater than or equal to 2(n-1)T, where T is the incremental delay from each to the next of the n=8 taps on delay line 4 constituting the output 9, it will be evident that this is in general not essential (provided of course that nT is greater than both the length of said output pulses and the length of the intervals therebetween). For example, if with a mark-to-space ratio of unity the length of each output pulse is changed to greater than or equal to 5T/8 but less than 3T/4 a repeating cycle of codes will still be obtained at the output 9, but this will now only comprise twelve different codes rather than sixteen, making the part of the arrangement other than the components 47, 4 and 10 inappropriate for use with these components. As another example, if the period of the output pulses is doubled and their mark-to-space ratio is changed to 1:3 the repeating sequence of codes obtained at output 9 will comprise only eight

different codes, necessitating some modification to the part of the arrangement other than the components 47, 4 and 10.

CLAIMS:

1. A timer circuit including a clock pulse generator arrangement, a delay device to which an output of the clock pulse generator arrangement is coupled and which is provided with n taps the positions of which correspond to substantially equal increments T of delay where nT is greater than both the length of the output pulses of the clock pulse generator arrangement applied thereto in operation and the length of the intervals therebetween, and a coupling from said taps to an output of the circuit, characterized in that said coupling includes a latch circuit to respective data bit inputs of which said taps are coupled in such manner that when data presented to said data bit inputs from said taps is latched in said latch circuit the latched data will be the acutal binary code currently present on said taps.

2. A circuit as claimed in Claim 1, characterized in that the mark-to-space ratio of said output pulses is substantially unity and the period of said output pulses is greater than or equal to 2(n-1)T.

3. A circuit as claimed in Claim 1 or Claim 2, characterized in that n is an integral power of 2 and a decoder is included in a coupling from the output of the latch circuit to the timer circuit output, which decoder is constructed to convert the successive n-bit codes appearing on said taps in operation to successive members of an m-bit binary code should said successive n-bit codes be supplied thereto.

4. A circuit as claimed in any preceding Claim, characterized in that it also includes a synchronous counter arrangement to which an output of said clock pulse generator arrangement is coupled and the output of which is coupled to the timer circuit output via a latch circuit.

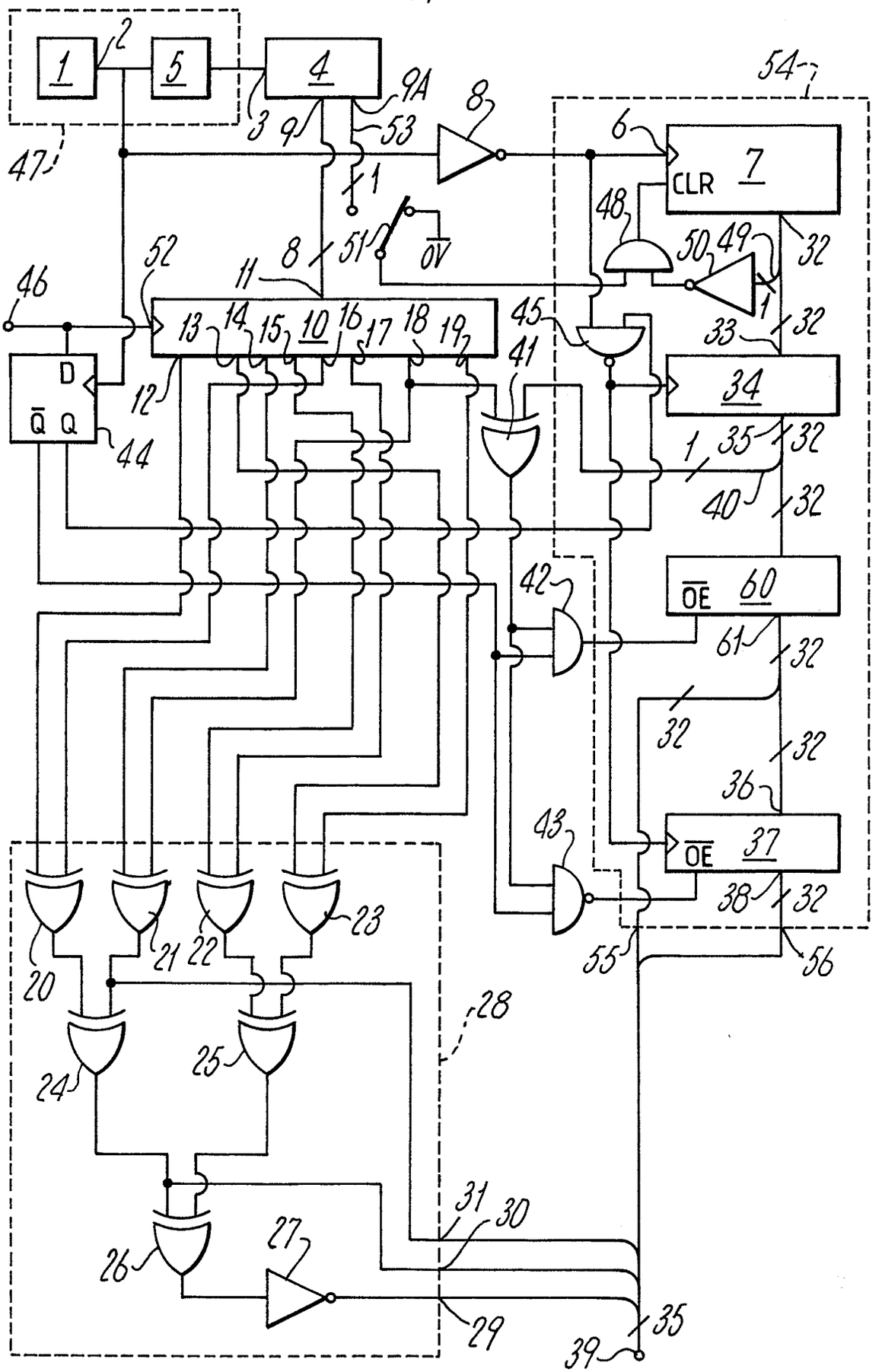
5. A circuit as claimed in Claims 2, 3 and 4 when taken together, characterized in that said counter arrangement is a binary counter arrangement constructed to produce its current count at a first output thereof and its immediately preceding count at a second output thereof, the coupling from an output of said clock pulse generator arrangement to said counter arrangement

circumventing said delay device and being such, relative to the coupling from the clock pulse generator arrangement to the delay device, that the clock pulses applied to said counter arrangement in operation will have twice the repetition rate of those applied to the delay device, resulting in the least significant bit of the outputs of said counter arrangement having the same significance as has the most significant bit of said m-bit binary code, said coupling and said counter arrangement moreover being such that the counts at said first and second outputs will be updated at instants which are offset with respect to each change in said n-bit code which corresponds to a change in the most significant bit of said m-bit binary code, comparison means being provided for comparing the value of the most significant bit of said m-bit binary code with the value of the least significant bit of the count at a said output and gating the count at one of said first and second outputs to the timer circuit output if the two compared bits have the same value and gating the count at the other of said first and second outputs to the timer circuit output if the two compared bits have opposite values.

6. A circuit as claimed in Claim 5, characterized in that said counter arrangement and the coupling thereto from the generator arrangement are such that the counts at said first and second outputs will be updated at instants which nominally lie substantially midway between each change in said n-bit code which corresponds to a change in said most significant bit.

7. A circuit as claimed in Claim 5 or Claim 6, characterized in that said counter arrangement comprises a counter, a first register to the data input of which the output of said counter is coupled, and a second register to the data input of which the data output of said first register is coupled, the data outputs of said first and second registers constituting the first and second outputs respectively of said counter arrangement and said generator arrangement being coupled to clock signal inputs of said counter and said first and second registers.

1/1


1
2
5
4
3
9
9A
53
8
54
6
CLR 7
47
1
51
0V
48
50
49
1
32
46
52
11
8
13 14 15 10 16 17 18 19
45
33
32
D
Q̄ Q
12
44
41
34
1
35
32
40
32
OE 60
42
61
32
32
32
36
43
OE 37
38
32
55
56
20
21
22
23
28
24
25
31
30
26
27
29
39
35

PHB 32945