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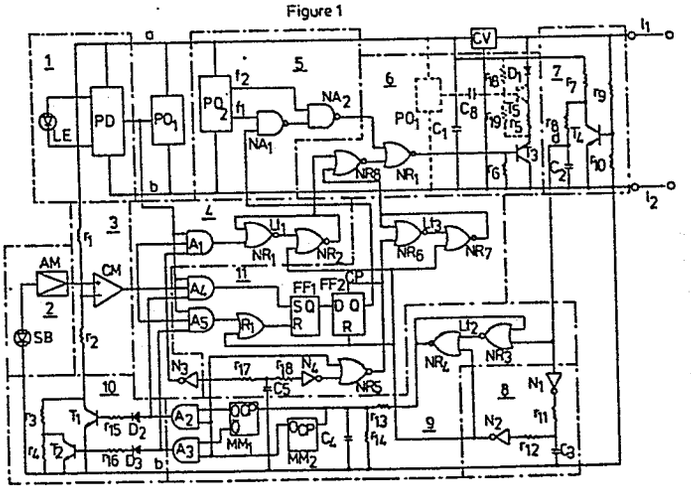
(54) Photoelectric smoke detector equipped with smoke detecting function test means.

(57) This invention relates to a photoelectric smoke detector which is capable of readily and precisely checking by itself whether light intensity reaching the smoke detector is within the normal level at which no false alarm, alarm failure nor delayed alarm is caused on the basis of the signal sent from a control panel through the lines connecting between the smoke detector and the control panel, and of reporting the result to the control panel through the same lines.

Figure 1



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Photoelectric smoke detector equipped with smoke detecting function test means.

It has been known that the operating test of the smoke detector which detects presence of smoke by scattering of light caused by entry of smoke into the light from the light emitting element and falling onto the light receiving element is carried out by increasing, from

the control panel, the output of the light emitting element to increase the output of the light receiving element with the noise light scattered in all directions on the wall surfaces in the labyrinth. Nevertheless, none of the photoelectric smoke detectors of this kind has ever had such a provision for checking, by remote operation from the control panel, the important function the detector, i.e. whether the output of the light receiving element of the detector is within the normal level range which causes no false alarm, alarm failure nor delayed alarm.

The purpose of this invention is to obtain a photoelectric smoke detector equipped with a smoke detecting function test means which, upon receipt of a signal sent from a control panel through lines connecting the smoke detector with the control panel, is capable of automatically, readily and precisely checking whether the output of the light receiving element in the smoke detector is within the normal level range, and of reporting to the control panel on the result of the check through the same lines. This invention is described below with reference to embodiments shown with figures.

Figure 1 is a circuit diagram of an embodiment according to the present invention relating to the light scattering type smoke detector which detects presence of smoke by scattered light. Figure 2 is a circuit diagram of a control panel used for this embodiment.

Shown in Figure 1 are as follows: Two lines l_1, l_2 which connect the light scattering type smoke detector shown in the Figure with the control panel shown in Figure 2. Conductors a, b connected with the lines l_1, l_2 through a voltage stabilizing circuit CV. A pulse oscillator PO_1 for synchronized signal connected between the conductors a, b. A light emitting part 1 which comprises a light emitting element LE such as light emitting diode, and a drive circuit PD connected between the conductors a, b. A light receiving part 2 comprising a light receiving element SB such as solar cell which receives light emitted by the light emitting element LE and scattered by smoke, and an amplifier AM to amplify the output of the light receiving element SB. A comparison part 3 which comprises a comparator CM with its - terminal on the input side connected with the voltage as operating level at the junction of resistors r_1, r_2 of those

resistors r_1, r_2, r_3, r_4 connected in series between the conductors a, b, and its + terminal on the input side connected with the output of the amplifier AM of the light emitting part 2. The resistors r_1, r_2, r_3, r_4 are provided to determine a fire level, an upper level of the normal level range as a threshold level at which a false alarm is likely to be produced, and a lower level of the normal level range as a threshold level at which alarm failure or delayed alarm is likely to occur. A fire discriminating part 4 which comprises an AND gate A_1 and a latch Lt_1 formed by NOR gates NR_1, NR_2. The AND gate A_1 receives outputs of the pulse oscillator PO_1 for synchronized signal, the comparator CM in the comparison part 3 and a NOT gate N_3 to the input terminal of which Q output of a monostable multivibrator MM_2 in a timer circuit 9 described hereafter is applied. The latch Lt_1 is set by output of the AND gate A_1 and cleared by output of the NOT gate N_2 in a reset signal generating circuit 8 which is described hereafter. A signal generating circuit 5 which comprises a pulse oscillator PO_2 and NAND gates NA_1, NA_2. The pulse oscillator PO_2 is connected between the conductors a, b and generates pulse outputs with low frequency f_1 and high frequency f_2. The NAND gate NA_1 receives the pulse output with frequency f_1 and the output of the flip-flop circuit FF_2 in a smoke detecting function discriminating circuit 11 described hereafter. The NAND gate NA_2 receives the pulse output with frequency f_2 and the output of the gate NA_1. A signal transmission circuit 6 which comprises NOR gates NR_8, NR_9 and a series circuit connected between the lines l_1, l_2, and sends out the pulse signal with frequency f_1, or f_2 to the lines l_1, l_2 by controlling the conduction of a transistor T_3 with output of the gate NR_9. The NOR gate NR_8 receives outputs developed when the fire discriminating part 4 has detected a fire and of a latch Lt_3 formed by NOR gates NR_6, NR_7 in the smoke detecting function discriminating circuit 11. The NOR gate NR_9 receives outputs of the NOR gate NR_8 and the NAND gate NA_2 in the signal generating circuit 5. The series circuit is formed by a diode D_1, resistor r_5 and a transistor T_3 with a resistor r_6 connected between the base and emitter. An additional circuit shown with dotted lines in the signal generating circuit 6 is provided for identifying an alarming detector at the control panel in case plural detectors are connected in parallel between the same

lines l_1, l_2. An oscillator PO_3 generating pulses which vary with each detector and have far higher frequencies than f_1, f_2 is connected between the conductors a, b. A transistor T_5 is connected between the diode D_1 and the resistor r_5. Resistors r_{18} and r_{19} are connected between the conductor a and the base of the transistor T_5, and between the base of the transistor T_5 and the collector of the transistor T_3 respectively. A capacitor C_6 is connected between the oscillator PO_3 and the base of the transistor T_5. With the pulse signal from the oscillator PO_3, each pulse of the pulse signals with frequencies f_1, f_2 sent from each detector to the lines l_1, l_2 is modulated. A signal receiving circuit 7 which receives a single pulse signal with narrow width for test start and a single pulse signal with wide width for resetting which are sent out from the control panel shown in Figure 2. The signal receiving circuit 7 is formed by resistors r_7, r_8 and a capacitor C_2 which are connected in series between the conductors a, b; an output line d which is led from the junction between the resistor r_8 and the capacitor C_2 to a reset signal generating circuit 8 and a timer circuit 9 described hereafter; and a transistor T_4, conduction of which is controlled by voltage at the junction of the resistors r_9, r_{10} connected in series between the lines l_1, l_2 and which shorts the series circuit of the resistor r_8 and the capacitor C_2 when became conductive. The reset signal generating circuit 8 confirms receipt of the reset signal from the control panel and transmits the reset signal to the detector. The reset signal generating circuit 8 is equipped with a capacitor C_3 which is charged with output of the signal receiving circuit 7 through a NOT gate N_1 and a resistor r_{11}, and produces the reset signal with the voltage of the capacitor C_3 through the resistor r_{12} and NOT gate N_2. The timer circuit 9 operates when the signal receiving circuit 7 has received the test start signal from the control panel, and comprises a latch Lt_2, resistors r_{13}, r_{14}, a capacitor C_4, monostable multivibrators MM_1, MM_2 and AND gates A_2, A_3. The latch Lt_2 is formed by NOR gates NR_3, NR_4 which are set by output of the signal receiving circuit 7. The output of the latch Lt_2 is sent to the monostable multiviblators MM_1, MM_2 having a short and long operating time respectively through the delay circuit formed by the resistor r_{13}, capacitor C_4 and resistor r_{14} to prevent the timer circuit 9 from operating with the output of the

latch Lt_2 when the signal receiving circuit 7 has received the reset signal from the control panel. The output of the monostable multivibrators MM_1, MM_2 are applied to the input terminals of the AND gates A_2, A_3. An operating level changeover circuit 10 which changes over the operating level of the comparator CM in the comparison part 3, and operates as follows. With the output of the AND gate A_2 in the timer circuit 9 transmitted through a diode D_2 and a resistor r_{15}, the transistor T_1 becomes conductive and shorts the series circuit formed by resistors r_3, r_4. With the output of the AND gate A_3 transmitted through a diode D_3 and a resistor r_{16}, the transistor T_2 becomes conductive and shorts the resistor r_4 alone. Thus, the voltage applied as operating level to the - terminal on the input of the comparator CM in the comparison part 3 becomes the fire level of the light scattering type smoke detector while the both transistors T_1, T_2 are not conducting. As the transistor T_1 become conductive, the voltage becomes the lower limit of the normal level range as a threshold level of the detector at which alarm failure or delayed alarm is likely to occur. As the transistor T_2 becomes conductive, the voltage becomes the upper level of the normal level range as a threshold level of the detector at which a false alarm is likely to be produced. A smoke detecting function discriminating circuit 11 which comprises AND gates A_4, A_5, OR gate R_1, R - S flip-flop circuit FF_1, D-type (delayed) flip-flop circuit FF_2, resistors r_{17}, r_{18}, capacitor C_5, NOT gate N_4, NOR gate NR_5 and latch Lt_3 formed by NOR gates NR_6, NR_7. The AND gates A_4, A_5 are connected with the outputs of the pulse oscillator PO_1 for synchronized signal, the comparator CM in the comparison part 3 and AND gates A_2, A_3 in the timer circuit 9. The R - S flip-flop circuit FF_1 receives the output of the AND gate A_4 as set input and the output of the OR gate R_1 as reset input which is connected with the outputs of the AND gate A_5 and the reset signal generating circuit 8. The D type flip-flop circuit FF_2 receives Q output of the flip-flop circuit FF_1 as D input, the clock signal as CP input generated by the NOR gate NR_5 and the output of the circuit 8 as reset input. The NOR gate NR_5 serving as clock signal generator is connected with the Q output of the monostable multivibrator MM_2 in the timer circuit 9 and the output of the NOT gate N_4 to which the voltage of the capacitor C_5 charged with the Q output through the resistor r_{17} is applied through

the resistor r_{18}. The latch Lt_3 formed by the NOR gates NR_6, NR_7 receives the output of the NOR gate NR_5 as set input and is cleared by output of the reset signal generating circuit 8.

Shown in Figure 2 are; a d.c. power supply E; a detecting circuit M for abnormal signal with frequency f_2 including a fire signal; a detecting circuit N for normal signal with frequency f_1; a relay X which operates when a test start switch SW_1 has closed; a relay Y which operates when a reset switch SW_2 has closed; a test start signal generator TS which operates when the contact x_1 of the relay X has closed; a reset signal generator RS which operates when the contact y_1 of the relay Y has closed; a fire indicator lamp La_1 which is lit through the break contact x_4 of the relay X and the make contact m_1 of the relay M; an abnormal indicator lamp La_2 which is lit through the make contact x_3 of the relay X and the make contact m_2 of the relay M; a normal indicator lamp La_3 which is lit through the make contact x_3 of the relay X and the make contact n_1 of the relay N; a timer T which starts operating when the contact x_5 of the relay X has closed; and a trouble indicator lamp La_4 which is operated through the make contact t of the timer T and the break contacts m_3, n_2 of the relays M, N to indicate accidents such as trouble in the detector lines or interruption of the lines l_1, l_2.

Firstly, operation of each part of this embodiment during the normal supervisory condition and in case of fire is described with reference to the time charts shown in Figure 3 (A). Shown in Figure 3 (A) are smoke density (1), voltage (2) on the lines l_1, l_2. During the normal supervisory condition without smoke, the voltage on the lines l_1, l_2 is E volts as shown in the left part of Figure (1) while the voltage on the output line d of the signal receiving circuit 7 is at L level as shown at the left part of Figure (3) because the transistor T_4 is conducting. Consequently, in the reset signal generating circuit 8, the output of the NOT gate N_1 becomes H level. With this output the capacitor C_3 is charged, and the output of the NOT gate N_2 becomes L level, thus no reset signal is generated as shown at the left part of Figure (4). In the timer circuit 9, the latch Lt_2 formed by the NOR gates NR_3, NR_4 has the input of L level, and accordingly its output, too, is at L level as shown in the left part of Figure (5), thus no

clock signal is generated. As shown in Figures (6), (7), the Q outputs of the monostable multivibrators MM_1, MM_2 are at L level, the $\overline{Q}$ output of the former MM_1 is at H level, and the outputs of the AND gates A_2, A_3 are at L level. Therefore, the transistors T_1, T_2 in the operating level changeover circuit 10 do not switch on, and as shown with the dotted line in Figure (11) the operating level of the comparator CM in the comparison part 3 is at fire level L_3 which is determined by dividing ratio of the resistance values of the resistors r_1 are $r_2+r_3+r_4$. The light emitting element LE emits light through the driving circuit PD in the light emitting part 1 each time the pulse oscillator PO_1 generates the synchronizing signal as shown in Figure (10). With the scattered light from the inner wall of the labyrinth the output amplifier AM of the light receiving element SB in the light receiving part 2 gives off an output as shown in Figure (11). Nevertheless, since this output is below the fire level L_3 under the condition without smoke, the comparator CM in the comparison part 3 has no output as shown in the left part of Figure (12). In the fire discriminating part 4 the output of the NOT gate N_3 is at H level because the Q output of the monostable multivibrator MM_2 in the timer circuit 9 is at L level. However, since the output of the comparator CM is at L level, the output of the AND gate A_1 becomes L level, and accordingly the input of the latch Lt_1 formed by NOR gates NR_1, NR_2 and the output of the NOR gate NR_2 are at L level as shown in the left part of Figure (13). In the smoke detecting function discriminating circuit 11 the output of the comparator CM in the comparison part 3 being at L level, the outputs of the AND gates A_4, A_5 are at L level. Accordingly the output of the OR gate R_1 is at L level and the Q output of the R - S flip-flop circuit FF_1 is at L level as shown in Figure (14). The Q output of the monostable multivibrator MM_2 in the time circuit 9 is at L level while the output of the NOT gate N_4 is at H level. Accordingly, the outputs of the NOR gate NR_5 serving as clock signal generator, the Q output of the D-type flip-flop circuit FF_2 and the output of the latch Lt_3 formed by NOR gate NR_6, NR_7 are at L level as shown in Figure (16), (15) and (17) respectively. Therefore, in the signal generating circuit 5 the pulse oscillator PO_2 produces pulses with frequencies f_1 and f_2 shown in Figure (18) and (19) respectively. With the pulse having frequency f_1 and the Q output of

the circuit FF_2 being at L level, the output of the NAND gate NA_1 becomes continuous H level. With the pulse signal having frequency f_2 and the continued H level output of the NAND gate NA_1, the NAND gate NA_2 generates a pulse signal with a phase opposite to that of the pulse signal having frequency f_2 from the pulse oscillator PO_2 as shown in Figure (20). Since the output of the NOR gate NR_8 in the signal transmission circuit 6 is at H level, the output of the NOR gate NR_9 is at L level as shown in the left part of Figure (21), consequently the transistor T_3 does not become conductive, and no output appears on the lines l_1, l_2 as shown in the left part of Figure (2).

When smoke generated by fire enters the labyrinth and its density exceeds the fire level L_3 as shown in the middle part of Figure (1), the amplifier AM for the light receiving element SB generates a pulse signals exceeding the fire level L_3 as shown in Figure (11), and the comparator CM generates a corresponding pulse signal as shown in Figure (12) at the time of light emission from the light emitting element LE. With this pulse signal, the synchronizing signal generated by oscillator PO_1 as shown in Figure (10) and the H level output of the NOT gate N_3, the AND gate A_1 generates a pulse signal corresponding to the output of the comparator CM. This pulse signal sets the output of the latch Lt_1 formed by NOR gates NR_1, NR_2 as shown in Figure (13), and the NOR gate NR_2 generates a fire detecting output. With the fire detecting output from the NOR gate NR_2, the output of the NOR gate NR_8 in the signal transmission circuit 6 becomes L level. With this L level output and the pulse signal of frequency f_2 from the NAND gate N_2 in the signal generating circuit 5 as shown in Figure (20), the NOR gate NR_9 generates a pulse signal with frequency f_2 as shown in Figure (21) and sends an abnormal signal with frequency f_2 as fire signal as shown in Figure (2) to the lines l_1, l_2 through the transistor T_3. As the abnormal signal detecting circuit M in the control panel shown in Figure 2 detects the fire signal, the contact m_1 closes and the fire indicator lamp La_1 lights. In order to reset the alarming detector the reset switch SW_2 on the control panel is closed to operate the relay Y. Then, the contact y_1 closes to operate the reset signal generator RS, which sends out the reset signal as shown with the symbol P_2 in Figure (2) to the lines l_1, l_2. With the signal P_2 the transistor T_4 in the signal receiving circuit 7 in the detector stops conducting,

and the signal P_2 as shown in Figure 3 (3) is generated in the output line d in the circuit 7, As a result of this, the output of the NOT gate N_1 in the reset signal generating circuit 8 becomes L level, and the charge on the capacitor C_3 is released through the NOT gate N_1. When the input of the NOT gate N_2 becomes L level, the NOT gate N_2 generates the clear signal c as shown in Figure (4). On the other hand, if the output P_2 of the circuit 7 is received by the input terminal of the latch Lt_2 formed by NOR gates NR_3, NR_4 in the timer circuit 9 before the NOT gate N_2 generates the clear signal, the latch Lt_2 is set and the NOR gate NR_4 gives an output at H level as shown in Figure (5). With the output of the NOR gate NR_4 the capacitor C_4 is charged as shown with the dotted line in Figure (5) through the resistor r_{13}. Since the circuit 8 generates the clear signal c as shown in Figure (4) before the capacitor voltage reaches such a level as may be judged as a clock signal, the setting of the latch Lt_2 is cleared by this signal c and the charge on the capacitor C_4 is released through the resistor r_{14}, thus no clock signal is generated. When resetting the detector in the above manner, if the smoke density is below the fire level L_3 as shown in Figure (1), setting of the latch Lt_1 formed by NOR gates NR_1, NR_2 is cleared by the clear signal c shown in Figure (4), and the fire detecting output of the NOR gate NR_2 stops as shonw in Figure (13). Then the output of the NOR gate NR_6 in the signal transmission circuit 6 becames H level, and the output of the NOR gate NR_9 stops, thus no fire signal is sent to the lines l_1, L_2. Consequently, the abnormal signal detecting circuit M in the control panel shown in Figure 2 no longer detects the fire signal, thus the contact m_1 opens, and the fire indicator lamp La_1 extinguishes.

Operation of each part at the time of testing while the output of the amplifier AM in the light receiving part 2 is within the normal level range is described below with reference to the time chart shown in Figure 4 (A).

As the test start switch SW_1 in the control panel shown in Figure 2 is closed, the relay X operates and the contacts $x_1 \sim x_3$ close. The test start signal generator TS sends the test start signal shown with a symbol P_1 in Figure 4A (2) to the lines l_1, l_2 to interrupt, for a short time, conduction of the transistor T_4 in the signal receiving

circuit 7 of the detector shown in Figure 1. The circuit 7 generates the pulse signal P_1' in the output line d as shown in Figure (3). With the signal P_1', the output of the NOT gate N_1 in the reset signal generating circuit 8 becomes L level, and the charge on the capacitor C_3 is released through the NOT gate N_1. Nevertheless, before the voltage of the capacitor C_3 raises the output of the NOT gate N_2 to H level, the output P_1' disappears and the output of the NOT gate N_1 again becomes H level. Therefore, the capacitor C_3 is recharged, thus the NOT gate N_2 maintains the L level output as shown in Figure (4). The output P_1' of the circuit 7 also sets the latch Lt_2 formed by NOR gates NR_3, NR_4 in the timer circuit 9. As the capacitor C_4 is charged with the H level output of the NOR gate NR_4 through the resistor r_{13} as shown with the dotted line in Figure (5) and its voltage reaches the H level, the clock signal is sent to the CP terminals of the monostable multivibrators MM_1, MM_2 with this voltage. At the Q terminals of the monostable multivibrators MM_1, MM_2, H level outputs develop as shown in Figures (6), (7), and a L level output develops on the $\overline{Q}$ terminal of the monostable multivibrator MM_1, then the output of the AND gate A_2 becomes H level as shown in Figure (8). The transistor T_1 in the operating level changeover circuit 10 too is conducting while the output of the AND gate A_2 is at H level. Thus, the operating level of the comparator CM in the comparison part 3 becomes the lower level L_1 of the normal level range which is determined by resistance dividing ratio of the resistor r_1, r_2, as shown with the dotted line in Figure (11). Furthermore, since the Q output of the monostable multivibrator MM_2 is at H level, the output of the NOT gate N_3 becomes L level and inhibits operation of the AND gate A_1. On the other hand the capacitor C_5 in the function discriminating circuit 11 is charged. When its voltage reaches a predetermined value, the output of the NOT gate N_4 becomes L level, but the other input of the NOR gate NR_5 is at H level. Therefore, the NOR gate NR_5 does not produce the clock signal.

Under this condition, if the pulse output of the amplifier AM in the signal receiving part 2 lies between the lower level L_1 and the upper level L_2 of the normal level range as shown in Figure (11), the comparator CM generates detecting pulse signal as shown in Figure

(12) because the pulse output of the amplifier AM is above the operating level of the comparator CM. With this pulse output of the comparator CM, synchronized signal generated by the pulse oscillator PO_1 and H level output of the AND gate A_2, the AND gate A_4 generates the pulse output similar to that of the comparator CM as shown in Figure (12). This output of the AND gate A_4 sets the Q output of the circuit FF_1 in the function discriminating circuit 11 at H level as shown in Figure (14). On the other hand the Q output of the circuit FF_2 remains at L level as shown in Figure (15) because the CP terminal receives no clock signal from the NOR gate NR_5.

After lapse of a predetermined short time the Q output and $\overline{Q}$ output of the monostable multivibrator MM_1 in the timer circuit 9 become L level and H level respectively as shown in Figure (6). Consequently, the output of the AND gate A_2 becomes L level as shown in Figure (8), inhibiting operation of the AND gate A_4 in the circuit 11, and rendering the transistor T_1 in the circuit 10 non conductive. On the other hand, the output of the AND gate A_3 becomes H level as shown in Figure (9), the transistor T_2 becomes conductive, and the operating level of the comparator CM in the comparison part 3 reaches the upper level of the normal level range as shown with the symbol L_2 in Figure (11) which is determined by dividing ratio of the resistors r_1 and r_2+r_3. Under this condition, if the amplifier AM in the light receiving part 2 has the normal output as shown in Figure (11), the output of the comparator CM is at L level as shown in Figure (12) because the output of the amplifier AM is below the level L_2.

When the output of the monostable multivibrator MM_2 becomes L level as shown in Figure (7) after lapse of a predetermined long time, this L level output and the output of the NOT gate N_4 in the function discriminating circuit 11 at L level cause the NOR gate NR_5 to generate the clock signal c as shown in Figure (16). With this signal c, the Q output of the flip-flop circuit FF_2 becomes H level as shown in Figure (15) because the Q output of the flip-flop circuit FF_1 is at H level as shown in Figure (14). With the H level output of the flip-flop circuit FF_2, the NAND gate NA_1 in the signal generating circuit 5 generates a pulse signal having the phase opposite to that of the

pulse signal with frequency f_1 generated by the oscillator PO_2, and the NAND gate NA_2 generates a pulse signal with frequency f_1 as shown in Figure (20). The clock signal from the NOR gate NR_5 sets the latch Lt_3 formed by NOR gates NR_6, NR_7, and the output of the NOR gate NR_7 becomes H level. With this H level output, the output of the NOR gate NR_8 in the signal transmission circuit 6 becomes L level, and the NOR gate NR_9 generates a pulse signal with frequency f_1 as shown in Figure (21), by which conduction of the transistor T_3 is controlled and the normal signal shown in Figure (2) is sent to the lines l_1, l_2.

Lastly, as the signal receiving circuit 7 has received the reset signal P_2 shown in Figure (2) and has an output P_2' shown in Figure (3) on its output line d, the NOT gate N_2 in the reset signal generating circuit 8 generates a clear signal c shown in Figure (4), which resets the latches Lt_2, Lt_3 formed by NOR gates NR_3, NR_4 and NR_6, NR_7 respectivel in the same manner as resetting in case of fire. Then, the outputs of the NOR gates NR_4, NR_7 become L level as shown in Figure (5) and (17) respectively. With the L level output of the NOR gate NR_7, the NOR gate NR_9 no longer generates the pulse signal as shown in Figure (21), and accordingly the signal transmission circuit 6 stops transmitting the normal signal as shown in Figure (2). The clear signal from the NOT gate N_2 resets the flip-flop circuit FF_1 in the function discriminatin circuit 11 through the OR gate R_1, and the flip-flop circuit FF_2 directly. The Q outputs of the both circuits become L level as shown in Figures (14), (15). With the L level output of the flip-flop circuit FF_2, the output of the NAND gate NA_1 in the signal generating circuit 5 become H level and the NOT gate NA_2 generates the pulse signal with frequency f_2 as shown in Figure (20), thus each part of the detector returns to the original state.

Now, the following describes operation of each part during the test with reference to the time chart shown in Figure 5 (A) in case that the output of the amplifier AM has been reduced below the lower level L_1 of the normal level range due to soiling by dust accumulating over the light receiving surface of the light receiving element SB in the light receiving part 2.

In this case, too, the signal receiving circuit 7 in Figure 1 generates a pulse signal P_1' in the output line d with the test start signal P_1

from the control panel shown in Figure 5 (A) (2). However, due to narrow pulse width of the pulse signal P_1', the NOT gate N_2 in the reset signal generating circuit 8 generates no clear signal. On the other hand the latch Lt_2 formed by NOR gates NR_3, NR_4 in the timer circuit 9 is set as shown in Figure (5) with the pulse signal P_1'. When the capacitor C_4 is charged with the H level output of the NOR gate NR_4 through the resistor r_{13} as shown with the dotted line in Figure 5 (A) (5) and the voltage reaches the H level, outputs of H level develop at the Q terminals of the monostable multivibrators MM_1, MM_2 as shown in Figure (6), (7), and the output of the AND gate A_2 becomes H level. Then, the transistor T_1 in the operating level changeover circuit 10 becomes conductive as shown in Figure (8), and the operating level of the comparator CM in the comparison part 3 becomes the lower level L_1 of the normal level range as shown with the dotted line in Figure (11).

With the H level output of the monostable multivibrator MM_2, the output of the NOT gate N_3 in the fire discriminating part 4 becomes L level and inhibits operation of the AND gate A_1, while on the other hand the NOR gate NR_5 in the function discriminating circuit 11 generates no clock signal as shown in Figure (16).

Under this condition, if the output of the amplifier AM in the light receiving part 2 is below the level L_1 as shown in Figure (11), the transistor T_1 in the operating level changeover circuit 10 becomes conductive as shown in Figure (8). Therefore, even if the operating level of the comparator CM in the comparison part 3 becomes the lower level L_1 as shown in Figure (11), no detecting signal is generated in the comparator CM as shown in Figure (12), the AND gate A_4 in the function discriminating circuit 11 has no output, and the flip-flop circuit FF_1 is not set as shown in Figure (14).

Then, after lapse of a predetermined time, the Q output of the monostable multivibrator MM_1 in the timer circuit 9 becomes L level as shown in Figure 6, and the $\overline{Q}$ output becomes H level. The outputs of the AND gates A_2, A_3 become L and H levels respectively as shown in Figures (8), (9), thus rendering the transistor T_1 non-conductive and the transistor T_2 conductive. Consequently the operating level of the comparator CM becomes the level L_2 as shown in Figure (11). Enen

at this level L_2, the comparator CM has no output as shown in Figure (12), and the AND gate A_5, too, has no output. After further lapse of a predetermined time the Q output of the monostable multivibrator MM_2 becomes L level as shown in Figure (7), and the NOR gate NR_5 generates the clock signal c shown in Figure (16), which sets the latch Lt_3. As the output of the NOR gate NR_8 in the signal transmission circuit 6 becomes L level with the H level output of the NOR gate NR_7 shown in Figure (17), the NOR gate NR_9 generates a pulse signal with frequency f_2 as shown in Figure (21) because the NAND gate NA_2 in the signal generating circuit 5 is generating a pulse signal with frequency f_2 as shown in Figure (20). By the pulse signal from the NOR gate NR_9, conduction of the transistor T_3 is controlled, and the abnormal signal is sent to the control panel through the lines l_1, l_2 as shown in Figure (2).

The following describes operation of each part during the test with reference to the time chart shown in Figure 6 (A), which is carried out in case the output of the amplifier AM for the light receiving element SB in the light receiving part 2 has exceeded the upper level L_2 of the normal level range due to accumulation of dust in the labyrinth.

As in the case of the foregoing, the signal receiving circuit 7 in Figure 1 generates the pulse signal P_1' in the output line d shown in Figure (3) with the test start signal P_1 from the control panel shown in Figure 6 (A) (2). Although the NOT gate N_2 in the reset signal generating circuit 8 does not generate the clear signal, the latch Lt_2 in the timer circuit 9 is set. The capacitor C_4 is charged with the H level output of the NOR gate NR_4 as shown with the dotted line in Figure (5). When the voltage reaches the H level, outputs of H level develop at the Q terminals of the monostable multivibrators MM_1, MM_2 as shown in Figure (6), (7) and the output of the AND gate A_2 becomes H level. Then, the transistor T_1 in the operating level changeover circuit 10 becomes conductive as shown in Figure 6 (8), and the operating level of the comparator CM in the comparison part 3 becomes the lower level L_1 of the normal level range as shown with the dotted line in Figure (11). With the H level output of the Q terminal of the monostable multivibrator MM_2, the output of the NOT gate N_3 in the fire discriminating circuit 4 becomes L level and inhibits operation of the AND gate A_1,

while on the other hand the NOR gate NR_5 in the function discriminating circuit 11 generates no clock signal.

Under this condition, if the output of the amplifier AM in the light receiving part 2 is over the level L_2 as shown in Figure (11), the transistor T_1 in the operating level changeover circuit 10 become conductive as shown in Figure (8). As the operating level of the comparator CM in the comparison part 3 becomes the level L_1 as shown in Figure (11), the output of the comparator CM becomes the H level. With this output of the comparator CM, the output of the AND gate A_4 in the function discriminating circuit 11 becomes H level, and accordingly the Q output of the flip-flop circuit FF_1 is set at H level as shown in Figure (14). However, since the CP terminal of the flip-flop circuit FF_2 receives no clock signal from the NOR gate NR_5, the Q output of the flip-flop circuit remains at L level. After lapse of a predetermined time under this condition, the Q output of the monostable multivibrator MM_1 in the timer circuit 9 becomes L level as shonw in Figure (6) and $\overline{Q}$ output becomes H level. The outputs of the AND gates A_2, A_3 become L and H levels respectively as shown in Figure (8), (9). Thus, the transistor T_1 becomes non-conductive and the transistor T_2 conductive. Then, the operating level of the comparator CM changes to level L_2 as shown in Figure (11), the output of the comparator CM remains at H level. With this output the AND gate A_5 and the OR gate R_1 generate H level outputs successively. With the output reaching the reset terminal R of the flip-flop circuit FF_1, the Q output of the flip-flop circuit FF_1 is reset at the L level as shown in Figure (14). Even if the comparator CM has an output thereafter, the Q output of the flip-flop circuit FF_1 remains at L level as shown in Figure (14) as long as the operating level of the comparator CM is at the level L_2, because the output of the comparator CM reaches the R terminal of the flip-flop circuit FF_1 through the AND gate A_5 and the OR gate R_1. As in the previous case, after lapse of a predetermined time the Q output of the monostable multivibrator MM_2 becomes L level as shown in Figure (7), and the NOR gate NR_5 in the circuit 11 generates the clock signal c shown in Figure (16), which sets the latch Lt_3. As the NOR gate NR_7 has H level output shown in Figure (17), and the output of the NOR gate NR_8 in the signal transmission circuit 6 becomes the L level, the NAND gate NA_2 in the signal generating circuit 5 generates a pulse signal with frequency f_2 as shown in Figure

(20), and accordingly the NOR gate NR_9 generates a pulse signal of frequency f_2 as shown in Figure (21) to control conduction of the transistor T_3 and to send an abnormal signal to the control panel through the lines l_1, l_2 as shown in Figure (2).

Now, the following describes how the signal receiving circuit 7 operates with the reset signal P_2 shown in Figure 5 (A) and 6 (A) (2) and received from the control panel after the test conducted in case that the output of the amplifier AM has fallen below the lower level L_1 and exceeded the upper level L_2. The signal receiving circuit 7 generates a pulse signal P_2' shown in Figure (3) in the output line d. The NOT gate N_2 in the reset signal generating circuit 8 generates the clear signal c shown in Figure 6 (4), with which the latches Lt_2, Lt_3 formed by NOR gates NR_3, NR_4 and NR_6, NR_7 respectively are reset. Then, the outputs of the NOR gates NR_4, NR_7 become L level as shown in Figures (5) and (17). Because of this L level output of the NOR gate NR_7, the NOR gate NR_9 no longer generates the pulse signal as shown in Figure (21), and the signal transmission circuit 6 stops transmitting the abnormal signal to the lines l_1, l_2 as shown in Figure (2), thus each part of the detector resets to the original condition.

Lastly, the following describes operation of the control panel when the test is conducted with the test start signal from the control panel shown in Figure 7. When the switch SW_1 is closed for testing, the relay X operates to close the contacts $x_1 \sim x_3$ and open the contact x_4. Therefore, on receipt of the normal signal from the detector shown in Figure 1, the relay N operates and close the contact N_1, and the normal indicator lamp La_3 lights. When the abnormal signal is received, the relay M operates and closes the contacts m_1, m_2 to cause the abnormal indicator lamp La_2 to light up indicating that there is abnormality in the smoke detecting function. As the switch SW_2 is closed to reset the detector, the relay Y operates and closes the contact y_1 and opens the contact y_2 to actuate the reset signal generator RS which sends the reset signal to the lines l_1, l_2. At the same time, operation of the relay X is stopped and the contacts x_1, x_2, x_3 are opened to prevent the test signal generator TS from operating and to extinguish the normal indicator lamps La_2, La_3. The contact x_4 is closed to reset the control panel in the normal supervisory condition.

Figure 7 is a circuit diagram of another embodiment according to the present invention relating to a light extinction type smoke detector which detects smoke on light extinction principle. The circuit diagram of the control panel used for this embodiment is the same as Figure 2. The light extinction type smoke detector shown in Figure 7 only differs from Figure 1 in that the resistors $r_1 \sim r_4$ are connected in series across the conductors a, b in opposite order to determine the upper level L_1 of the normal level range as threshold level at which alarm failure or delayed alarm is likely to occur, a lower level L_2 as threshold level at which false alarm is likely to be produced, and the fire level L_3, and that the voltage of operating level developing at the junction of the resistors r_1 and r_2 is applied to the + terminal of the comparator CM in the comparison part 3 and the output of the amplifier AM in the light receiving part 2 is led to the - terminal so that the comparator CM generates the detecting output when the output of the amplifier AM has fallen below the operating level. Therefore, as compared with the time chart of Figure 3 (A) of the embodiment shown in Figure 1, the normal supervisory state of this embodiment and the operating state of each part in case of fire only differs in the outputs of the amplifier AM in the light receiving part 2 and of the comparator CM in the comparison part 3 as shown in Figures (11) and (12). Therefore, these different outputs shown with Figures (11), (12) are extracted and indicated at the lower part of Figure 3 (A) as Figures (B) (11'), (12').

Now, operation of the embodiment is described with reference to Figures 3 (A) but (11), (12), and (B) (11'), (12'). With respect to Figure 3 (A) some descriptions have already been made, and only their summary is given hereunder. In normal supervisory condition without smoke the transistor T_1 in the signal receiving circuit 7 is conducting and its output line d has no output as shown in the left part of Figure (3). Consequently, the outputs of the reset signal generating circuit 8 and of the AND gates A_2, A_3 in the timer circuit 9 are L level, and the transistors T_1, T_2 in the operating level changeover circuit 10 do not conduct. As the operating level of the comparator CM in the comparison part 3 is at the fire level L_3 (e.g. 85% light transmittivity of the output of the amplifier AM as indication of light transmittivity while

no smoke presents), the comparator CM has the L level output shown in Figure (12') and the output of the AND gate A_1 is at the L level when the amplifier AM generates a pulse signal exceeding the level L_3 shown in Figure (11'). Consequently, no signal is sent to the lines l_1, l_2. Nevertheless, when the amplifier AM has generated a pulse signal below the fire level as shown Figure (11') as a result of entry of smoke from fire between the light emitting element LE in the light emitting part 1 and the light receiving element SB in the light receiving part 2, the comparator CM has the H level output as shown in Figure (12'), with which and the synchronizing signal from the oscillator PO_1 and the H level output of the NOT gate N_3, the AND gate A_1 in the fire detecting part 4 generates a pulse signal corresponding to the output of the comparator CM. Then, the latch Lt_1 formed by the NOR gates NR_1, NR_2 is set as shown in Figure (13). With the H level output of the NOR gate NR_2, a fire signal with frequency f_2 shown in Figure (2) is sent to the lines l_1, l_2 through the signal transmission circuit 6. Operation of the control panel after receipt of this fire signal and resetting of the fire detector by reset signal from the control panel are same as in the case of the light scattering type smoke detector.

Operation of each part at the time of the test while the output of the amplifier AM in the light receiving part 2 of this embodiment only differs in Figure (11) showing the output of the amplifier AM in the light receiving part 2 and Figure (12) showing the output of the comparator CM in the comparison part 3 as compared with the time chart, Figure 4 (A) for the embodiment shown in Figure 1. Therefore, only these different outputs shown with Figures (11), (12) are extracted and indicated at the lower part of Figure 4 (A) as Figure (B) (11'), (12').

Now, operation of the embodiments is described with reference to Figures 4 (A) but (11), (12), and (B) (11'), (12'). With the test start signal P_1 shown in Figure (2) from the control panel the signal receiving circuit 7 generates a pulse output P_1' shown in Figure (3) in its output line d, but the reset signal generating circuit 8 does not generate the clear signal due to the narrow pulse width. The pulse signal P_1' sets the latch Lt_2 formed by NOR gates NR_3, NR_4 in the timer circuit 9. With the H level output of the NOR gate NR_4 shown

in Figure (5) the capacitor C_4 is charged as shown with the dotted line in Figure (5). As the voltage of the capacitor C_4 reaches the H level, the clock signal is transmitted to the CP terminals of the monostable multivibrators MM_1, MM_2. Then, the Q terminals of the monostable multivibrators MM_1, MM_2 have H level outputs as shown in Figures (6), (7), with which the output of the AND gate A_2, too, become the H level as shown in Figure (8), and the transistor T_1 in the operating level changeover circuit 10 becomes conductive. The operating level of the comparator CM in the comparison part 3 becomes the upper level L_1 of the normal level range (e.g. 105% light transmittivity) as shown with the dotted line in Figure (11'). Under this condition, if the pulse output of the amplifier AM in the light receiving part 2 lies between the upper level L_1 and the lower level L_2 of the normal level range as shown in Figure (11'), the pulse output is below the operating level of the comparator CM. Therefore, the comparator CM has no L level output, but H level output as shown in Figure (12'). With this H level output and the synchronizing signal from the oscillator PO_1 and the H level output of the AND gate A_2, the AND gate A_4 generates a pulse output which is similar to that shown in Figure (12). By this pulse signal the output of the Q terminal of the flip-flop circuit FF_1 in the function discriminating circuit 11 is set at H level. However, since no clock signal is transmitted from the NOR gate NR_5 to the CP terminal of the flip-flop circuit FF_2, the output of the Q terminal remains at L level as shown in Figure (15). After lapse of a predetermined time the output of the Q terminal of the monostable multivibrator MM_1 in the timer circuit 9 becomes L level as shown in Figure (6), and the output of the $\overline{Q}$ terminal becomes H level. The outputs of the AND gates A_2 and A_3 become L and H levels respectively as shown in Figures (8) and (9). In the operating level changeover circuit 10, the transistor T_1 stops conducting and the transistor T_2 become conductive, thus the operating level of the comparator CM in the comparison part 3 becomes the lower level L_2 of the normal level range. Under this condition, the output of the amplifier AM in the light receiving part 2, if generated, is above the level L_2, and therefore the output of the comparator CM becomes the L level as shown in Figure (12'). When the output of the monostable multivibrator MM_2 in the timer circuit 9 become L level as shown in Figure (7) after lapse of a predetermined

time, this L level output and the L level output of the NOT gate N_4 in the function discriminating circuit 11 cause the NOR gate NR_5 to generate the clock signal c as shown in Figure (16). With this signal c the flip-flop circuit FF_2 has the H level output shown in Figure (15) at the Q terminal. With this H level output and the H level output shown in Figure (17) of the NOR gate NR_7 of the latch Lt_3 which is set by the clock signal c, the normal signal shown in Figure (2) is sent to the lines l_1, l_2 through the signal generating circuit 5 and the signal transmission circuit 6. As the signal receiving circuit 7 receives from the control panel the reset signal P_2 shown in Figure (2), each part of the fire detector returns to its original state in the same manner as the light scattering type smoke detector.

Operation of each part at the time of the test in case the output of the light receiving element SB in the light receiving element 2 has increased due to influence of the external light and the output of the amplifier AM has exceeded the upper level L_1 of the normal level range only differs in Figure (11) showing the output of the amplifier AM and Figure (12) showing the output of the comparator CM in the comparison part 3 as compared with the time chart, Figure 5 (A) for the embodiment shown in Figure 1. Therefore, only these different outputs shown in Figures (11), (12) are extracted and indicated at the lower part of Figure 5 (A) as Figure (B) (11'), (12').

Now, operation of the embodiment is described with reference to Figure 5 (A) but (11), (12), and to Figures (B) (11'), (12'). With the test start signal P_1 shown in Figure (2) the signal receiving circuit 7 generates a pulse output P_1' shown in Figure (3) in its output line d, but the reset signal generating circuit 8 does not generate a clear signal due to the narrow pulse width. The pulse signal P_1' sets the latch Lt_2 formed by NOR gates NR_3, NR_4 in the timer circuit 9. With the H level output of the NOR gate NR_4 shown in Figure (5), the H level outputs shown in Figures (6), (7) appear on the Q terminals of the monostable multivibrators MM_1, MM_2, and the output of the AND gate A_2 becomes H level, and the transistor T_1 in the operating level changeover circuit 10 becomes conductive as shown in Figure (8). Thus, the operating level of the comparator CM becomes the upper level L_1 of the normal level range as shown with the dotted line in Figure (11'). Under this condition, if the output of the amplifier AM in

the light receiving part 2 is above the upper level L_1, the comparator CM in the comparison part 3 has no output as shown in Figure (12'), and the transistors T_1, T_2 in the operating level changeover circuit 10 become conductive as shown in Figures (8), (9). Therefore, even if the operating level of the comparator CM has changed from the level L_1 to the level L_2, the comparator CM has no output. After lapse of a predetermined time the output of the Q terminal of the monostable multivibrator MM_2 becomes L level as shown in Figure (7). The NOR gate NR_5 in the smoke detecting function discriminating circuit 11 generates the clock signal c shown in Figure (16), and the NOR gate NR_7 has the H level output as shown in Figure (17). The output of the NOR gate NR_8 in the signal transmission circuit 6 becomes L level. Then, the NOR gate NR_9 generates a pulse output with frequency f_2 as shown in Figure (21) to send the abnormal signal to the lines l_1, l_2 as shown in Figure (2).

Operation of each part at the time of the test in case the output of the amplifier AM has fallen below the lower level L_2 of the normal level range due to soiling of the light receiving surface of the light receiving element SB in the light receiving part 2 by dust only differs in Figure (11) showing the output of the amplifier AM and Figure (12) showing the output of the comparator CM as compared with the time chart, Figure 6 (A) for the embodiment shown in Figure 1. Therefore, only these different outputs shown in Figures (11), (12) are extracted and indicated at the lower part of Figure 6 (A) as Figures (B) (11'), (12').

Now, operation of the embodiment is described with reference to Figure 6 (A) but (11), (12), and to Figures (B) (11'), (12'). With the test start signal P_1 shown in Figure (2) the signal receiving circuit 7 generates a pulse output P_1' with narrow width shown in Figure (3) in its output line d, but the reset signal generating circuit 8 does not generate a clear signal. The latch Lt_2 formed by NOR gates NR_3, NR_4 is set. With the H level output of the NOR gate NR_4 shown in Figure (5) the H level outputs shown in Figures (6), (7) appear on the Q terminals of the monostable multivibrators MM_1, MM_2, and the output of the AND gate A_2 becomes H level, and the transistor T_1 in the operating level changeover circuit 10 becomes conductive as shown in Figure (8). Thus, the operating level of the comparator

CM becomes the upper level L_1 of the normal level range as shown with the dotted line in Figure (11'). If the output of the amplifier AM in the light receiving part 2 is below the lower level L_2 of the normal level range at this time, the comparator CM has no L level output but the H level output as shown in Figure (12'). With this H level output the AND gate A_4 in the function discriminating circuit 11 generates a pulse output similar to that shown in Figure (12). This pulse output sets the output of the Q terminal of the flip-flop circuit at H level as shown in Figure (14), but the output of the Q terminal of the flip-flop circuit FF_2 remains at L level because no clock signal is transmitted to the CP terminal of the flip-flop circuit FF_2. Under this condition, the transistor T_2 soon becomes conductive in place of the transistor T_1 as shown in Figure (9), and the operating level of the comparator CM changes to the level L_2 as shown in Figure (11'). In this case, too, the output of the comparator CM is at H level, with which the AND gate A_5 and OR gate R_1 successively generate H level outputs to the R terminal of the flip-flop circuit FF_1, the Q output of which becomes the L level as shown in Figure (14). After lapse of a predetermined time as the output of the Q terminal of the monostable multivibrator MM_2 becomes L level as shown in Figure (7), and the NOR gate NR_5 in the function discriminating circuit 11 generates the clock signal c as shown in Figure (16), the latch Lt_3 formed by NOR gates NR_6, NR_7 is set. Then, the NOR gate NR_7 has a H level output as shown in Figure (17), and the abnormal signal is transmitted to the control panel through the signal transmission circuit 6 and the lines l_1, l_2 in the same manner as described with regard to Figure 6 (A) for the light scattering type smoke detector.

Operation of the smoke detector when its signal receiving circuit 7 has received the reset signal P_2 from the control panel after the test in case the output of the amplifier AM exceeded the upper level L_1 of the normal level range and fallen below the lower level L_2, and operation of the control panel when tested with the test start signal from the control panel are same as in the case of the light scattering type smoke detector.

In the both cases of the light scattering type and light extinction type smoke detectors, if there is a trouble in the detector circuit

or interruption of the lines l_1, l_2, and neither normal signal nor abnormal signal from the detector reaches the control panel despite the lapse of the operating time of the timer T after the test start signal is sent from the control panel shown in Figure 2, the timer T operates and closes its contact t to operate the trouble indicator lamp La_4, by which it is possible to know the trouble in the detector circuit or lines l_1, l_2.

In the above embodiments, the descriptions are made with respect to such cases that the smoke detector and the control panel are connected by two lines which are commonly used as power supply lines and signal lines. However, in Figures 1 and 7 the terminal on the right side of the voltage stabilizing circuit CV may be disconnected from the line l_1 and connected with a third line l_3 which is exclusively used for power supply so that the power supply lines may be separated from the signal lines to avoid influence of the pulse signal width upon the voltage stabilizing circuit and to get a larger S/N ratio.

As can be seen from the above description, the photoelectric type smoke detector equipped with smoke detecting function test means according to this invention has such as advantage that with proper composition it is capable of automatically, readily and precisely checking, on the basis of the signal sent from the control panel through the lines connecting the smoke detector with the control panel, whether the output of the detector is within the normal level range which cause no false alarm, alarm failure nor delayed alarm, i.e. an important function of this type of detector, and of reporting to the control panel on results of the test through the same lines.

4. Brief Description of Drawings

Figures 1 and 7 are circuit diagrams of embodiments of the light scattering type and light extinction type smoke detectors equipped with smoke detecting function test means according to this invention. Figure 2 is a circuit diagram of a control panel which is common to these two embodiments. Figures 3 through 6 are time charts showing operating status of each part of the embodiments shown with Figures 1 and 7 in different casses, i.e. Figure 3 (A) is the one for the embodiment of Figure 1 in normal condition and in case of fire, Figure 4 (A) is the one at the time of test while the output of the embodiment

shown in Figure 1 is within the normal level range, and Figures 5 (A) and 6 (A) are the ones at the time of tests in the cases that the output of the embodiment shown in Figure 1 is below the lower limit and above the upper limit of the normal level range. Figures 3 (B) through 6 (B) shown only outputs (11') and (12') of amplifier AM and comparator CM respectively which differ from those shown in Figures 3 (A) through 6 (A) in the time charts corresponding to Figures 3 (A) through 6 (A) of the embodiment shown with Figure 7.

1	.....	Light emitting part
2	.....	Light receiving part
3	.....	Comparison part
4	.....	Fire discriminating part
5	.....	Signal generating part
6	.....	Signal transmission circuit
7	.....	Signal receiving circuit
8	.....	Reset signal generating circuit
9	.....	Timer circuit
10	.....	Operating level changeover circuit
11	.....	Smoke detecting function discriminating circuit

Claims

1. A photoelectric smoke detector equipped with smoke detecting function test means which is characterized in that an operating level changeover circuit and a smoke detecting function discriminating circuit are provided to automatically changeover, with test start signal from a control panel, the operating level from the fire level to the upper and lower level of the normal level range of the received light within which no false alarm, alarm failure nor delayed alarm is caused, and to send a normal signal to the control panel when the light received is within the normal level range, and an abnormal signal to the control panel when the light received is out of the normal level range.

2. A photoelectric smoke detector equipped with smoke detecting function test means as set forth in Claim 1 wherein changeover of the operating level is done by changeover of another input value having the equivalent operating level to that of the comparator to the input side of which the output of the received light is applied.

3. A photoelectric smoke detector equipped with smoke detecting function test means as set forth in Claim 1 wherein the normal signal and abnormal signal are discriminated by difference in pulse frequencies of the pulse signals.

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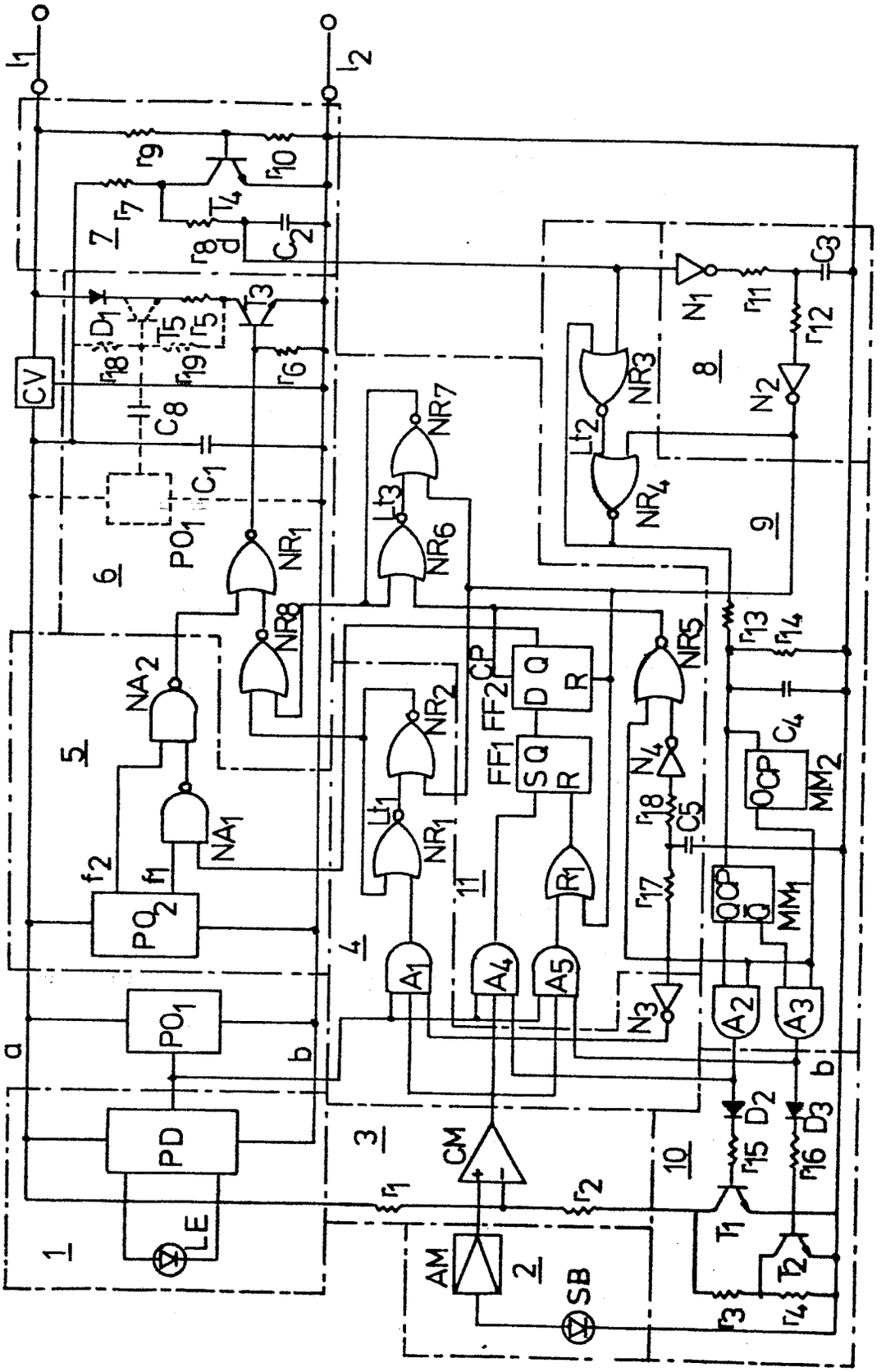
l1
l2
CV
PD
LE
AM
SB
CM
PO1
PO2
NA1
NA2
NR1
NR2
NR3
NR4
NR5
NR6
NR7
NR8
A1
A2
A3
A4
A5
N1
N2
N3
N4
FF1
FF2
R1
MM1
MM2
CP
D Q
S Q
R
T1
T2
T3
T4
T5
D1
D2
D3
C1
C2
C3
C4
C5
C8
r1
r2
r3
r4
r5
r6
r7
r8
r9
r10
r11
r12
r13
r14
r15
r16
r17
r18
r19
a
b
f1
f2
1
2
3
4
5
6
7
8
9
10
11

Figure 1

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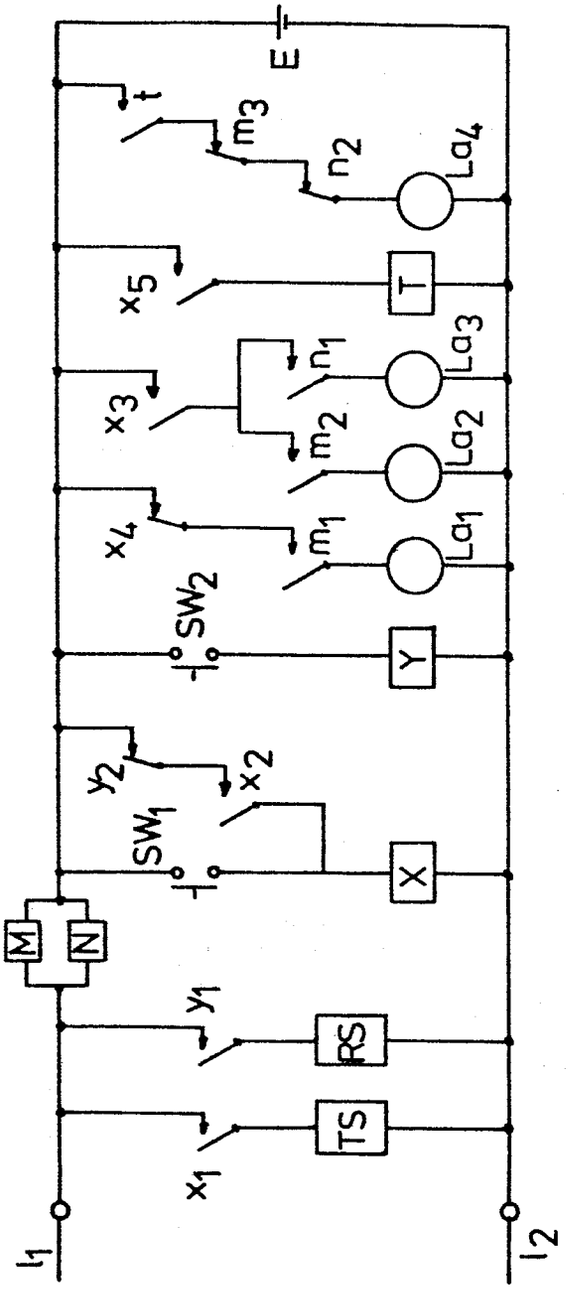
E
t
m3
n2
La4
x5
T
x3
n1
La3
m2
La2
x4
m1
La1
SW2
Y
y2
x2
SW1
X
M
N
y1
RS
TS
x1
l1
l2

Figure 2

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Figure 3

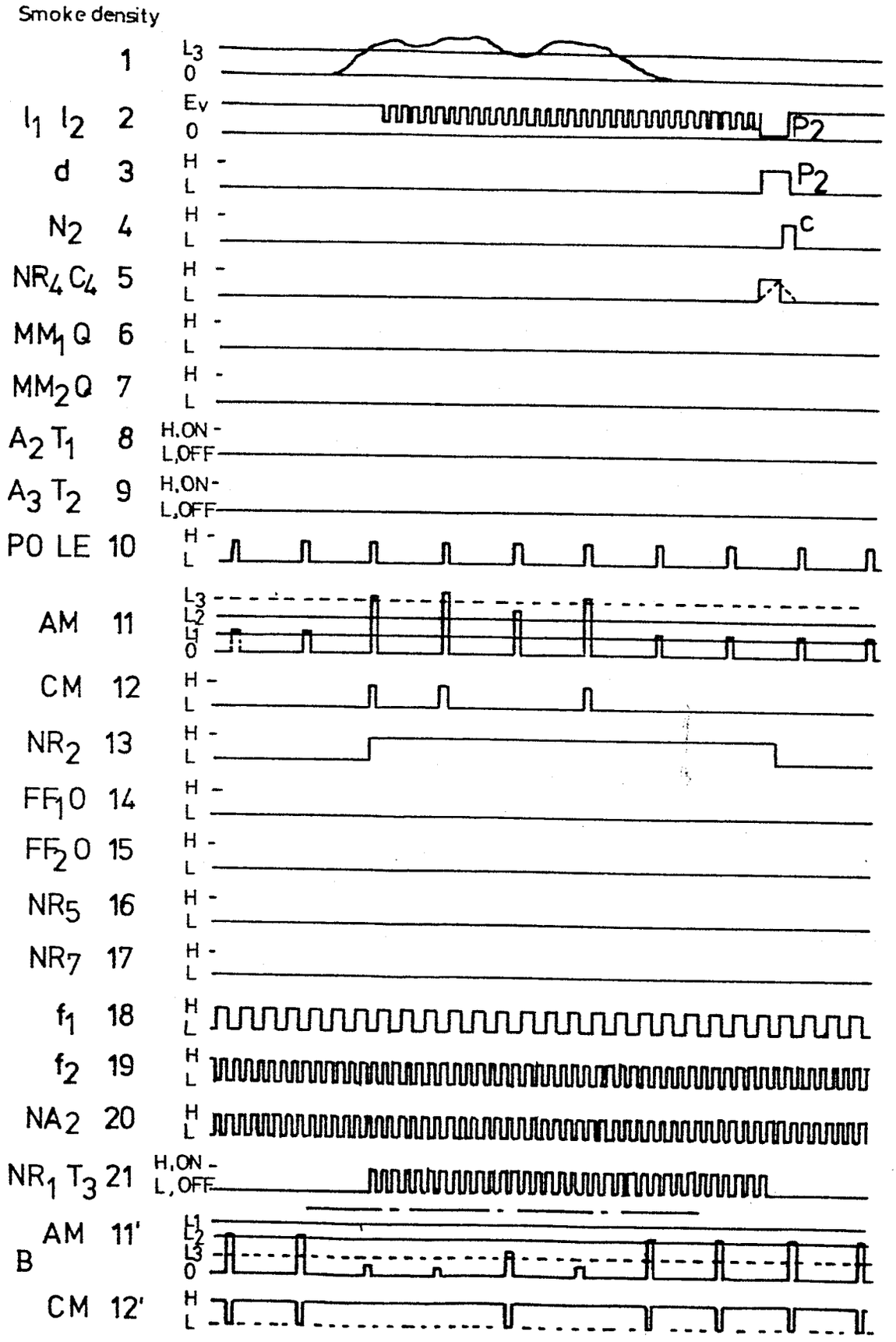
Smoke density
1
L3
0
I1 I2 2
Ev
0
P2
d 3
H
L
P2
N2 4
H
L
C
NR4 C4 5
H
L
MM1 Q 6
H
L
MM2 Q 7
H
L
A2 T1 8
H.ON
L,OFF
A3 T2 9
H.ON
L,OFF
PO LE 10
H
L
AM 11
L3
L2
L1
0
CM 12
H
L
NR2 13
H
L
FF1 O 14
H
L
FF2 O 15
H
L
NR5 16
H
L
NR7 17
H
L
f1 18
H
L
f2 19
H
L
NA2 20
H
L
NR1 T3 21
H.ON
L,OFF
B
AM 11'
L1
L2
L3
0
CM 12'
H
L

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Figure 4

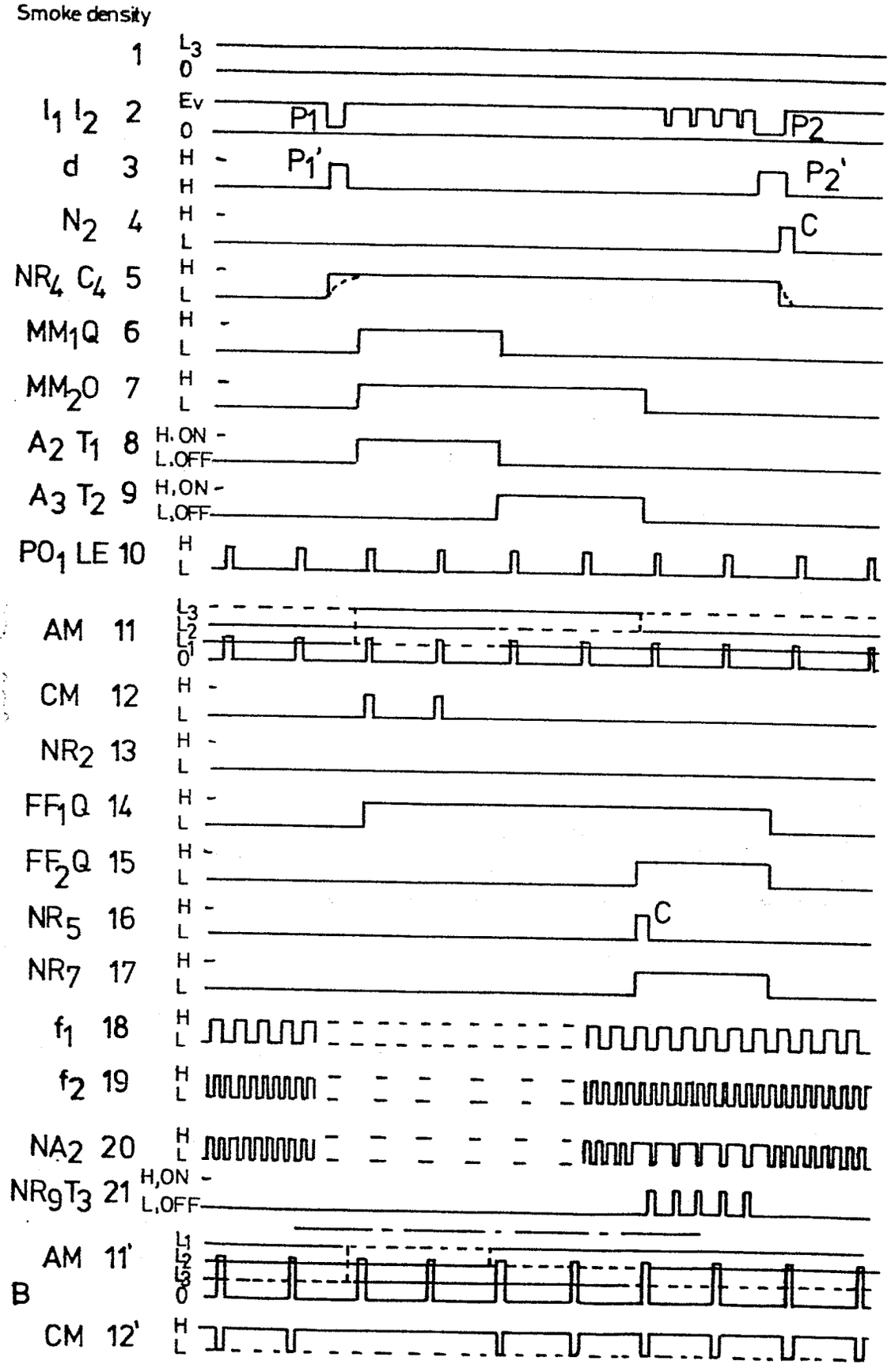
Smoke density
1 L3 0
I1 I2 2 Ev 0 P1 P2
d 3 H H P1' P2'
N2 4 H L C
NR4 C4 5 H L
MM1Q 6 H L
MM2O 7 H L
A2 T1 8 H,ON L,OFF
A3 T2 9 H,ON L,OFF
PO1 LE 10 H L
AM 11 L3 L2 L1 0
CM 12 H L
NR2 13 H L
FF1Q 14 H L
FF2Q 15 H L
NR5 16 H L C
NR7 17 H L
f1 18 H L
f2 19 H L
NA2 20 H L
NR9T3 21 H,ON L,OFF
AM 11' L1 L2 L3 0
B
CM 12' H L

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Figure 5

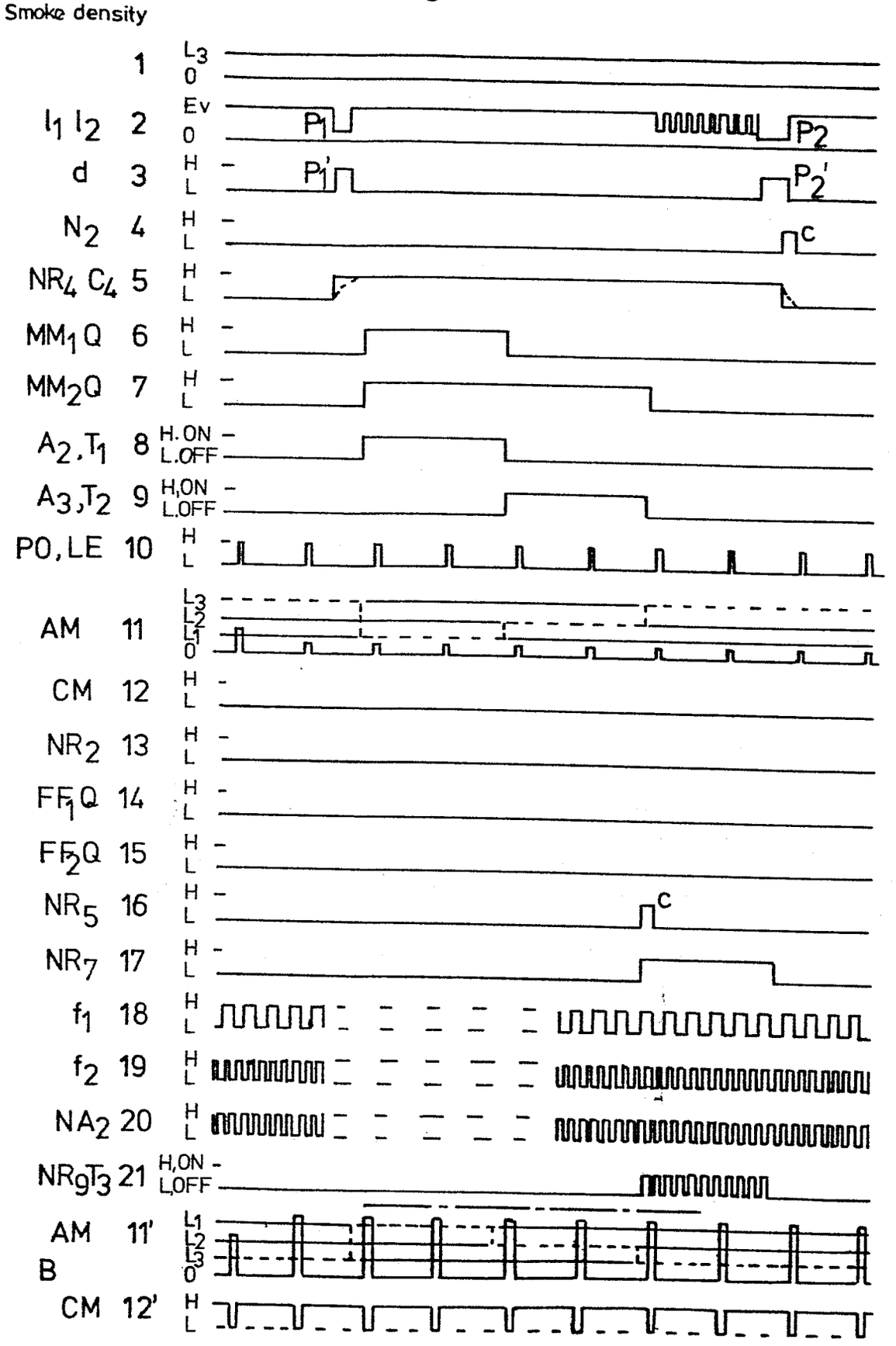
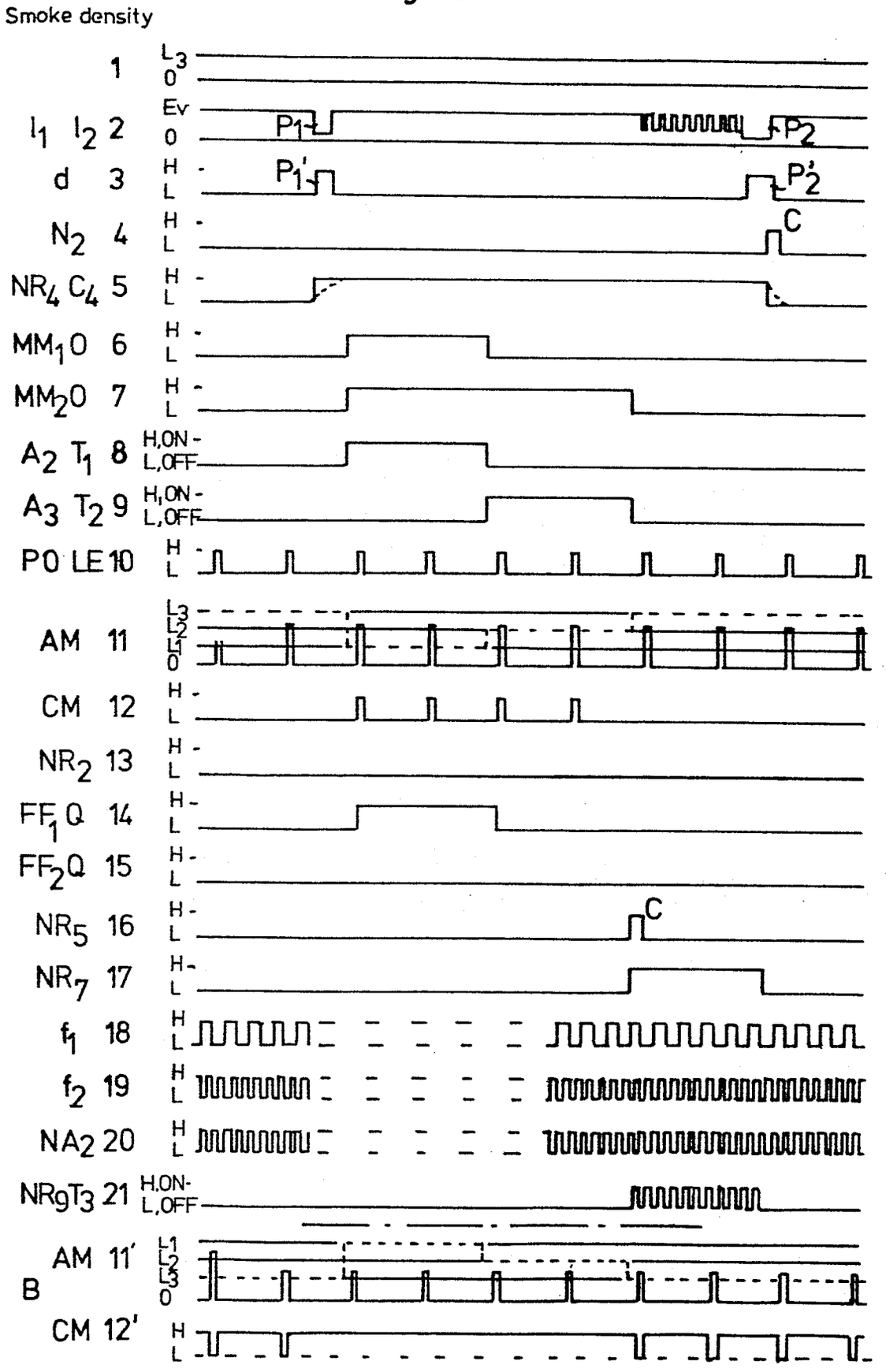

Smoke density
1
I_1 I_2 2
d 3
N_2 4
NR_4 C_4 5
MM_1Q 6
MM_2Q 7
A_2, T_1 8
A_3, T_2 9
PO, LE 10
AM 11
CM 12
NR_2 13
FF_1Q 14
FF_2Q 15
NR_5 16
NR_7 17
f_1 18
f_2 19
NA_2 20
NR_9T_3 21
AM 11'
B
CM 12'
L_3
L_2
L_1
0
Ev
H
L
H.ON
L.OFF
H,ON
L.OFF
P_1
P_2
P_1'
P_2'
C

Figure 6


Smoke density
1
I_1 I_2 2
d 3
N_2 4
NR_4 C_4 5
MM_1O 6
MM_2O 7
A_2 T_1 8
A_3 T_2 9
PO LE 10
AM 11
CM 12
NR_2 13
FF_1 Q 14
FF_2 Q 15
NR_5 16
NR_7 17
f_1 18
f_2 19
NA_2 20
NR_9T_3 21
AM 11'
B
CM 12'
L_3
L_2
L_1
0
Ev
H
L
H,ON
L,OFF
P_1
P_2
P_1'
P_2'
C

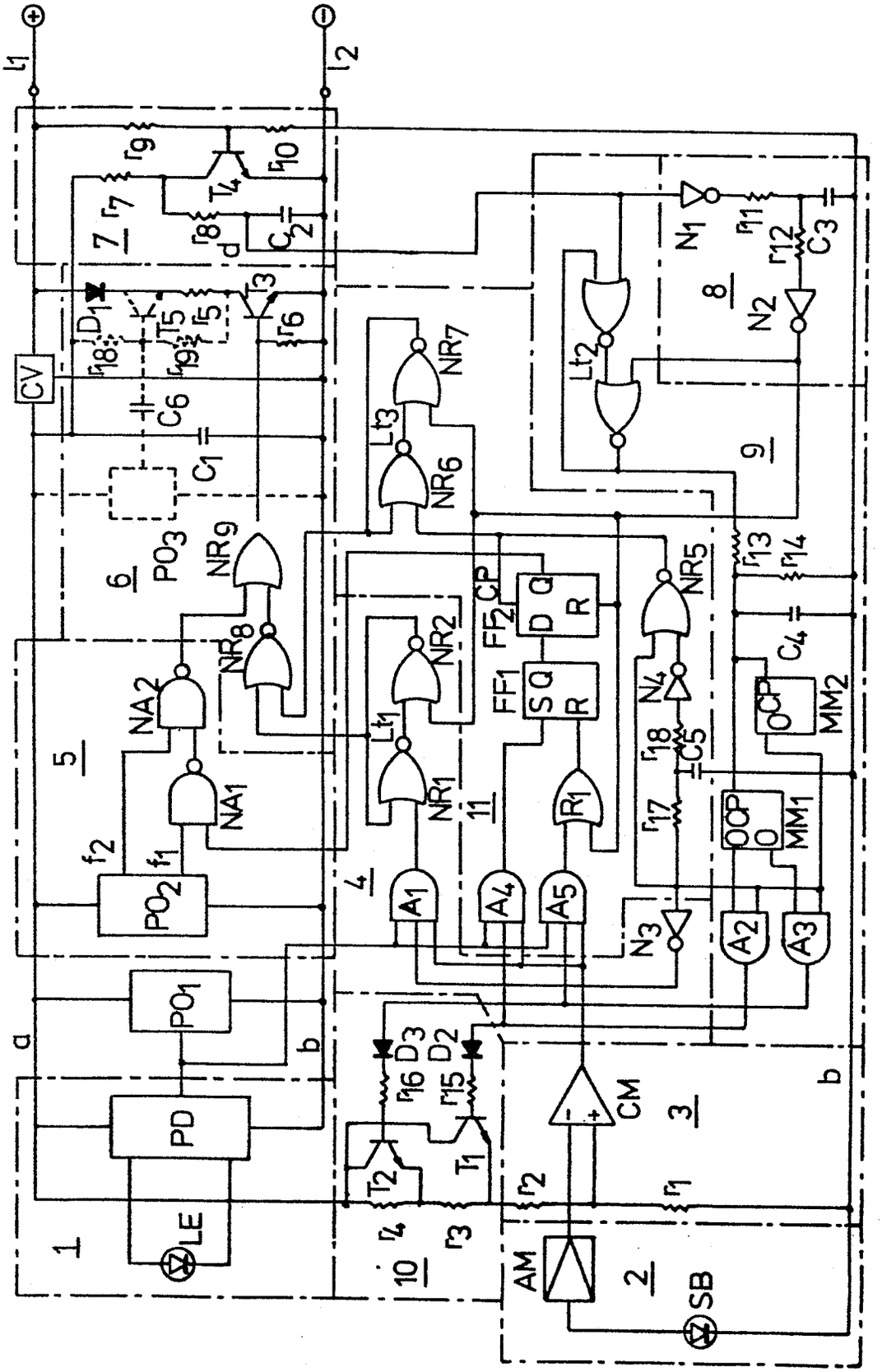

l1
l2
CV
PD
LE
SB
AM
CM
PO1
PO2
PO3
NA1
NA2
NR1
NR2
NR5
NR6
NR7
NR8
NR9
FF1
FF2
A1
A2
A3
A4
A5
R1
N1
N2
N3
N4
MM1
MM2
OCP
CP
D
Q
R
S
T1
T2
T3
T4
T5
D1
D2
D3
C1
C2
C3
C4
C5
C6
r1
r2
r3
r4
r5
r6
r7
r8
r9
r10
r11
r12
r13
r14
r15
r16
r17
r18
r19
Lt1
Lt2
Lt3
1
2
3
4
5
6
7
8
9
10
11

Figure 7

0122432

European Patent Office

EUROPEAN SEARCH REPORT

Application number

EP 84102465.6

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
A	EP - A2 - 0 067 339 (SIEMENS) * Page 1, line 1 - page 2, line 5 *	1	G 08 B 17/10 G 08 B 29/00
A	US - A - 4 374 329 (SCHOENFELDER et al.) * Column 1, lines 5-31; column 7, line 35 - column 9, line 18; fig. 8-11 *	1	
A	US - A - 4 306 230 (FORSS et al.) * Column 2, line 33 - column 3, line 16; fig. 1-3 *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl. ³)

G 08 B 17/00
G 08 B 29/00
G 08 B 26/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	10-07-1984	HAJOS

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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