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(54) **Time measuring circuit.**

(57) A time measuring circuit for meters of the pulse reflection type includes a gate signal generator (3) for producing a gate pulse signal (D) the duration of which is proportional to a value of an object to be measured, an oscillator (1) for producing clock pulses at a predetermined frequency, a complementary-output element (2, 200) responsive to the gate pulse signal for producing first and second clock pulses (G, H) which are the same at their phase and relatively inverted, a pair of gates (4, 5) for passing therethrough the first and second clock pulses during appearance of the gate pulse signal, a flip-flop (6) for applying the first clock pulses to a counter (7) and for applying the first and second clock pulses to a pair of integration circuits (11, 12). The counter (7) counts the first clock pulses (G) to produce an output signal indicative of the counted value, and the integration circuits (11, 12) selectively integrate the first and second clock pulses (G, H) in response to the gate pulse signal. An analog-to-digital converter (13) is connected to the integration circuits to convert the finally integrated value into a digital value, and a computer (14) is arranged to calculate a sum of the counted value and the digital value.

EP 0 122 984 A1

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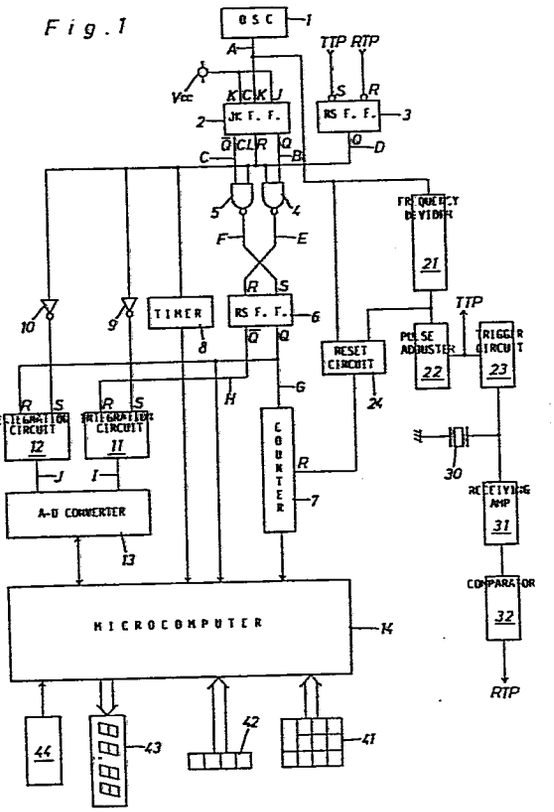
Fig. 1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24
PULSE ADJUSTER
22
TRIGGER CIRCUIT
23
TTP
H
G
INTEGRATED CIRCUIT
12
INTEGRATED CIRCUIT
11
COUNTER
7
R
J
I
30
A-D CONVERTER
13
RECEIVING AMP
31
COMPARATOR
32
RTP
MICROCOMPUTER
14
44
43
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41

TIME MEASURING CIRCUIT.

The present invention relates to a time measuring circuit for meters of the pulse reflection type such as an ultrasonic axial force meter, an ultrasonic thickness meter or the like.

For accurate measurement of a distance by using light, an axial force of a bolt or a thickness of an object by using ultrasonic waves, it is required to measure a time of approximately 1 nS or a frequency of approximately 1 GHz with an error less than one percent. To effect such accurate measurement, an expensive high speed counter has been utilized heretofore, resulting in provision of a special and complicated circuits for the counter.

It is, therefore, a primary object of the present invention to provide an improved time measuring circuit which is capable of effecting accurate measurement of a time of substantially 1 nS without provision of a high speed counter.

According to the present invention there is provided a time measuring circuit for meters of the pulse reflection type which includes a pulse oscillator means for applying a transmission pulse signal to an object to be measured, a receiving amplifier for receiving an echo pulse signal reflected from the object, a gate signal generator connected to receive the transmission pulse signal from the oscillator means and the echo pulse signal from the amplifier so as to produce a gate pulse signal the duration of which is proportional to a value of the

object to be measured, first means for producing first and second output pulses at a predetermined frequency during appearance of the gate pulse signal, second means for measuring a value of the first output pulses from the first means and for producing an output signal indicative of the measured value, third means responsive to the first and second output pulses from the first means for converting the duration of the gate pulse signal into the corresponding voltage value, fourth means for converting the finally converted voltage value into a digital value and for producing an output signal indicative of the digital value, and a measuring means for measuring a sum of the measured value and the digital value in response to the output signals from the second and fourth means.

In the actual practices of the present invention, it is preferable that the first means comprises an oscillator for producing clock pulses at a predetermined frequency, a complementary-output element responsive to the gate pulse signal from the gate signal generator for producing first and second clock pulses which are the same at their phase and relatively inverted, gate means responsive to the gate pulse signal from the gate signal generator for passing therethrough the first and second clock pulses during appearance of the gate pulse signal, and a flip-flop for applying the first clock pulses to the second means and for applying the first and second clock pulses to the third means.

It is also preferable that the second means is in the form of a counter connected to the flip-flop to count the first clock pulses, the third means is in the form of a pair of integration circuits connected to the flip-flop to selectively integrate the first and second clock pulses in response to the gate pulse signal, and the fourth means is in the form of an analog-to-digital converter connected to the integration circuits to convert the finally integrated value into a digital value.

For a better understanding of the present invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in which:-

Fig. 1 is a schematic block diagram of a time measuring circuit in accordance with the present invention;

Figs. 2 and 3 illustrate waveforms appearing at various points in the circuit diagram of Fig. 1;

Fig. 4 is a schematic block diagram of a modification of the time measuring circuit of Fig. 1; and

Fig. 5 illustrates waveforms appearing at various points in the circuit diagram of Fig. 4.

Referring now to the drawings, Fig. 1 illustrates a time measuring circuit adapted to an ultrasonic axial force meter of the pulse reflection type. The time measuring circuit includes a crystal oscillator 1 for producing clock pulses A in the form of rectangular waves at a frequency of 100 KHz - 10 MHz, and a JK flip-flop 2 connected at its clock terminal CK to the output terminal of oscillator 1 and at its other input terminals J and K to a DC voltage source Vcc. The time measuring circuit further includes an RS flip-flop 3 which is applied at its set terminal S with a transmission pulse signal TTP from the ultrasonic axial force meter and at its reset terminal R with a reflection echo pulse RTP from the axial force meter. RS flip-flop 3 is connected at its output terminal Q to a clear input terminal CLR of flip-flop 2, each first input terminal of NAND gates 4 and 5, and the input terminal of a timer 8. The output terminal Q of RS flip-flop 3 is further connected to each set terminal S of first and second integration circuits 11 and 12 respectively through inverters 9 and 10. NAND-gates 4 and 5 are connected at their second input terminals to output terminals Q and $\overline{Q}$ of JK flip-flop 2 and at their output terminals to reset and set terminals R and S of a second flip-flop 6 respectively.

A first output terminal Q of RS flip-flop 6 is connected to the input terminal of a counter 7, a micro-

computer 14 and a reset terminal R of the second integration circuit 12, while a second output terminal $\overline{Q}$ of RS flip-flop 6 is connected to a reset terminal R of the first integration circuit 11. Each output terminal of integration circuits 11 and 12 is connected to an analog-to-digital or A-D converter 13. The microcomputer 14 is commercially available the interface of which is connected at its input terminals to respective output terminals of counter 7, timer 8 and A-D converter 13.

The ultrasonic axial force meter includes a frequency divider 21 in the form of a counter for dividing the frequency of the clock pulses A from oscillator 1, and a pulse width adjustor 22 in the form of a one-shot circuit or a differentiation circuit for forming rectangular impulse waves from the divided clock pulses. The rectangular impulse waves are transmitted to a trigger circuit 23 and also transmitted as the transmission pulse signal TTP to RS flip-flop 3. The ultrasonic axial force meter further includes a probe 30 connected to trigger circuit 23 for producing an ultrasonic pulse wave, which is transmitted to an object to be measured, a receiving amplifier 31 for receiving an echo pulse train output from probe 30, and a comparator 32 for comparing an output of the amplifier 31 with a predetermined value to produce the reflection echo pulse RTP. Furthermore, the ultrasonic axial force meter includes a reset circuit 24 connected to a reset terminal R of counter 7 and responsive to the divided clock pulses from frequency divider 21 for producing a reset signal in accordance with the clock pulses from oscillator 1, a ten-key board 41 for applying an input signal indicative of a constant of the object such as a bolt to the computer 14, a select-key board 42 for selecting input data for the computer 14, an indicator 43 for indicating a value measured by the computer 14, and a thermometer 44 for measuring a temperature of the object and the ambient temperature.

In operation, as is illustrated in Fig. 2,

RS flip-flop 3 is set in response to the transmission pulse signal TTP to produce a gate signal D at a high level and is reset in response to the reflection echo pulse RTP to make the gate signal low level. The duration of gate signal D is proportional, for instance, to an axial length of the bolt to be measured. When received the high level gate signal D, JK flip-flop 2 divides clock pulses A from oscillator 1 to produce at its terminals Q and $\overline{Q}$ output signals B, C in the form of rectangular waves which are relatively inverted at half the frequency of the clock pulses. When the level of gate signal D becomes low, the output signal B from terminal Q is maintained at a high level, while the output signal C from terminal $\overline{Q}$ is maintained at a low level. NAND gates 4 and 5 are responsive to the high level gate signal D to permit the output signals B and C applied to the second RS flip-flop 6 from JK flip-flop 2. When the level of gate signal D becomes low, the timer 8 produces a high level signal therefrom after lapse of a time t, and the computer 14 is responsive to the high level signal from timer 8 to receive output signals from counter 7 and A-D converter 13, as is described in detail later.

As is illustrated in Fig. 3, each wave form of the output signals E and F from NAND gates 4 and 5 is relatively inverted during appearance of the high level gate signal D. When the level of gate signal D becomes low, the output signals E and F are maintained at a high level respectively. Thus, the second RS flip-flop 6 is applied at its terminals S and R with the relatively inverted output signals E and F to produce relatively inverted output signals G and H at its terminals Q and $\overline{Q}$. Upon disappearance of the high level gate signal D, the second RS flip-flop 6 acts to memorize each level of the output signals E and F.

If the level of gate signal D becomes low when the output signal B from JK flip-flop 2 is at a low level, the high level output signal G from RS flip-flop 6 is applied as an input signal to the counter 7, as is illus-

trated in (a) of Fig. 3. If the level of gate signal D becomes low when the output signal B from JK flip-flop 2 is at a high level, the low level output signal G from RS flip-flop 6 is applied as an input signal to the counter 7, as is illustrated in (b) of Fig. 3. As a result, the counter 7 acts to count the output signal G from RS flip-flop 6 thereby to measure a time $T_1$. Simultaneously, the coumputer 14 is responsive to the output signal G from RS flip-flop 6 to discriminate the operation of integration circuit 11 or 12 so as to produce an output signal therefrom for activation of A-D converter 13.

When applied with the high level output signal G from RS flip-flop 6, the first integration circuit 11 operates to produce an output signal I in the form of saw tooth waves. In this instance, A-D converter 13 is responsive to the output signal from computer 14 to convert the final voltage level of output signal I into a digital value indicative of a time $T_2$. In the case that the full scale of each saw tooth wave of signal I represents a time defined by one-fourth the frequency of the clock pulses, the time $T_2$ is measured by a digital value converted from the final saw tooth wave of signal I. When applied with the low level output signal G from RS flip-flop 6, as is illustrated in (b) of Fig. 3, the second integration circuit 12 operates to produce an output signal J in the form of saw tooth waves. In this instance, A-D converter 13 is responsive to the output signal from computer 14 to convert the final voltage level of output signal J into a digital value indicative of a time $T_3$.

In such operation as described above, each of integration circuits 11 and 12 starts to integrate the high level input signal G or H applied to its reset terminal R during appearance of the high level gate signal D and discharges when the level of the input signal becomes low. When the level of gate signal D becomes low, each of integration circuits 11 and 12 acts to hold therein

the finally integrated voltage, and subsequently A-D converter 13 is activated in response to the output signal from computer 14 to convert the integrated voltage into the digital value and produces an output signal indicative of the digital value upon completion of the voltage conversion. When applied with the output signal from A-D converter 13, the computer 14 receives an output signal from counter 7 to measure a sum of the time $T_1$ and the time $T_2$ and/or $T_3$, and the counter 7 is reset by a reset signal from reset circuit 24.

In the case that the counter 7 is applied with the high level input signal G upon disappearance of the high level gate signal D, the time T is measured on a basis of the following equation:

$$T = T_1 + T_2$$

In the case that the counter 7 is applied with the low level input signal G upon disappearance of the high level gate signal D, the time T is measured on a basis of the following equation:

$$T = T_1 + T_2 + T_3$$

where the value of $T_2$ is determined in its full scale.

In Fig. 4 there is illustrated a modification of the time measuring circuit described above, in which JK flip-flop 2 in Fig. 1 is replaced with a complementary-output element 200, and the integration circuits 11 and 12 are replaced with a voltage generator 90, a selector 100 and a single integration circuit 110. The complementary-output element 200 is arranged to produce relatively inverted clock pulses A and $\overline{A}$ at the same phase in response to input clock pulses from oscillator 1. The voltage generator 90 is arranged to produce positive and negative voltage signals $+V_s$, $-V_s$ which are the same at their voltage levels and different at their polarity, the selector 100 is, for example, in the form of an analog switch which is connected to voltage generator 90 to produce a positive voltage signal $+V_s$ in response to the high level signal H from RS flip-flop 6 and to produce a negative voltage signal $-V_s$ in response to the high

level signal G from RS flip-flop 6, and the integration circuit 110 is arranged to charge in response to the positive voltage signal $+V_s$ and discharge in response to the negative voltage signal $-V_s$ thereby to produce an output signal $I_a$ in the form of triangular waves as is illustrated in Fig. 5. The other arrangements are substantially the same as those in the time measuring circuit of Fig. 1.

Having thus described the preferred embodiments of the invention it should be understood that numerous structural modifications and adaptations may be resorted to without departing from the spirit of the invention. For instance, it is noted that A-D converter 13 of the above embodiment may be replaced with a voltage-frequency converter with a counter.

Claims:

1. A time measuring circuit for meters of the pulse reflection type including a pulse oscillator means (1, 21, 22, 23) for applying a transmission pulse signal (TTP) to an object to be measured, a receiving amplifier (31) for receiving an echo pulse signal reflected from said object, a gate signal generator (3) connected to receive the transmission pulse signal from said oscillator means and the echo pulse signal from said amplifier so as to produce a gate pulse signal (D) the duration of which is proportional to a value of said object to be measured, and a measuring means for measuring the duration of the gate pulse signal, said time measuring circuit being characterised by;

first means (1, 2, 4, 5, 6) for producing first and second output pulses (G, H) at a predetermined frequency during appearance of the gate pulse signal;

second means (7) for measuring a value of the first output pulses (G) from said first means and for producing an output signal indicative of the measured value;

third means (11, 12) responsive to the first and second output pulses (G, H) from said first means for converting the duration of the gate pulse signal (D) into the corresponding voltage value (I, J); and

fourth means (13) for converting the finally converted voltage value into a digital value and for producing an output signal indicative of the digital value, and being characterised in that said measuring means (14) is arranged to measure a sum of the measured value and the digital value in response to the output signals from said second and fourth means.

2. A time measuring circuit as claimed in Claim 1, characterised in that said first means comprises:

an oscillator (1) for producing clock pulses at a predetermined frequency;

a complementary-output element ( 2, 200 ) responsive to the gate pulse signal from said gate signal generator for producing first and second clock pulses (G, H) which are the same at their phase and relatively inverted;

gate means (4, 5) responsive to the gate pulse signal from said gate signal generator for passing therethrough the first and second clock pulses during appearance of the gate pulse signal; and

a flip-flop (6) for applying the first clock pulses to said second means and for applying the first and second clock pulses to said third means.

3. A time measuring circuit as claimed in Claim 2, characterised in that said complementary-output element is in the form of a JK flip-flop (2) connected to receive the clock pulses (A) from said oscillator (1) and to produce first and second clock pulses (B, C) in response to the gate pulse signal (D) from said gate signal generator, and said gate means includes a pair of NAND gates (4, 5) connected to permit the first and second clock pulses (E, F) applied to said flip-flop from said JK flip-flop in response to the gate pulse signal from said gate signal generator.

4. A time measuring circuit as claimed in Claim 2, characterised in that said second means is in the form of a counter (7) connected to said flip-flop (6) to count the first clock pulses (G), said third means is in the form of a pair of integration circuits (11, 12) connected to said flip-flop to selectively integrate the first and second clock pulses (G, H) in response to the gate pulse signal from said gate signal generator, and said fourth means is in the form of an analog-to-digital converter (13) connected to said integration circuits to convert the finally integrated value into a digital value.

5. A time measuring circuit as claimed in Claim 2, characterised in that said third means includes a voltage generator (90) for generating positive and negative voltage signals which are the same at their voltage levels

and different at their polarity, a selector means (100) connected to said voltage generator for producing a positive voltage signal in response to the first clock pulses from said flip-flop and producing a negative voltage signal in response to the second clock pulses from said flip-flop, and an integration circuit (110) connected to said selector means to charge in response to the positive voltage signal from said selector means and discharge in response to the negative voltage signal from said selector means.

6. A time measuring circuit as claimed in Claim 4, characterised in that said measuring means is in the form of a microcomputer (14) arranged to calculate a sum of the counted value of the first clock pulses and the digital value from said analog-to-digital converter.

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Fig. 1

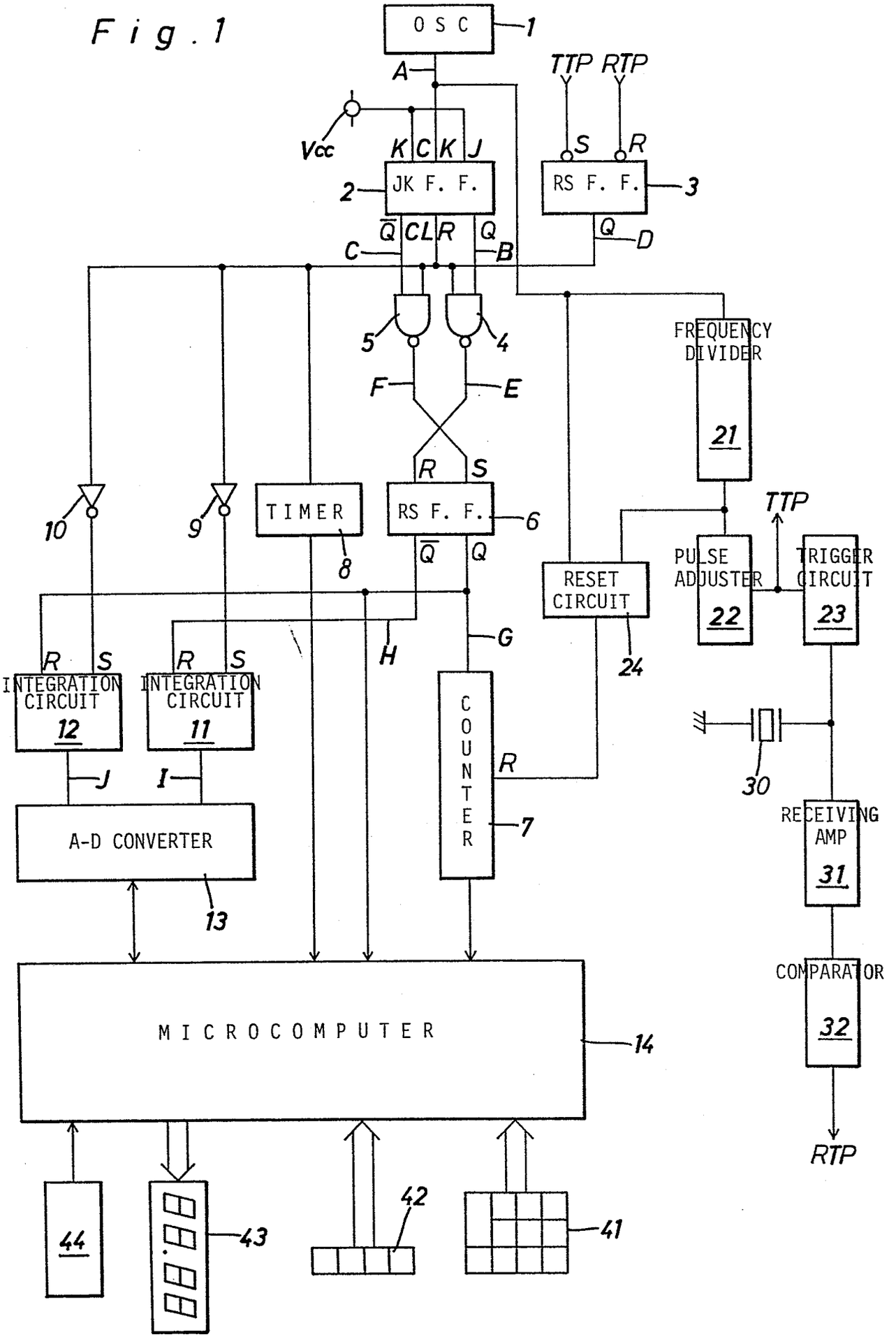


Fig. 2

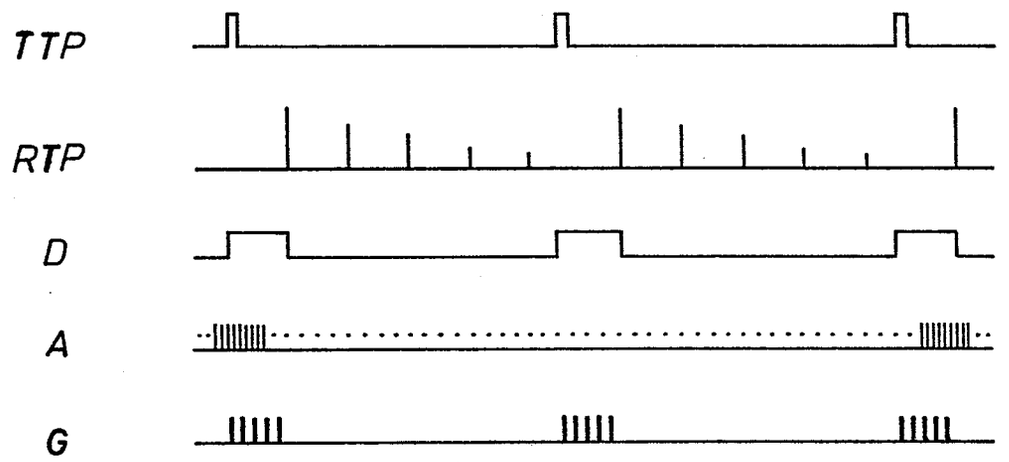



Fig. 3

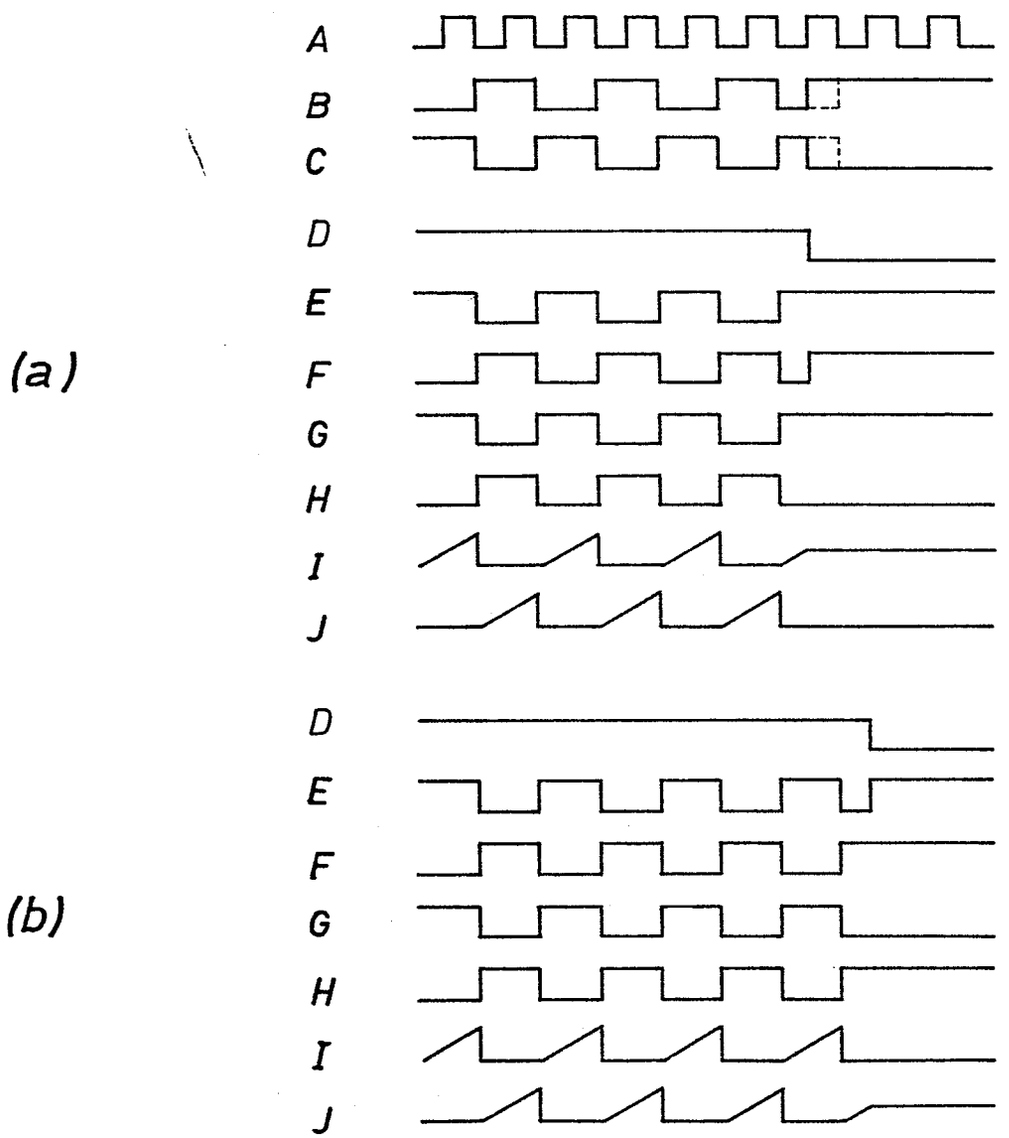
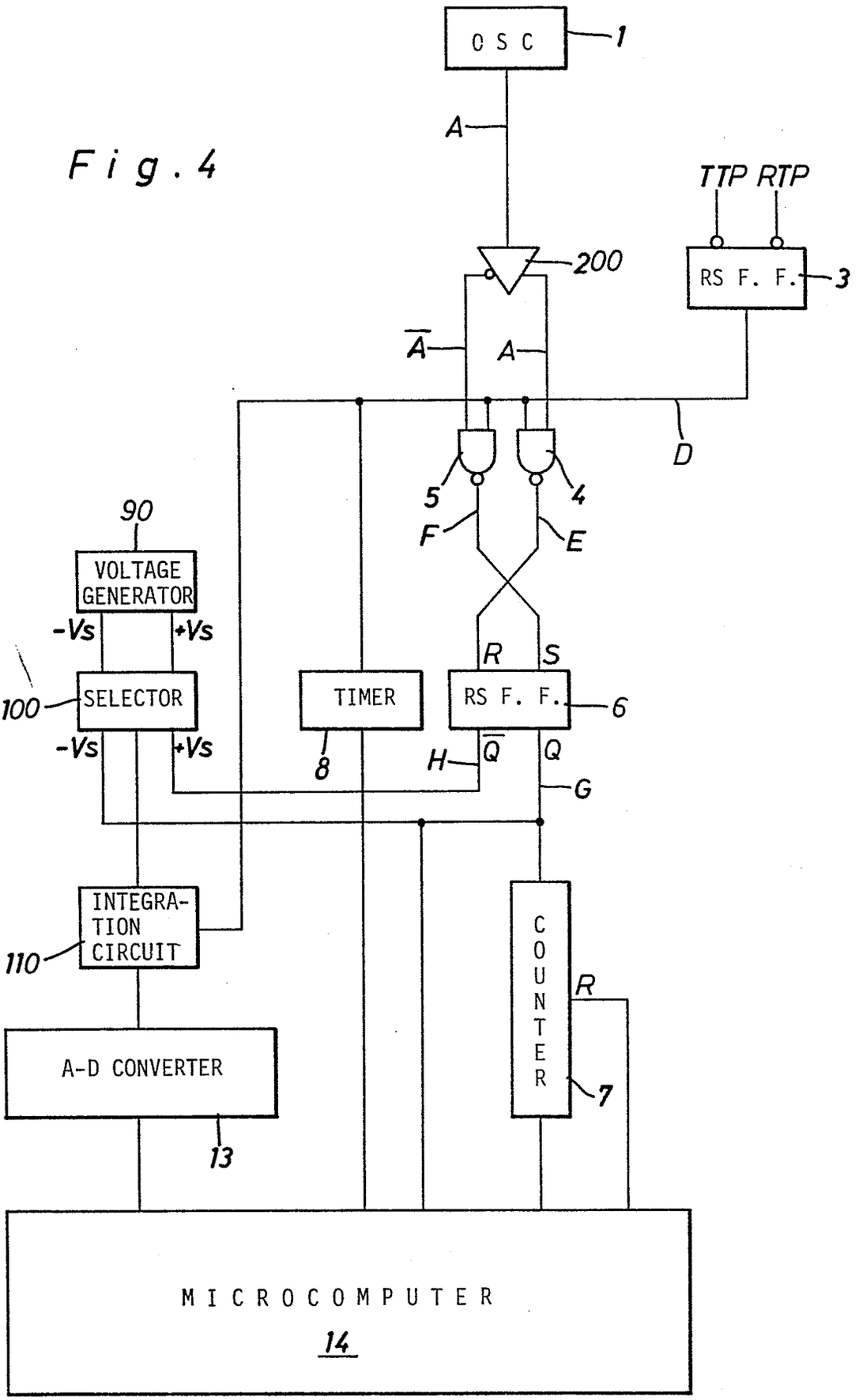


Fig. 4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VOLTAGE GENERATOR
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COUNTER
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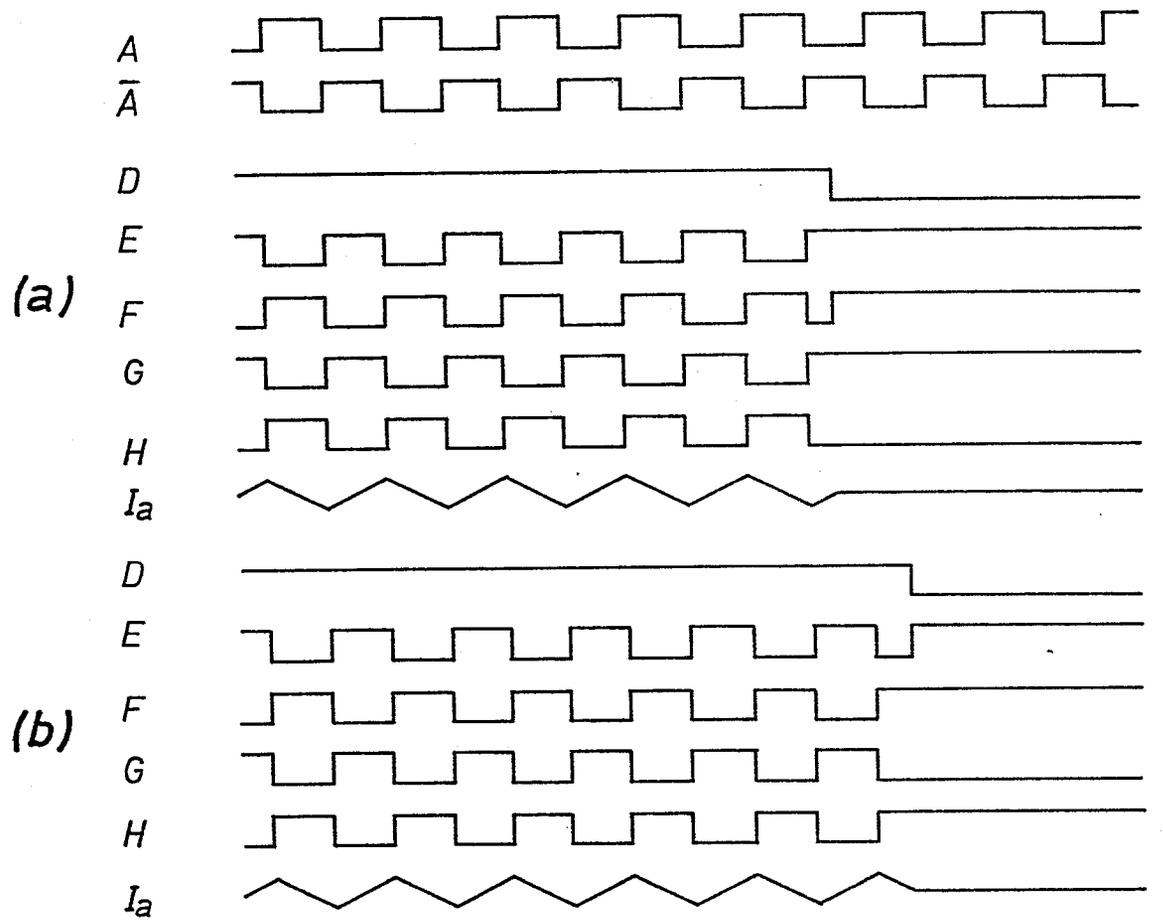
7
A-D CONVERTER
13
MICROCOMPUTER
14

Fig.5



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# EUROPEAN SEARCH REPORT

0122984
Application number

EP 83 30 2263

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl. ³) |
|---|---|---|---|
| X,Y | IBM TECHNICAL DISCLOSURE BULLETIN, vol. 4, no. 5, October 1961, New York (US) J. DIAZ:"Radar pulse measuring", page 27 * Figure * | 1,4,5 | G 04 F 10/00 |
| Y | IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, vol. IM-21, no. 4, November 1972 R.A. BENSON et al.:"The folded ramp: A new technique for computer-controlled time-interval measurement", pages 409-412 * Figure 1 * | 1,3-5 | |
| A | US-A-4 112 358 (H. ASHIDA) * Figures 4-6 * | 1 | |

TECHNICAL FIELDS SEARCHED (Int. Cl. ³)

G 04 F

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 12-12-1983 | EXELMANS U.G.J.R. |

CATEGORY OF CITED DOCUMENTS

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