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(54) Register control system for a printing press.

(57) Optical scanners (18, 19) mount to a press (1 to 8) and provide information to a register control system (15, 16, 17, 20) which automatically maintains color-to-color register. The same information is processed to provide signals to a scanner interface circuit (17) which controls the position of the optical scanners (18, 19) to insure that they track the register patterns on the moving web (6).

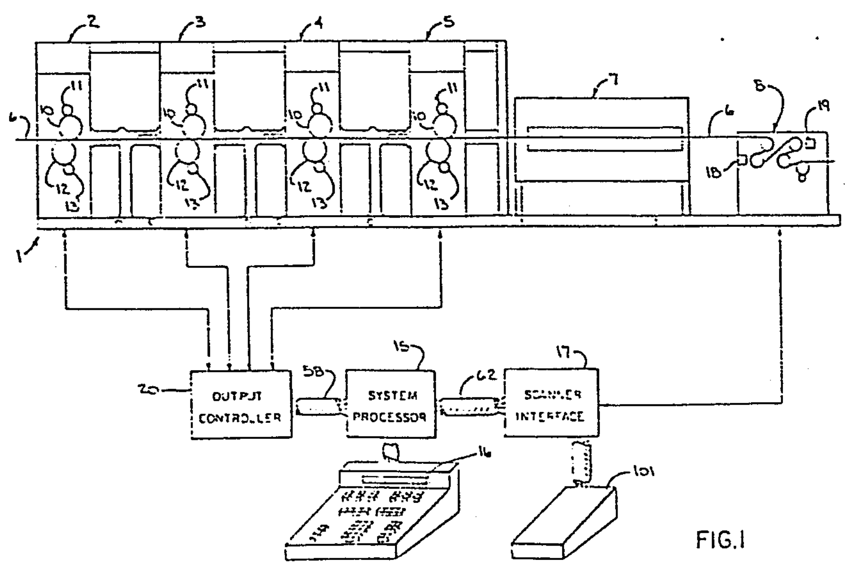


FIG.1

Croydon Printing Company Ltd

Register control system for a printing press

The field of the invention is control systems for adjusting the color-to-color register on web offset presses, gravure presses and flexographic presses.

In both processes a web of material to be printed is driven through a series of cylinders which separately print an image on the web using inks of selected colors. The rotational and lateral position of each print cylinder is precisely aligned such that the register of the separate colors is maintained to provide an accurate and clear print image.

Numerous types of register control systems are employed in the art to maintain color-to-color register under a variety of operating conditions. These control systems are in most cases open loop systems in which an operator periodically examines the print image and manually enters correction values to adjust the lateral or rotational alignments of one or more print cylinders.

Closed loop register control systems have been employed on gravure printing presses. In such control systems a series of register marks is printed by each print cylinder and an optical detector is positioned after each print cylinder to detect these marks. The timing of the electrical pulses produced by the optical detector and the duration of each pulse provide position feedback information indicative of the rotational and lateral alignment of the print cylinder with respect to the framework of the press. This position feedback information is employed to automatically adjust the register of the print cylinder with respect to the press framework.

Prior closed loop register control systems have not been used on offset presses. The web on offset presses is not mechanically constrained after passing over each print cylinder, and as a result, an optical detector cannot accurately read a register mark. Instead, such measurements must be made at the output of the press after all colors have been printed and the ink dried.

The present invention relates to a closed loop register control system in which a single optical scanner is employed to provide position feedback information that indicates the relative register of each print cylinder with respect to a designated reference print cylinder. Each print cylinder produces a specific register mark which forms part of a register pattern. The feedback signal produced by the optical scanner as it reads the register pattern is analyzed to determine the lateral and rotational register of each print cylinder with respect to the reference print cylinder. Register error signals are thus produced for each print cylinder and are employed to control motors that adjust the position of each.

A general object of the invention is to provide a closed loop register control system for an offset printing press. A single optical scanner may be employed and it is positioned at the output of the press where the moving web can be properly constrained to allow accurate detection of the register pattern.

Another object of the invention is to provide an accurate register control system. By measuring the relative register of each print cylinder with respect to the reference print cylinder rather than a timing signal related to press position, mechanical inaccuracies in the press gear train are eliminated.

Yet another object of the invention is to provide an accurate indication of register error which is not subject to spurious deviations. Each signature which is output by the press contains a register pattern and thus discrete position feedback signals are generated at a high rate. Spurious position feedback signals are eliminated in a first analysis which rejects position feedback signals that indicate extraordinary register errors. The position error signal used for control purposes is obtained by averaging a series of acceptable readings.

A more specific object of the invention is to enable the register control system to be easily configured to any press. The set-up procedure is an interactive process in which the operator is prompted to enter the required data. Such data includes offset data for each color print cylinder to account for printing errors in the register pattern. The print cylinder which is to be used as the reference color is also identified during set-up.

The foregoing and other objects and advantages of the invention will appear from the following description. In the description, reference is made to the accompanying drawings which form a part thereof, and in which there is shown by way of illustration a preferred embodiment of the invention. Such embodiment does not necessarily represent the full scope of the invention, however, and reference is made therefore to the claims herein for interpreting the scope of the invention.

F I G . 1 is a schematic drawing of a printing press which employs the register control system of the present invention;

F I G . 2A to 2C are electrical schematic diagrams of the system processor which forms part of the system of Fig. 1;

F I G . 3 is an electrical schematic diagram of the scanner interface which forms part of the system of Fig. 1;

F I G . 4A and 4B are electrical schematic diagrams of the output controller which forms part of the system of Fig. 1;

F I G . 5 is a partial elevation view of an optical scanner which forms part of the system of Fig. 1;

F I G . 6 is a schematic representation of the register pattern and corresponding electrical signals which appear in the register control system;

F I G . 7A to 7D are schematic representations of register patterns illustrating types of misregister;

F I G . 8 is a general flow chart of the manner in which the system processor of Fig. 2 operates;

F I G . 9A to C are flow charts of interrupt service routines executed by the system processor of Fig. 2;

F I G . 10 is a flow chart of an interrupt service routine executed by the system processor of Fig. 2;

F I G . 11A to B are schematic representations of a portion of a register pattern;

F I G . 12 is a flow chart of the register error calculation routine executed by the system processor of Fig. 2;

F I G . 13 is a portion of a register pattern; and

F I G . 14 is a flowchart of programs executed by the system processor of Fig. 2.

Referring particularly to Fig. 1, the present invention is applied to a web offset printing press 1 which includes four blanket-to-blanket printing units 2 to 5. A web 6 is fed through the successive printing units 2 to 5 from a reel stand (not shown in the drawings) and it is then fed through a dryer unit 7 and a chill unit 8. The printed web 6 may then be guided through coating equipment (not shown) and folding equipment (not shown) which fold and separate the web into individual signatures.

Each printing unit 2 to 5 includes an upper printing couple comprised of an upper blanket cylinder 10 and upper plate cylinder 11, and a lower printing couple comprised of a lower blanket cylinder 12 and lower plate cylinder 13. In a typical multicolor printing operation the printing unit 2 prints the color black on the top and bottom surfaces of the web 6, and subsequent printing units 3 to 5 print other colors on both surfaces of the web 6. Both the lateral and rotational position of the upper plate cylinders 11 and lower plate cylinders 13 are separately controlled by electric motors to precisely register the separate color images.

In prior presses which employ the offset lithography process register of the various colors is maintained manually. The pressman examines signatures at the output of the press and enters lateral and rotational offset values into a register control system which operates the proper electric motor. The maintenance of color register in such systems requires the constant attention of the pressman during a typical run, since register is often lost due to a number of uncontrollable variables in the web material and the press hardware.

The present invention is a register control system which automatically controls the register of the four printing units 2 to 5. It will become evident that while a four unit, single web, offset lithography printing press is shown and described in this specification, that the present invention is applicable to other presses.

Referring still to Fig. 1, the register control system includes a centrally located system processor 15 which is operated from a main control panel 16. Information regarding the register of the four printing units 2 to 5 is received by the system processor 15 from a scanner interface 17, which in turn connects to a pair of optical scanner units 18 and 19 mounted in the chill unit 8. Based on the register information received from the scanner interface 17, the system processor 15 operates an output controller 20. The output controller 20 operates in response to commands from the system processor 15 to separately operate the motors which control the lateral and rotational alignment of the upper plate cylinder 11 and lower plate cylinder 13 in each of the four printing units 2 to 5. A closed loop register control system is thus formed.

Referring particularly to Figs. 1 and 5, the optical scanners 18 and 19 are slidably mounted to the frame of the chill unit 8 with one scanner 18 directed at the bottom surface of the web 6 and the other scanner 19 directed at the top surface. The scanners 18 and 19 may be mounted on other "downstream" equipment which provides good web support. The scanners 18 and 19 produce signals on lines 24 which are proportional in amplitude to the light reflected from the surface of the web 6. Each scanner includes a lens which focuses on a small area of the web 6 and the scanners 18 and 19 are positioned to sense a register pattern 25 which is repeatedly printed along one edge of the web 6 by the printing units 2 to 5. The scanners 18 and 19 are mounted to read the register pattern 25 as the supporting web 6 passes over a chill roller. As a result, the pattern 25 is relatively stable and an accurate reading of register can be obtained.

The signal generated by each scanner 18 and 19 not only contains color register information, but also, information which indicates when the register pattern 25 has shifted laterally to the left or right of the focal point of the scanner. As shown in Fig. 5, the scanner 18 is mounted for translation along a slide 26 when a worm gear 27 is rotated by a scanner motor 28. The motor 28 is energized when a power relay 29 is energized and the direction of travel is determined by the state of a direction relay 30. One of the functions of the register control system of the present invention is to operate the power relay 29 and direction relay 30 for each optical scanner 18 and 19 to maintain their focal points near the center of the register patterns 25 which pass beneath. Thus the scanners 18 and 19 will "track" the register patterns 25 as the web 6 shifts laterally in the press.

Referring particularly to Fig. 2A, the system processor 15 is structured about an 8-bit microprocessor 35 which couples to an 8-bit bi-directional data bus 36 and a 16-bit address bus 37. During a read or write cycle, a least significant byte of address data is output to a latch 38 when an ALE control line is active, and immediately thereafter the least significant byte of address data is output to an address latch 39. Data is either read from the data bus 36 through a set of bi-directional data gates 40 or output through the data gates 40 to an addressed device coupled to the data bus 36. The direction of data flow through the gates 40 is determined by the microprocessor control lines, RD and INTA, which connect to a NAND gate 41 through a set of buffers 42. These two control lines along with the remaining microprocessor control lines (CLKOUT, WR, IO/M, RSTϕ) form a control bus 43 which connects to a number of system elements.

A random access, read/write memory (RAM) 44 connects to the address bus 37 and data bus 36. As will be explained in more detail hereinafter, the RAM 44 stores a variety of data structures which are employed by the register control system and which may be separately read into the microprocessor 35 for processing or which may be altered by a write operation. A chip select control line 45 enables the RAM 44 and a memory write control line 46 determines whether a read or write operation is performed. The processor 15 also includes a read-only memory (ROM)47 which stores machine language program instructions and constants. The ROM 47 is enabled when a chip select control line 48 is active and addressed data is read therefrom when a memory read control line 49 is active. The program instructions which direct the operation of the microprocessor 35 are sequentially read from the ROM 47 and executed to control the operation of the system processor 15.

A decoder circuit 50 connects to the address bus 37 and control bus 43. The decoder circuit 50 includes 2-to-4 and 3-to-8 decoder circuits along with associated gates which generate chip select signals to the various system elements. These include the RAM control line 45 and ROM control line 48 which are enabled when an address whithin their range appears on the address bus 37.

Referring still to Fig. 2A, an interrupt controller circuit 51 connects to the data bus 36 and control bus 43. The interrupt controller 51 accepts interrupt requests generated on four lines INTϕ, INT3, INT4 and INT7, determines which request has the highest priority, determines whether the incoming request has a higher priority than the process currently being serviced, and issues an interrupt through INT control line 52 to the microprocessor 35 based on this determination. An 8259 programmable interrupt controller manufactured by Intel Corporation is employed and it is enabled to receive control data from the data bus 36 by a control line 53 which is driven by the decoder circuit 50.

A universal asynchronous receiver/transmitter (UART) 54 generates one of the interrupt requests (INTϕ) whenever it receives or transmits a character. The UART 54 connects to the data bus 36 and it is enabled through a control line 55. A character may be output through the UART 54 for transmission through a serial output circuit 56 or a character may be input serially through input circuit 57 and read from the UART 54. The circuits 56 and 57 interface the UART 54 to a serial data link 58 which connects to the output controller 20. The UART 54 serves as the means for outputting control data over a substantial distance, and the system processor 15 may thus be centrally located while the output controller 20 may be located adjacent the printing press 1.

Referring particularly to Figs. 2A and 2B, the system processor 15 includes an arithmetic processor 60 for performing high speed arithmetic functions. The processor 60 is enabled by the decoder circuit 50 through a control line 61 and data may be written to it for processing. A 9511A processor manufactured by Advanced Devices, Inc. is employed, and when an answer is ready, the processor 60 generates an interrupt request to the interrupt controller 51 through the INT3 control line. When the interrupt is serviced by the microprocessor 35, it is vectored to a service routine which directs the microprocessor 35 to read the arithmetic result from the arithmetic processor 60 and set a flag in RAM 44 which indicates that the arithmetic processor is available for further computations.

Referring particularly to Figs. 1 and 2B, the system processor 15 receives data from the scanner interface 17 and outputs data to the scanner interface 17 through a parallel I/O bus 62. Four bits of output data are stored in a latch 63 when a chip select control line 64 is driven low by the decoder circuit 50. This 4-bit nibble is coupled through resistors 65 to corresponding leads 66 to 69 in the I/O bus 62. As will be explained in more detail below, this data indicates if either of the optical scanners 18 or 19 are to be repositioned, and if so, in which direction.

Three bits of data are input from the scanner interface 17. Two of these are received at two inputs of a multiplexer 70. These two input signals 71 and 72 are digital representations of the signals generated by respective optical scanners 18 and 19 as the register patterns 25 pass beneath them. One of these two signals is selected for analyses by the multiplexer 70 which has its select terminals connected to the outputs of a latch 73. By enabling the latch 73 through chip select line 74, the microprocessor 35 can write a code to the latch 73 which selects either of the two scanner signals 71 or 72. The selected scanner signal appears at a "Y" output on the multiplexer 70 and its inversion appears at a "W" output. The selected scanner signal is applied directly to RST1 and RST2 inputs on the microprocessor 35 and to gate inputs Gϕ and G1 on a timer/counter circuit 75.

Referring still to Fig. 2B, the timer/counter 75 is a programmable device which receives data through the data bus 36 when a chip select control line 76 is active. It contains three counters which are preset to given values and which are decremented by pulses received at clock inputs CLKϕ, CLK1 and CLK2. The clock inputs CLKϕ and CLK1 are driven by the output of a second timer/counter 77, and the third clock input

CLK2 is driven by a gate 78 which receives a press speed feedback signal in the form of a pulse stream produced by a shaft encoder. An RST3 control line is enabled when the internal counter driven by the speed feedback signal (CLK2) reaches its terminal count, and this event is employed by the microprocessor 35 to sense press speed.

The other two counters in the timer/counter 75 generate interrupt requests INT7 and INT4 when their terminal counts are reached. Only one of these counters is operated at any single moment, since the gate inputs G1 and Gϕ are always in opposite logic states. For example, when the scanner signal at the multiplexer output "Y" is high, counter 1 is enabled through gate G1. The logic low voltage at the "W" output disables counter ϕ through gate Gϕ and it generates a reset request to the microprocessor 35 through control line RST1. In response the microprocessor 35 reads the value of counter ϕ and resets to a preselected value. When the multiplexer outputs Y and W change logic state the reverse is true. Counter ϕ becomes active and counter 1 is stopped. The reset request on RST2 vectors the microprocessor 35 to a program which reads the value of counter 1 and presets it for the next cycle. The timer/counter 75 is thus employed to measure the duration of each light and dark portion of the register pattern 25 as it passes beneath the optical scanner 18 or 19. These measured intervals are employed by the microprocessor 35 to determine the register of each printing unit 2 to 5 as will be described in more detail below.

Referring particularly to Figs. 1 and 2C, the last section of the system processor 15 interfaces with the main control panel 16. This interface includes a keyboard/display interface circuit 80 which connects to the data bus 36 and to a number of control lines in the bus 43. A model 8279 integrated circuit manufactured by Intel, Inc. is employed and it is programmed with control data from the microprocessor 35 to scan a keyboard matrix 81 and to maintain a display matrix 82. The keyboard matric includes a variety of control panel switches which are arranged in an eight-by-eight matrix. The interface circuit 80 outputs a sequence of three-bit codes to a 3-to-8 decoder 83 and inputs a corresponding sequence of eight bytes of keyboard data through a bus 84. The state of up to sixty-four keys are stored in a keyboard image table inside the interface 80, and this table may be read by the microprocessor 35. Similarly, an output image table is written to the interface circuit 80 by the microprocessor 35 and the keyboard/display interface 80 operates to output this data in sequence through an eight-bit bus 84 to the display matrix 82. The display 82 is comprised of individual lamps arranged in an eight-by-sixteen matrix with the sixteen rows being sequentially selected by a 4-bit code applied to a 4-to-16 decoder circuit 85.

The control panel 16 also includes a 40-digit alphanumeric display subsystem 87 which connects to the data bus 36 and control bus 43. A display subsystem model DE/240 manufactured by Digital Electronics Corporation is employed and it is enabled through a control line 88 by the decoder circuit 50. ASCII characters, including control characters, may be output to the display 87 and an internal cursor determines where the next ASCII character will appear. This cursor may be moved by outputting ASCII control characters to the display 87.

Referring particularly to Figs. 1, 3 and 5, the scanner interface 17 couples information between the optical scanners 18 and 19 and the system processor 15. The scanner interface 17 includes a pair of identical input circuits 90A and 90B and a pair of identical output

0123305

circuits 91A and 91B. The output circuit 91A connects to the output port leads 66 and 67 in the I/O bus 62 and its output terminal 92A and 93B connect respectively to the scanner motor relay 29 and the scanner motor direction relay 30. When a logic high voltage appears on lead 66 the scanner 18 is to be moved left, and when a logic high voltage appears on lead 67, it is to be moved to the right. These signals are applied through inverter gates 94 and 95 to respective NAND gates 96 and 97, and the NAND gates 96 and 97 drive the inputs of an exclusive OR gate 98. The OR gate 98 energizes the scanner motor on/off relay 29 through an inverter gate 99 when motion in either direction is indicated. The output of NAND gate 97 provides a direction indication which is coupled through inverter gate 100 to energize or de-energize the scanner motor direction relay 30.

Referring particularly to Figs. 1 and 3, the scanners 18 and 19 can also be positioned manually using a remote control panel 101 which connects to the scanner interface 17. This manual mode of operation is used primarily during start-up to orient the scanners 18 and 19 for automatic operation. The panel 101 includes a pair of pushbutton switches 102 and 103 which connect to inputs on respective NAND gates 96 and 97. By depressing the pushbutton 102 the operator can move the scanner 18 to the left and by depressing pushbutton 103 the scanner 18 moves to the right. The panel 101 also includes a pair of indicator lamps 104 and 105, one of which is energized when the optical scanner 18 is moved in either direction. The lamps 104 and 105 are driven by inverter gates 106 and 107 which connect to the outputs of NAND gates 96 and 97.

Referring particularly to Fig. 3, the input circuit 90A of the scanner interface 27 receives an analog electrical signal through the leads 24A from the optical scanner 18 and generates a corresponding digital signal to the system processor 15 through lead 71. As shown in Fig. 6, as the register pattern 25 passes beneath the optical scanner 18, an analog signal 110 is produced. The register pattern 25 includes reference portions 111 and 112 which are printed by one of the printing units 2 to 5 along with reference color marks 113. The reference color is preferably black because it produces a strong output signal from the optical scanner 18. Additional colors, indicated by color marks 114 to 116, may be printed by the remaining printing units, and the amplitude of the scanner output signal which they produce will depend on the color of the ink. The scanner interface 17 converts this analog signal 110 to a corresponding logic level signal 117 for input to the system processor 15.

Referring still to Fig. 3, the analog input signal 110 is received through leads 24 and amplified by operational amplifier 120. The output of amplifier 120 is applied directly to one input of a comparator 121 and to the inputs of a positive precision peak detector formed around amplifier 122 and a negative precision peak detector formed around amplifier 123. The outputs of the peak detectors 122 and 123 are buffered by amplifiers 124 and 125 and summed at potentiometer 126. The reference signal produced at potentiometer 126 is applied to the inverting input of the comparator 121, and it serves as a voltage level which is proportional to approximately twenty percent of the peak signal produced by the optical scanner 18. As shown in Fig. 6, this reference level is indicated by dashed line 127 and it is well below the minimum signal produced by any colored mark in the register pattern 25. The comparator 121 is thus driven sharply into and out of saturation to produce the digitized output signal 117 on the lead 71.

Referring particularly to Figs. 1 and 4A, the output controller 20 receives command data from the system processor 15 through the serial data link 58 and operates the motors which control the register for each printing unit 2 to 5. As shown in Fig. 4A, the output controller 20 is microprocessor-based and includes many of the same circuit elements as the system processor 15. Indeed, these same elements are indicated with the same reference numbers as in Fig. 2A, but with the prefix "2" to distinguish them from the corresponding system processor elements. Although the RAM 244 and ROM 247 are the same as the corresponding elements in the system processor, it can be appreciated that the data structures and programs stored therein are different and that their size need not be the same.

Referring particularly to Fig. 4B, the input/output section of the output controller 20 is substantially different than that of the system processor 15. It includes a set of four 8-bit latches 130 to 133 which connect to the data bus 236 and which are separately enabled through chip select lines 134 to 137 driven by the decoder circuit 250. An 8-bit byte of data may be written to a selected latch 130 to 133 when a write control line WR is driven low. The outputs of each latch 130 to 133 are connected through line drivers 138 to relays which operate the register control motors on each printing unit 2 to 5. For example, the latch 130 drives the four motors (upper lateral, upper rotational, lower lateral and lower rotational) on the first printing unit 2. If the top print image for unit 2 is to be advanced, the upper rotational motor is energized in the forward direction by outputing a logic "1" to the bit 3 position of latch 130. When the adjustment has been made, a logic "0" is output to de-energize the same motor.

The status of the four register control motors in each printing unit 2 to 5 is also continuously monitored by the output controller 20. Referring again to Fig. 4B, a 4-bit latch 140 connects to the data bus 236 and is enabled through a chip select line 141 to apply a 4-bit code to the select inputs of a multiplexor 142. The sixteen inputs on the multiplexor 142 connect to input circuits 143 which receive signals from each register control motor on the press 1 indicating whether or not the motor is energized. When a chip select line 144 is enabled, one of the sixteen inputs to the multiplexor 142 is selected and the signal thereon is applied to a serial input port SID on the microprocessor 235. By sequentially writing different codes to the latch 140 and enabling the multiplexor 142, the microprocessor 235 can scan the state of the register control motors and transmit a two-byte status message to the system processor 15 through the serial data link 58.

It should be apparent that a number of variations are possible in the hardware of the preferred embodiment. Although the system could be formed as a single microprocessor-based unit, it is physically convenient to separate the output controller from the centrally located system processor 15 in most installations. The output controller 20 is usually located on the press 1 with other press control electronics. Also, the hardware disclosed herein is shown controlling four printing units for a single web 6. However, it may be more economical in some installations to use the same system processor to control register on additional printing units for additional webs. Indeed, the system processor 15 and output controller 20 disclosed herein have been employed to control register for both sides of two webs, or in other words, eight printing units and four optical scanners.

Before discussing in detail the operation of the register control system, it is helpful to discuss the manner in which the register marks 111 to 116 in the register pattern 25 are employed to control color-to-color register. Referring to Figs. 6 and 7A, when register is perfect and the optical scanner is positioned to focus at the center (dashed line 150) of the register pattern 25 as it passes by, a series of voltage pulses are produced as shown at 110. Each register mark 113 to 116 is comprised of two triangular sections that produce two voltage pulses of equal time duration. If the focal point of the scanner is not centered as shown by the dashed line 151 in Fig. 7B, the two pulses produced by the reference mark 113 are not of equal duration. When this condition is sensed by the system processor 15, it outputs signals to the scanner interface 16 which reposition the optical scanner 18 or 19 at the center of the pattern. Thus, if the web 6 shifts laterally as it passes through the dryer 7 and chill unit 8, the optical scanners 18 and 19 will automatically track the movement.

Referring particularly to Figs. 1 and 7C, if the print unit 4, for example is misregistered in the lateral direction, the register mark 115 which it produces will not be properly aligned. With the optical scanner properly centered as indicated by dashed line 152, the two voltage pulses produced by the register mark 115 will be unequal in duration. If the misregister is to the left as shown, the first pulse will be shorter, and if the misregister is to the right, the second voltage pulse will be shorter. Either situation is sensed by the system processor 15 which monitors the scanner waveform 117 (Fig. 6) and which outputs corrective commands to the output controller 20 to move the print cylinder back into register.

Referring to Figs. 1 and 7D, if the printing unit 3 is misregistered in the rotational direction, the register mark 114 which it produces will not be properly aligned in the register pattern 25. More specifically, the two voltage pulses produced by the register mark 114 are either advanced or delayed relative to the remainder of the registration pattern 25. As shown in Fig. 7A the leading and trailing edges of the register mark 114 are 5.40 and 6,35 cm (2.125 and 2.50 inches) respectively from the leading edge of the pattern 25 when register is proper. The center of the mark 114 is, therefore, 5.87 cm (2.3125 inches) from the pattern reference point when the printing unit 3 is in register. As will be explained in more detail below, the system processor 15 analyzes the signal 117 (Fig. 6) produced by the optical scanners 18 and 19 and determines the center of the register marks 114 to 116 relative to the pattern reference point. If any deviations of these center points are detected, the system processor 15 outputs a command to the output controller 20 which brings the printing unit back into register.

Referring particularly to Fig. 1, the register control system can be operated in a conventional "open loop", or "manual" mode in which the human operator enters corrective data into the system through the main control panel 16. Such corrective data is processed by the system processor 15 to form an alignment command which is output to the controller 20. Such an alignment command may, for example, direct that the register control motor for the upper portion of the printing unit 2 be energized to move laterally 12.7/1000 of a cm (five-thousandths of an inch). The output controller 20 accepts such commands and operates the proper motor to carry out the alignment motion. The human operator then checks the register of the signatures at the output of the press to determine if further corrections are necessary. While the system of the present invention may be operated in this conventional manual mode, it can also be switched to an automatic mode in which the register of the signatures is examined by the optical scanner 18 or 19 and appropriate alignment commands are automatically produced and output to the controller 20. While the automation of this process may appear straight forward, in practice there are many difficulties which must be overcome.

Most of the difficulties which arise relate to the imperfect nature of the printing process. For example, the register pattern 25 may not print accurately or properly at all times. One of its marks may not be properly aligned with the image which it is to register, or the pattern may be distored by stretching of the web due to press tension. Also, the web has a certain amount of random lateral motion, or "jitter", as it moves through the press which produces a corresponding random misregister. Such random misregister can be caused by other factors as well, such as momentary variations in web thickness. It is neither possible nor desirable to make register corrections in response to such short term changes. The human operator is capable of discerning the difference between these random short term changes and long term changes in register, and it is important that the automatic register control do the same.

As indicated above, the programs which direct the operation of the system processor 15 are stored in its ROM 47. The operation of the register control system will now be described with reference to flow charts which schematically illustrate the functions carried out by these programs. The overall operation will be described in general terms first, and then the data collection and data analysis functions will be described in detail.

Referring particularly to Fig. 8, when the register control system is powered up, a set of instructions indicated by process block 200 is executed to initialize the system hardware and the data structures stored in the RAM 44 (Fig. 2A). A loop is then entered in which a set of instructions, indicated by process block 201, is executed to enable the operator to enter data. As will be described in more detail below, this set-up data includes information about the particular printing job, such as which printing unit is the reference unit and which register marks are produced by which units. In addition, the set-up data may pertain to the press, such as its characteristic jitter and its speed. The operator may also enter offset data which compensates for errors in the printing of the register pattern 25.

After the system has been set up the operator may switch to automatic control of register. Each surface of the web 6 is controlled separately and it is possible to have automatic control of one surface and manual control of the other surface. If automatic control has been selected, as indicated at decision block 202, a data collection sequence is begun for one surface of the web 6. This sequence includes a preparation phase indicated by process block 203 in which a data table 204 in the RAM 44 is cleared. Referring to Fig. 2B, such preparation includes the selection of the proper input channel on the multiplexer 70 and the presetting of the counter (2) in the timer/counter 75. The counter (2) is decremented by pulses received from an encoder on the printing press, and when decremented to zero, an interrupt request is generated on line RST3. The counter (2) is preset to a value which will result in an interrupt after the plate cylinders in each press unit have rotated two and one-quarter revolutions. This ensures that at least two register patterns 25 are scanned during the data acquisition interval. The actual data acquisition is accomplished by two inter-

0123305

rupt driven routines which store a sequence of numbers in the data table 204.

When the data acquisition sequence is completed, as indicated at process block 206, the numbers stored in the data table 204 are examined to determine if the register patterns 25 were correctly and accurately scanned. As indicated at decision block 207, if good data was not obtained, the system loops back through process block 208 to collect data on the other surface of the web 6. As indicated above, there are many reasons why poor register data may be obtained, but in most instances the situation corrects itself and good data may be collected a moment later.

Referring still to Fig. 8, when good data is obtained from a scan sequence, the data is analyzed and used both to correct the lateral position of the scanner 18 or 19 and to correct the register of the printing units 2 to 5. As shown by process block 209, the errors in both scanner position and color register are calculated. The errors are computed by averaging the errors indicated by the two register patterns scanned during the data acquisition sequence. This averaged error data is then processed as indicated by block 210, to determine if corrections should be made. This further processing is designed to eliminate needless corrections where the measured errors are due to short term random events such as jitter.

If the optical scanner 18 or 19 is not centered on the register pattern 25 and a move is required as indicated at decision block 211, a routine indicated by process block 212 is executed. Referring to Figs. 2B and 5, this routine 212 writes data to the latch 63 which energizes the proper scanner motor 28 in the desired direction. The counter (2) in the timer/counter circuit 75 is then preset to an appropriate value, and when it "times out", the scanner motor 28 is turned off by again writing to the latch 63. In this manner, the scanner 18 or 19 can be moved to the left or right to "track" the register patterns 25 being printed on the web 6.

Referring again to Fig. 8, before looping back to perform the next data collection sequence, register corrections are made. As determined at decision block 213, when significant register errors are detected, a routine 214 is executed to generate alignment commands to the output controller 20. Referring particularly to Fig. 2A, the routine 214 generates a message to the output controller 20 through the UART 54. This message is a command that identifies the print unit, web surface and the lateral or rotational motor. The alignment command also indicates the direction of the move and the distance in 2.54/1000 of a cm (thousandths of an inch). Referring particularly to Figs. 4A and 4B, the output controller 20 receives this alignment command at its UART 254 and writes an appropriate bit pattern to one of the output latches 130 to 133 to energize the proper alignment motor for the time needed to move this commanded distance. Referring again to Fig. 8, after the alignment commands have been issued to the output controller 20, the system loops back to the process block 208 to scan the other surface of the web 6.

It should be apparent from this general description that the register control system collects data from one web surface, makes corrections to scanner position and color register when necessary, and then repeats the sequence with the other web surface. The number of print surfaces which can be monitored in this manner need not be limited to two. The system is much faster than human operators in making register corrections, even when four print surfaces are scanned and even when a significant portion of the collected scanner data is discarded as unacceptable. Indeed, one of the functions of the process indicated by block 210 is to average the large amount of collected data, and to thereby effectively slow the response of the register control system to a level which is appropriate to the particular press and printing process being controlled.

Referring particularly to Figs. 2B and 9A-C, the automatic control of color register will now be described in more detail. Each data collection cycle is comprised of a series of interrupts which are produced by the scanner signal appearing at the Y and W outputs on the multiplexer 70. As indicated at process block 220, this cycle is initiated by first presetting the counter (2) in the timer/counter 75 to a value which represents two and one-quarter revolutions of a plate cylinder. The RST2 and RST3 interrupts are then enabled as indicated at process block 221, and the system then waits for the RST3 interrupt to occur at process block 222. Incremental position feedback pulses are applied to decrement the counter (2) through the gate 78, and after two and one-quarter plate cylinder revolutions, and RST3 interrupt occurs and the data collection cycle is terminated. As indicated at process block 223, the three interrupts RST1, RST2 and RST3 are then disabled and the system proceeds to examine the collected data.

Referring particularly to Figs. 2B and 6, as the register pattern 25 passes beneath the active scanner 18 or 19 during the data collection cycle, a series of logic high (light) and logic low (dark) signals are produced and a corresponding series of RST1 and RST2 interrupts occur. That is, when the scanner "sees" a mark in the pattern 25 an RST1 interrupt is produced, and when it sees light, and RST2 interrupt is produced. Referring particularly to Fig. 9C, an RST2 interrupt occurs immediately after the data collection cycle begins and the system is vectored to an RST2 interrupt routine. As indicated at process blocks 225 and 226, the first functions performed by this routine is to disable further RST2 interrupts and to enable the RST1 interrupt. As indicated at process block 227, the counter (1) in the timer/counter 75 is then enabled and the counter (0) is disabled. The value of counter (0) is then read from the timer/counter 75 and saved in the data table 204 of the RAM 44 (Fig. 2A), as indicated at process block 228. The counter (0) is then reset, as indicated at process block 229, and the system returns to await the RST1 interrupt.

Referring particularly to Fig. 2B, when the leading edge of a mark in the register pattern 25 is detected, an RST1 interrupt occurs. The system is vectored to a service routine which disables the RST1 interrupt and enables the RST2 interrupt as indicated at process blocks 230 and 231. The counter (1) in the timer/counter 75 is then disabled and counter (0) is enabled to start counting, as indicated at process block 232. The count in counter (1) is then read from the timer/counter 75 and saved in the data table 204, as indicated at process block 233; and the counter (1) is reset at process block 234 in preparation for the next RST2 interrupt.

The RST1 and RST2 interrupts occur alternately during the data collection cycle as the scanner 18 or 19 alternately sees light and dark segments of the register patterns 25. The counter values which are stored in the data table 204 by the RST1 and RST2 interrupt routines represent the duration of each light or dark segment seen by the scanner 18 or 19 and these numbers can be converted to dimensions which correlate with those dimensions illustrated in Fig. 7A.

The data collection sequence is terminated when an RST3 interrupt occurs after two and one-quarter revolutions of each printing unit plate cylinder. Referring to Figs. 7 and 10, the RST3 interrupt service routine is then executed,and the first function, as indicated by process block 250, is to convert the sequence of counter numbers stored in the data table 204 to corresponding dimensions. These dimensions indicate the size of each mark and their spacing. As indicated at process block 251, the size of each mark is then read from the data table 204 and examined to determine if it is the 2.54 cm (one inch) reference mark 111 which indicates the beginning of the register pattern 25. If not, as determined at decision block 252, the system loops to read the next mark from the data table 204. When the 2.54 cm (one inch) reference mark 111 is found, the dimension which corresponds to the 1.27 cm (one-half inch) reference mark 112 is read from the data table 204. If this mark is indeed 1.27 cm (one-half inch) long, a register pattern 25 has been found. Otherwise, the system loops at decision block 253 to continue the search for valid data.

When a register pattern 25 is found in the data table 204, the dimensions thereof are calibrated as indicated by process block 254. This is accomplished by finding the distance between the leading edge of the 2.54 cm (one inch) reference mark 111 and the leading edge of the 1.27 cm (one-half inch) reference mark 112. This distance should be exactly 11.43 cm (four and one-half inches), and all of the data table entries are scaled to exactly produce this distance. This distance measurement is employed to calibrate the dimensions in the data table 204 because the measurement between leading edges of the reference marks 111 and 112 is relatively immune to inking problems.

Smearing usually occurs at the trailing edge, not the leading edge, and the growth of marks due to an overabundance of ink affects both leading edges equally.

Referring still to Figs. 7 and 10, the reference color marks 113 are examined next to determine if they are present and are printed properly. If not, as indicated at decision block 255, the system loops and continues the search for good data. The same tests are then performed on the color marks 114 to 116 as indicated at decision block 256, and if good data is obtained for the entire register pattern 25, the location of this data in the table 204 is identified, as indicated by process block 257.

The system continues to read from the data table 204 until the last entry is reached. When this occurs, as determined at decision block 258, a test is made at decision block 259 to determine if good data for two register patterns 25 has been located. If so, the system returns to process the data, otherwise, the data is discarded and the system loops to scan the other web surface as shown in Fig. 8.

The division of the reference mark 113 and color marks 114 to 116 into two triangular segments provides considerable diagnostic information which facilitates the above-described process. Referring particularly to Figs. 11A and 11B, each mark 113 to 116 is comprised of an upper section 260 and a lower section 261. The sections 260 and 261 are triangular in shape, and when formed properly, they have a combined length L which is constant regardless of their position relative to the scanner path 262 and 263. For example, the scanner path 262 passes through the sections 260 and 261 left of center to produce entries in the data table 204 of duration X_U1 and X_L1. On the other hand, the scanner path 263 passes through the sections 260 and 261 right of center to produce entries in the data table 204 of duration X_U2 and X_L2. Regardless of the scanner path, the sum of these readings is a constant value and a significant deviation from this constant value indicates that the register mark is not properly printed. That is:

$$X_U1 + X_L1 = L = X_U2 + X_L2$$

This diagnostic check is made by a set of instructions which are listed in Appendix A and which are executed as part of the decision blocks 255 and 256 shown in Fig. 10.

After two register patterns 25 have been successfully scanned, the rotational and lateral register errors are calculated for each print unit. Referring particularly to Figs. 12 and 13, the scanner misalignment is calculated first as indicated by process block 270. This is accomplished by measuring the difference between the measured length (A) on the upper section 271 of the reference mark 113 and the measured length (B) of the lower section 272. The misalignment, or tracking error, of the scanner 18 or 19 is given by the following expression:

$$\text{Error} = (B-A)/2$$

A loop is then entered in which the rotational and lateral register error for each print unit is calculated. As indicated by process block 273, the center C1 to C4 of each mark 113 to 116 is calculated by averaging the distance to its leading edge and its trailing edge. This method has been found to provide good immunity to colorimetry changes, since colorimetry changes usually cause both the leading and trailing edges to shift equally toward or away from the center. The centerlines of each mark 113 to 116 are ideally spaced 1.91 cm (.75 inches) apart and any deviation from this pattern is a direct measure of rotational misregister of the print unit. The rotational register error indicated by the respective color marks 114 to 116 is calculated as follows:

ROTERROR (114) = 1.91 (.75) - S1
ROTERROR (115) = 3.81 (1.50) - (S1+S2)
ROTERROR (116) = 5.72 (2.25) - (S1+S2+S3)

These values are calculated at process block 274 and saved in the RAM 44 (Fig. 2A).

Referring still to Figs. 12 and 13, the lateral register error for a printing unit is calculated next as indicated at process block 275. If the color marks 114 and 116 are in perfect register, they should be "off-center" by the same amount as the reference mark 113. The lateral register error indicated by the respective color marks 114 to 116 is calculated as follows:

LATERROR (114) = [(D-C) - (B-A)] /2
LATERROR (115) = [(F-E) - (B-A)] /2
LATERROR (116) = [(H-G) - (B-A)] /2

The division by 2 in these equations accounts for the 45-degree angle of the hypotenuse of the color triangles.

After each color mark 114 to 116 is analyzed as determined at decision block 276, the same analysis is performed on the data obtained for the second register pattern 25. When both patterns have been analyzed, as determined at decision block 277, the errors indicated by each pattern are compared. If the measured errors are substantially different, bad data is indicated and the system branches at decision block 278. Otherwise, the errors indicated by the two scanned register patterns 25 are averaged and saved in the RAM 44 as indicated at process block 279. This averaging step eliminates needless register corrections which would otherwise occur due to "packing errors".

Finally, although the color marks 114 to 116 may indicate a register error, this does not necessarily indicate that the print images are out of register. For example, the register marks 114 to 116 are generally laid down separately from the print image material on the plate, and perfect alignment is difficult. As a result, the register indicated by the marks may require an offset to give correct register of the print image. This offset may be entered by the operator during system set-up (Fig. 8) and the offset values are stored in a table 280 in the RAM 44 (Fig. 2A). These offsets are added to the measured register errors at process block 281 to provide register error data which is stored in a table 282 in the RAM 44. As indicated above, this error data is employed to form motion commands to the scanner interface 17 to re-align the scanner 18 or 19 with the center line of the register patterns 25. This data is also employed to produce alignment commands for the output controller 20 which correct the register errors in each printing unit 2 to 5.

Referring particularly to Fig. 8, the error data in table 282 is processed at block 210 prior to the formation of any scanner motion signal or alignment command. This processing is indicated by the flow chart of Fig. 14, and it is intended to further eliminate needless corrections. A loop 290 is entered which processes the register error data for each print unit in the press, and when the data for all print units has been processed, as determined at decision block 291, the loop 290 is exited.

If the measured rotational or lateral register error exceeds a preset limit, as determined at decision block 292, a correction is made. This preset limit is entered by the operator during the set-up process, and it is typically set to a value which is greater than the random jitter characteristic of the press. Register errors less than this limit may be self-correcting and changes are not made immediately. Instead, as indicated by process block 293, the most recent register error reading is averaged with the

N-1 previous error readings. The standard deviation of these n register error readings is then calculated at process block 294, and the average error is compared with this standard deviation. The standard deviation can be viewed as a measure of the uncertainty of the register error readings, and as long as the average error is less than this uncertainty, no corrections are made. When the average error increases above this uncertainty level however, a register correction is needed, as indicated at decision block 295. The number of readings (N) which are averaged in this manner is selected by the operator during the set-up process.

Even though a register correction is indicated, such corrections cannot be made at a high repetition rate because it requires motion for corrected signatures to travel from the printing units 2 to 5 to the chill rolls 8 where the scanners 18 and 19 are located. Thus, a motion delay is imposed in the register control loop to insure that signatures containing prior register corrections have ample opportunity to pass through the press. This delay is different for each printing unit 2 to 5 and it is selected when the control system is installed.

As determined at decision block 296, if the delay has elapsed since the last register correction, a register alignment command for the proper printing unit 2 to 5 and web surface is formed. As indicated at process block 297, the alignment command may alter either rotational or lateral register or both. The command is output to the output controller 20 which operates to execute the alignment command. As indicated at process block 298, a timer associated with the printing unit 2 to 5 and web surface which is affected by this alignment command is then preset to provide the necessary delay time. As shown in Fig. 2A, a delay table 299 is stored in the RAM 44 which includes a "software" timer for each printing unit and web surface. The appropriate timer is set at process block 298 with the proper delay time, and this delay time is subsequently measured by periodic comparison with a real time clock formed by the timer/counter circuit 77 (Fig. 2B).

The register control system controls the register of each printing unit relative to the printing unit which produces the reference marks 111, 112 and 113. Because register is measured relative to the reference marks 111, 112 and 113, rather than being measured relative to the frame of the press, any changes in the register of the reference printing unit will be corrected by making corresponding changes in the register of each color printing unit. While it is preferable this "reference" printing unit produces a black image, the selection of a reference printing unit and the number and position of the color printing units may be determined by the operator during the set-up process.

APPENDIX A

REGISTER MARK DIAGNOSTIC PROGRAM

```
OBJECT           SOURCE
 CODE          STATEMENT              COMMENTS

08D4 2A2F09 notras:    lhld clrtop     ;get top of color
08D7 EB                xchg            ;in DE
08D8 2A3109            lhld clrbot     ;and bottom
08DB CD0000            call avgdh      ;get center
08DE 44                mov b,h         ;sav in BC
08DF 4D                mov c,l
08E0 2A2B09            lhld topsiz     ;get top triangle size
08E3 EB                xchg            ;in DE
08E4 2A2D09            lhld botsiz     ;get bottom size
08E7 E5                push h          ;sav bottom size
08E8 19                dad d           ;get total size
08E9 D5                push d          ;save top size
08EA E5                push h          ;save total
08EB 110B09            lxi d,tottsz+2  ;allow for black
08EE 2A8D09            lhld totptr     ;get offset
08F1 29                dad h           ;2 bytes apiece
08F2 19                dad d           ;add in array start
08F3 EB                xchg            ;save this
08F4 2A9409            lhld surfac
08F7 29                dad h           ;2
08F8 29                dad h           ;4
08F9 29                dad h           ;8 bytes/surface
08FA 19                dad d           ;point to right part
                                        of array
08FB D1                pop d           ;get total back
08FC 73                mov m,e         ;save for viewing
08FD 23                inx h
08FE 72                mov m,d
08FF EB                xchg            ;put total back in HL
0900 E5                push h          ;save total
0901 2A9409            lhld surfac     ;12 bytes/surface
0904 29                dad h           ;2
0905 29                dad h           ;4
0906 54                mov d,h
0907 5D                mov e,l         ;save this
0908 29                dad h           ;8
0909 19                dad d           ;12!
090A 11C508            lxi d,colszl    ;point to table of
                                        limits of allowable size
090D 19                dad d           ;index into array
090E EB                xchg            ;save in DE
090F 2A8D09            lhld totptr     ;get color
0912 29                dad h           ;2 words/color
0913 29                dad h
0914 19                dad d           ;point to this color
0915 5E                mov e,m
0916 23                inx h
0917 56                mov d,m         ;get max size
0918 23                inx h           ;point to lsb of min
```

APPENDIX A (continued)

REGISTER MARK DIAGNOSTIC PROGRAM

```
OBJECT       SOURCE
 CODE        STATEMENT                       COMMENTS
0919 229099                shld mmxptr       ;save pointer to min
                    dseg
0999        mmxptr: ds     2                 ;temp pointer to colszl
                    cseg
091C E1                    pop h             ;get total back
091D CD0000                call cmpDE
0920 D1                    pop d             ;get top triangle size
                                              back
0921 E1                    pop h             ;and bottom size
0922 DA2B09                jc totrsm         ;skip this if total
                                              not too big
0925 E3                    xthl              ;get pointer to status
0926 7E                    mov a,m           ;mark smudges in data
0927 F604                  ori 4
0929 77                    mov m,a
092A E3                    xthl
092B E5     totrsm:        push h            ;save bottom size
092C D5                    push d            ;and top size
092D E5                    push h            ;save total size
092E 2A9909                lhld mmxptr       ;get pointer to minimum
                                              size
0931 5E                    mov e,m
0932 23                    inx h
0933 56                    mov d,m
0934 E1                    pop h             ;get total size back
0935 CD0000                call cmpDE        ;carry here if too small
0938 D1                    pop d             ;get top size
0939 E1                    pop h             ;and bottom size
093A D24209                jnc totrbg        ;skip this if OK
093D E3                    xthl              ;get pointer to status
093E 7E                    mov a,m
093F F608                  ori 8             ;show marks missing
0941 E3                    xthl
```

0123305

Claims

1. A register control system for a printing press, the combination comprising:

optical scanner means (18, 19) positioned to detect a register pattern (25) on a moving web (6), which pattern includes register marks (113 to 116) produced by a plurality of separately adjustable printing units (2 to 5), the optical scanner means being operable to generate an electrical signal indicative of the relative position of each register mark;

a processor (15) coupled to the optical scanner means to receive the electrical signal and including:

(a) means for designating a reference printing unit,

(b) means for establishing the relative position of each register mark produced by the other printing units with respect to the register mark produced by the designated reference printing unit,

(c) means for establishing a desired position for each of the other printing units,

(d) means for comparing each established relative position with the corresponding desired position to produce a register error for each of the other printing units which indicates their misregister with respect to the reference printing unit, and

(e) means for adjusting the position of each printing unit in response to its associated register error to reduce its misregister.

2. The register control system as recited in claim 1 in which each printing unit (2 to 5) has a rotational and a lateral position adjustment, the means for establishing the relative position of each register mark with respect to the register mark produced by the designated reference printing unit provides a lateral relative position and a rotational relative position, separate lateral and rotational desired positions are established for each of the other printing units, and separate lateral and rotational register errors are produced for separately operating the respective lateral and rotational adjustments of each of the other printing units.

3. The register control system as recited in claim 1 in which a keyboard (16) is coupled to the processor and the processor includes means for receiving position offset data from the keyboard and adding such position offset data to a selected desired position.

4. The register control system as recited in claim 1 in which each register mark (113 to 116) is divided into an upper section (260) and a lower section (261) and in which the length (L) of the register mark taken along any longitudinal axis through the register mark is a constant value

$$L = X_U + X_L$$

where: X_U = longitudinal dimension of upper section,
X_L = longitudinal dimension of lower section,

and the processor (15) includes error detection means for summing the lengths of the signals produced by the optical scanner means as it detects both the upper and lower sections of each register mark, and for indicating an error when the sum deviates a preset amount from said constant value.

5. The register control system as recited in claim 1 in which each register mark (113 to 116) is comprised of two sections (260, 261) and the optical scanner means produces two voltage pulses when it detects each register mark and the two sections are shaped such that the relative duration of the two voltage pulses indicates the lateral misregister of the printing unit which produced the register mark.

6. The register control system as recited in claim 1 in which said means for adjusting the position of each printing unit includes:

means for averaging successive ones of the register errors to produce an average register error for each of the other printing units; and

means for reducing the misregister of each of the other printing units when its associated average register error exceeds a selected amount.

7. The register control system as recited in claim 6 in which the means for adjusting the position of each printing unit also includes:

means for calculating the standard deviation of successive ones of the register errors to produce said selected amount.

8. The register control system as recited in claim 1 the processor (15) further includes:

(f) means for establishing a time delay interval when the position of a printing unit is adjusted to reduce misregister; and

(g) means for inhibiting the position adjustment of each printing unit until the time delay interval associated with that printing unit has expired.

9. A register control system for a printing press, the combination comprising:

optical scanner means (18, 19) mounted to detect a series of register patterns (25) on a moving web (6) and being operable to generate an electrical signal indicative of the register of each printing unit (2 to 5) in the press;

adjusting means (26 to 30) for moving the optical scanner laterally across the moving web in response to an adjustment command;

tracking means (15, 17) connected to receive the electrical signal from the optical scanner means (18, 19) and being operable to generate adjustment commands to the adjusting means (26 to 30) to maintain the optical scanner means (18, 19) in alignment with the register patterns on the moving web; and

processor means (15, 17, 20) connected to receive the electrical signal from the optical scanner means (18, 19) and being operable in response thereto to control the register of the printing units (2 to 5).

10. The register control system as recited in claim 6 in which the optical scanner means (18, 19) includes a scanner interface circuit (90A, 90B) which converts the analog signal (110) from an optical scanner device to a digital signal (117) comprised of voltage pulses of substantially uniform amplitude.

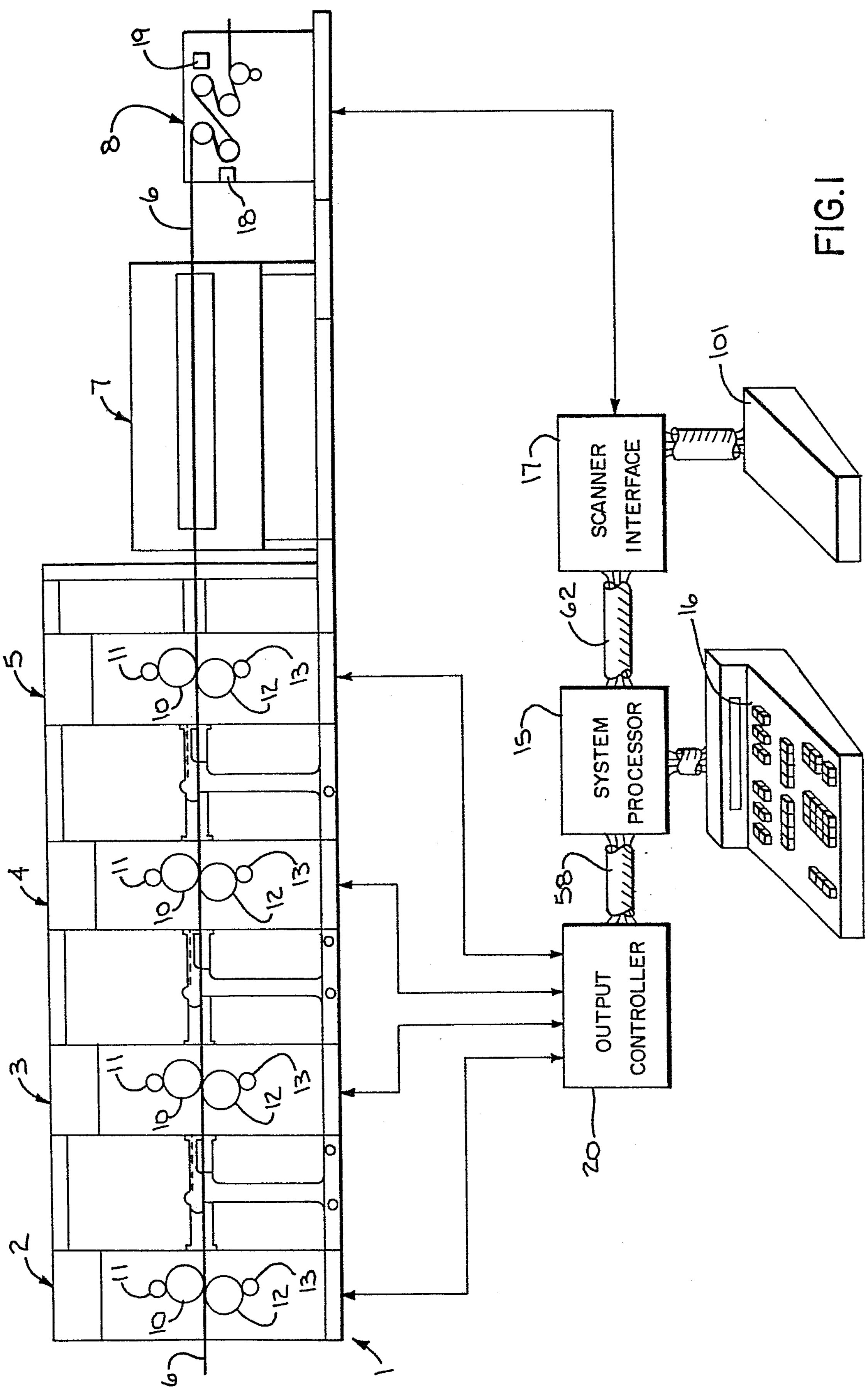


FIG.1

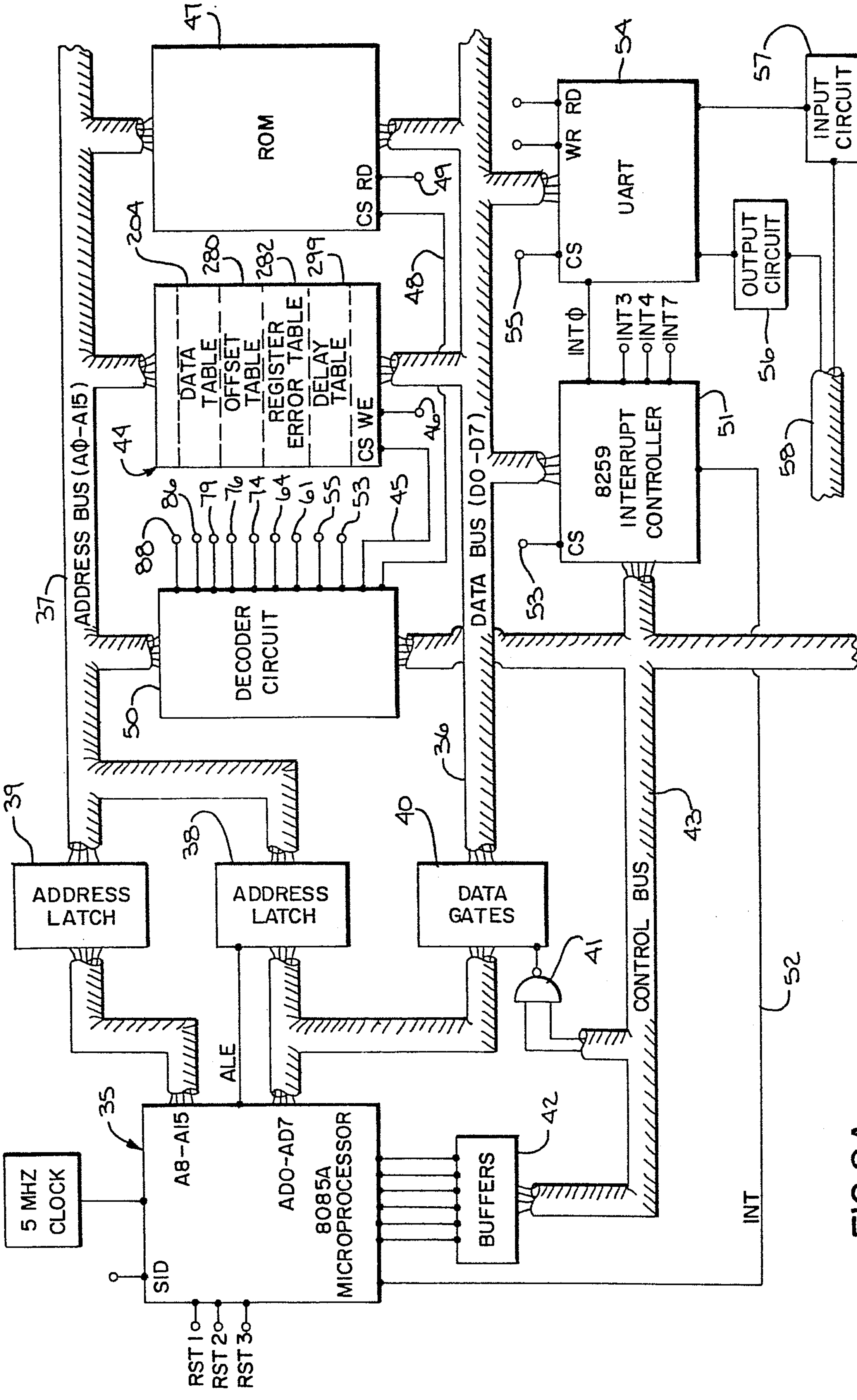

47
ROM
CS RD
49
48
UART
RD
WR
CS
54
55
INPUT CIRCUIT
57
OUTPUT CIRCUIT
56
58
204
280
282
299
DATA TABLE
OFFSET TABLE
REGISTER ERROR TABLE
DELAY TABLE
CS WE
46
44
INT Φ
INT3
INT4
INT7
8259 INTERRUPT CONTROLLER
CS
51
53
88
86
79
76
74
64
61
55
53
45
DECODER CIRCUIT
50
ADDRESS BUS (AΦ-A15)
37
DATA BUS (D0-D7)
36
39
ADDRESS LATCH
38
ADDRESS LATCH
40
DATA GATES
41
CONTROL BUS
43
52
ALE
35
A8-A15
AD0-AD7
8085A MICROPROCESSOR
SID
5 MHZ CLOCK
BUFFERS
42
INT
RST 1
RST 2
RST 3

FIG.2A

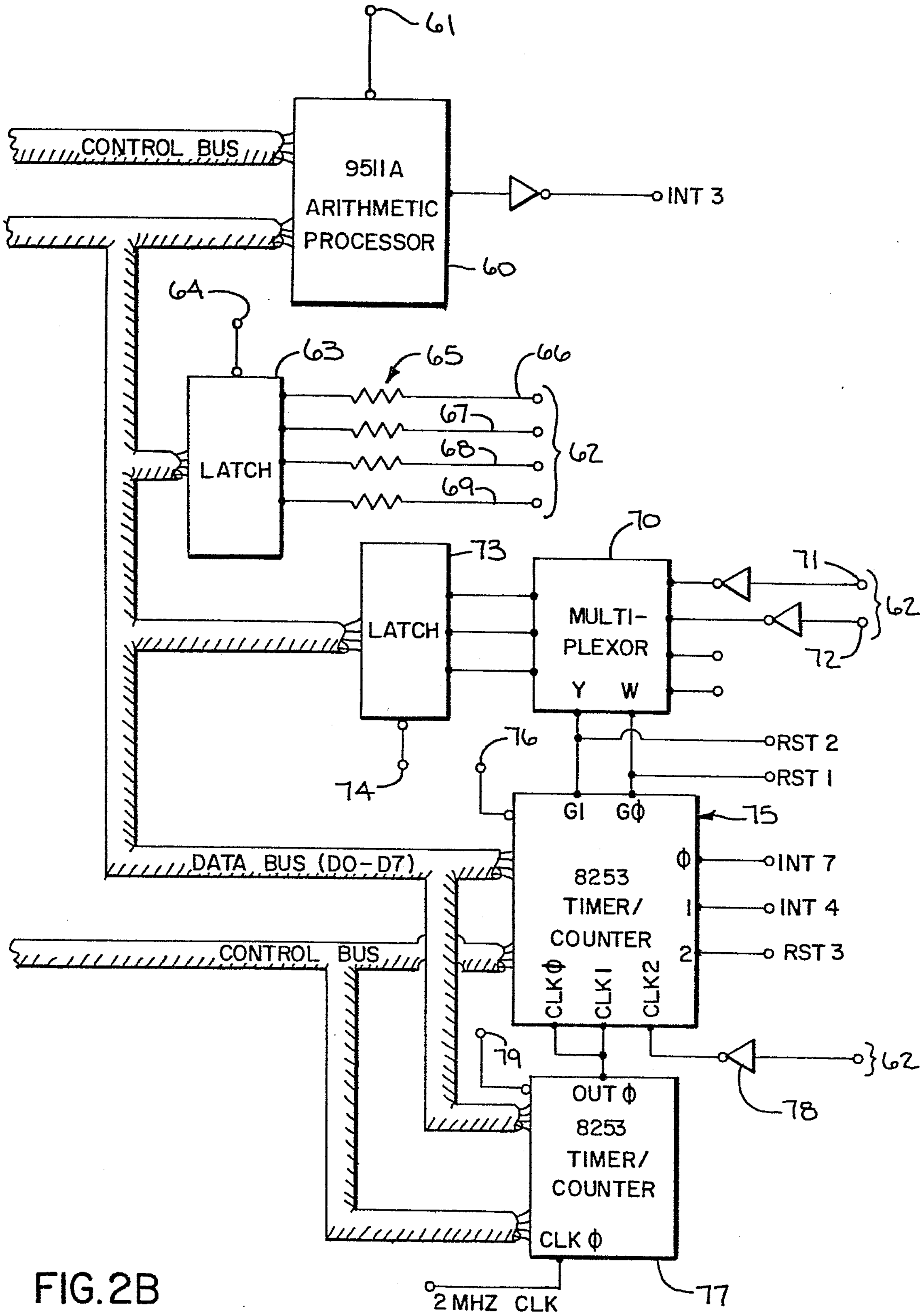

61
CONTROL BUS
9511A
ARITHMETIC
PROCESSOR
INT 3
60
64
63
65
66
LATCH
67
68
69
62
70
73
LATCH
MULTI-
PLEXOR
Y W
71
72
62
RST 2
RST 1
74
76
75
G1 GΦ
8253
TIMER/
COUNTER
Φ
INT 7
1
INT 4
2
RST 3
DATA BUS (D0-D7)
CONTROL BUS
CLKΦ
CLK1
CLK2
79
62
78
OUT Φ
8253
TIMER/
COUNTER
CLK Φ
2 MHZ CLK
77

FIG.2B

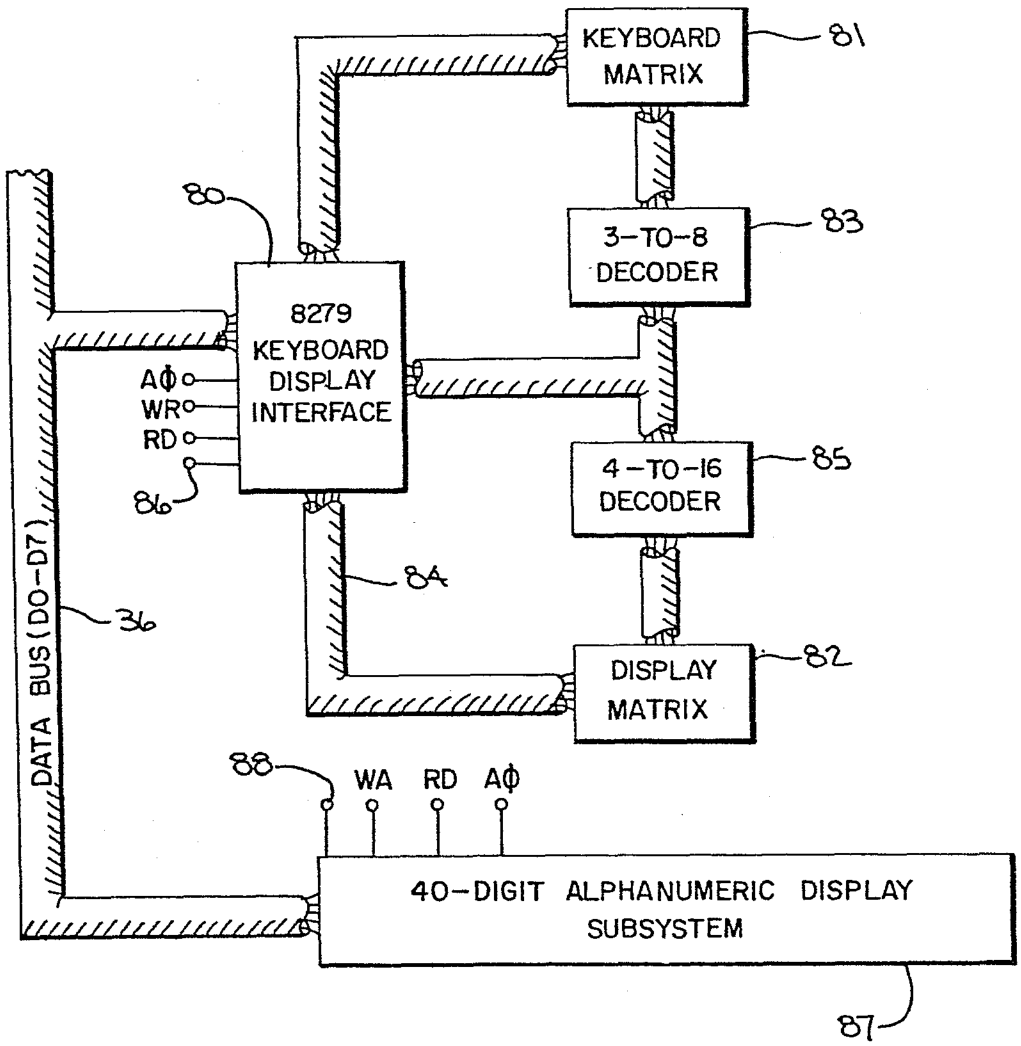
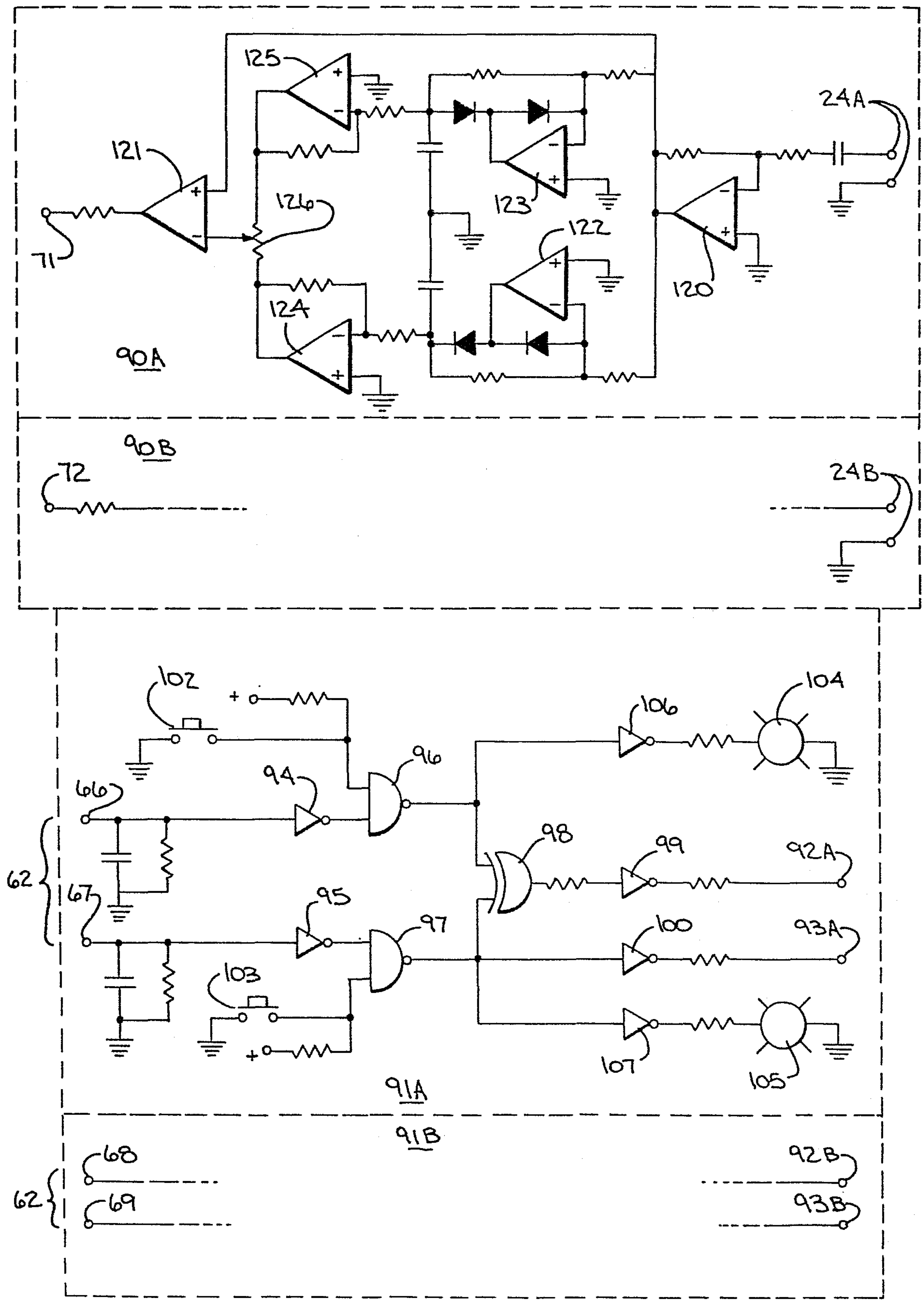

KEYBOARD MATRIX
81
80
3-TO-8 DECODER
83
8279 KEYBOARD DISPLAY INTERFACE
AΦ
WR
RD
86
4-TO-16 DECODER
85
84
DATA BUS (D0-D7)
36
DISPLAY MATRIX
82
88
WA
RD
AΦ
40-DIGIT ALPHANUMERIC DISPLAY SUBSYSTEM
87

FIG. 2C



125
121
126
123
122
24A
120
71
124
90A
90B
72
24B
102
104
106
96
94
66
98
99
92A
62
67
95
97
100
93A
103
107
105
91A
91B
68
92B
62
69
93B

FIG.3

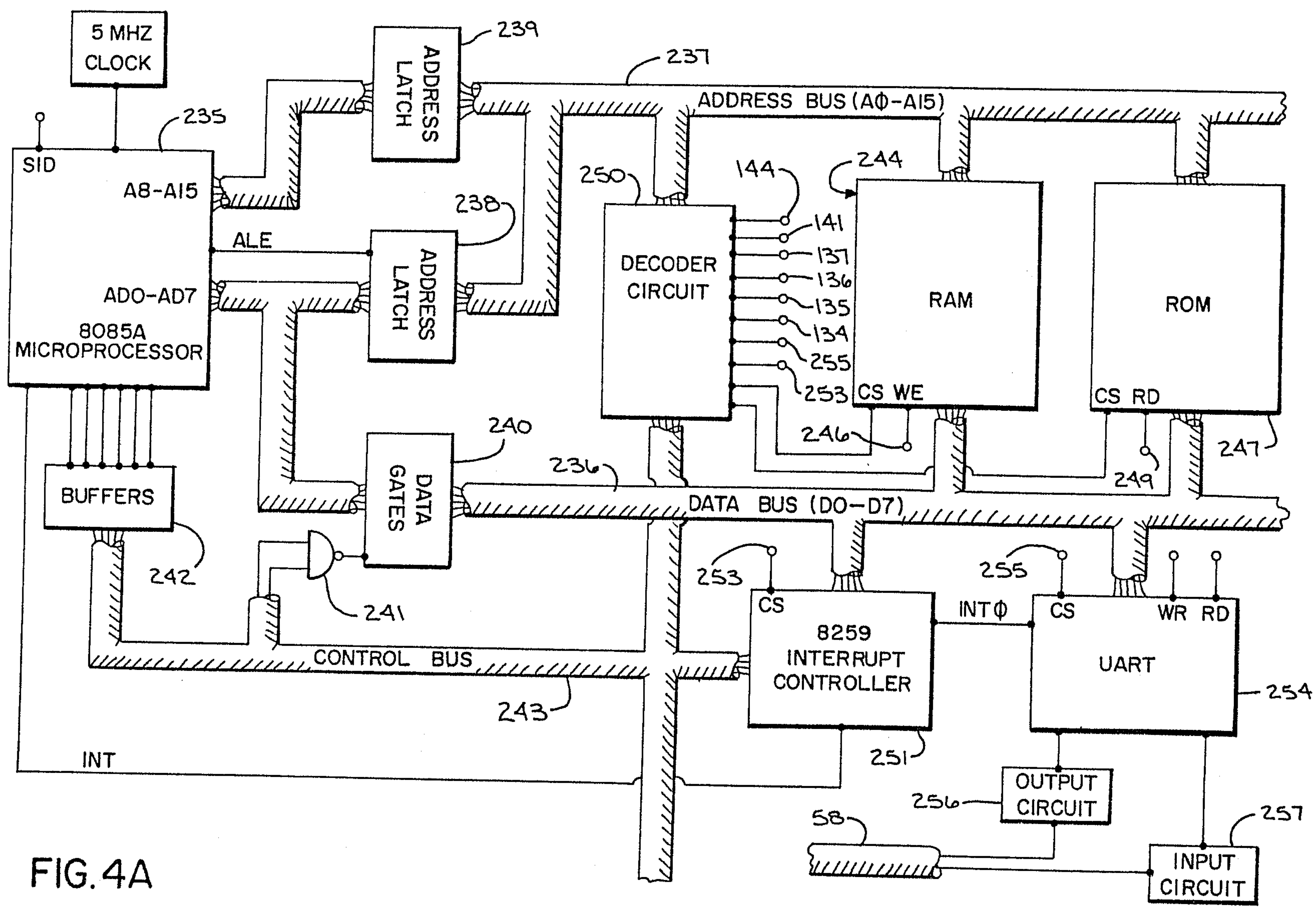
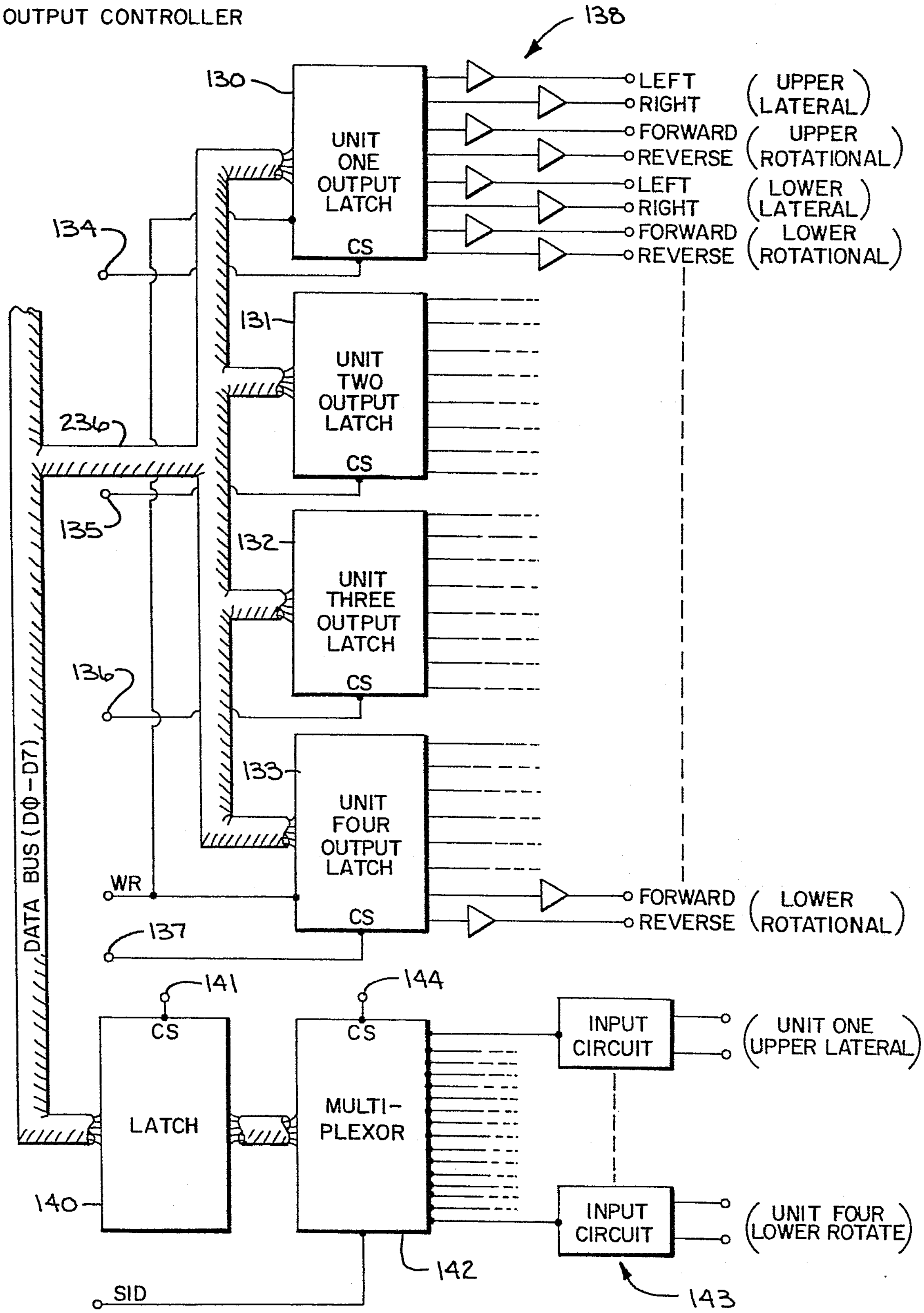

5 MHZ CLOCK
SID
A8-A15
ALE
AD0-AD7
8085A MICROPROCESSOR
ADDRESS LATCH
ADDRESS LATCH
DATA GATES
BUFFERS
ADDRESS BUS (AΦ-A15)
DATA BUS (D0-D7)
CONTROL BUS
INT
DECODER CIRCUIT
RAM
CS WE
ROM
CS RD
CS
8259 INTERRUPT CONTROLLER
INTΦ
CS
WR RD
UART
OUTPUT CIRCUIT
INPUT CIRCUIT
235
239
237
238
240
236
242
241
243
250
144
141
137
136
135
134
255
253
244
246
247
249
253
255
251
254
256
257
58

FIG. 4A

FIG.4B

OUTPUT CONTROLLER



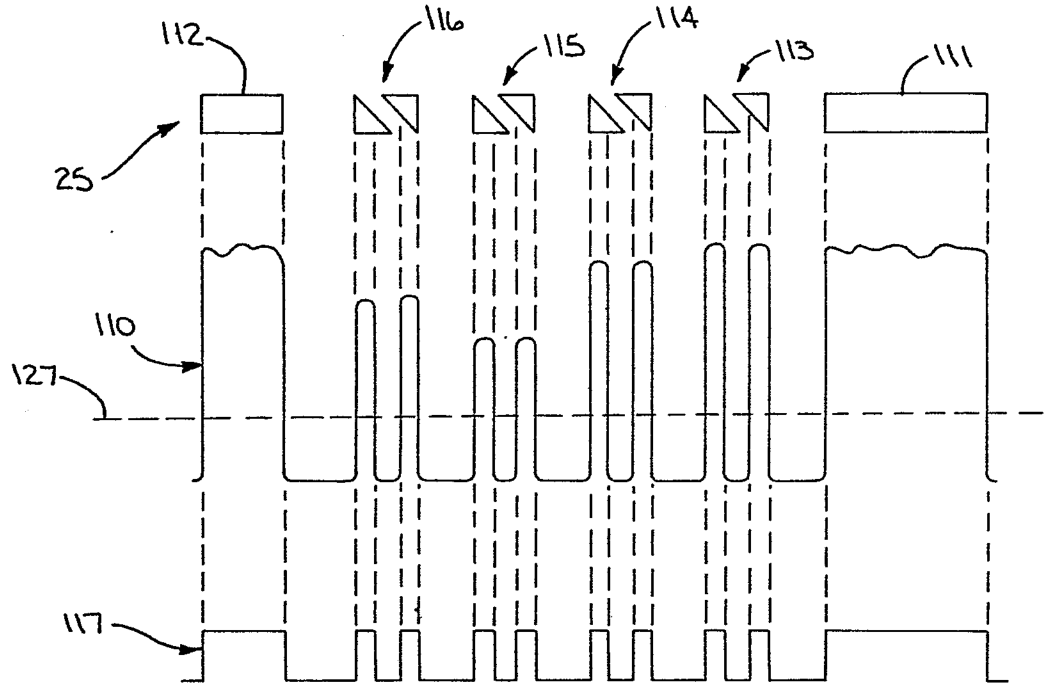

112
116
115
114
113
111
25
110
127
117

FIG.6

FIG.5

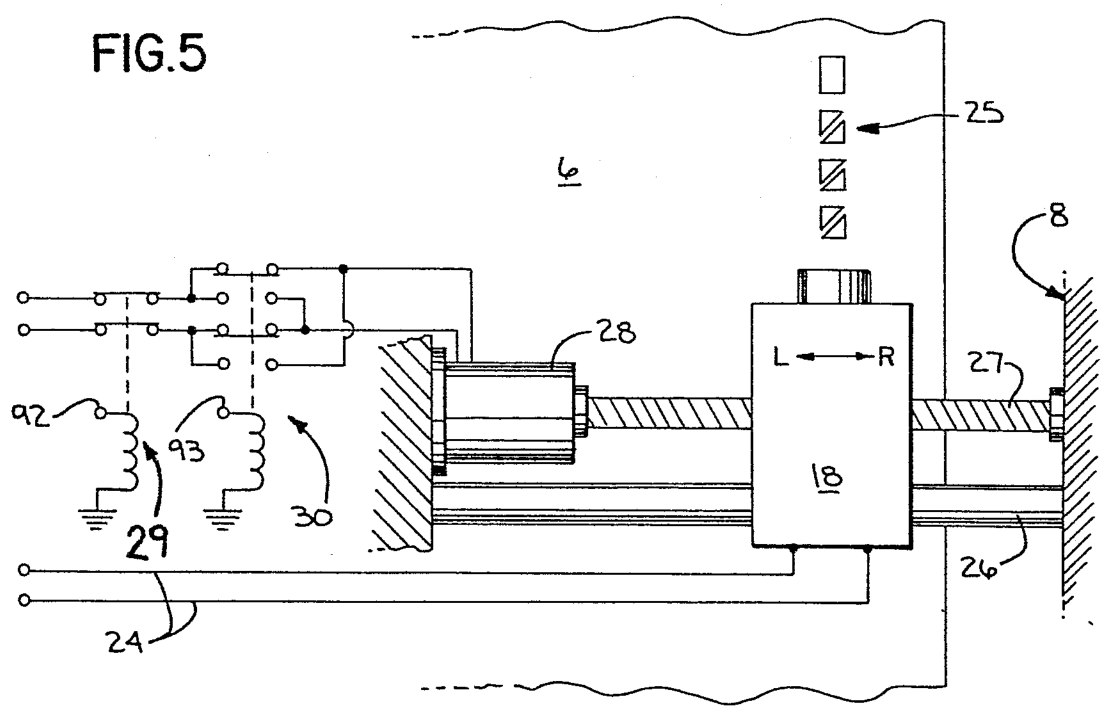

25
6
8
28
L R
27
92
93
30
18
29
26
24

FIG.7A FIG.7B FIG.7C FIG.7D

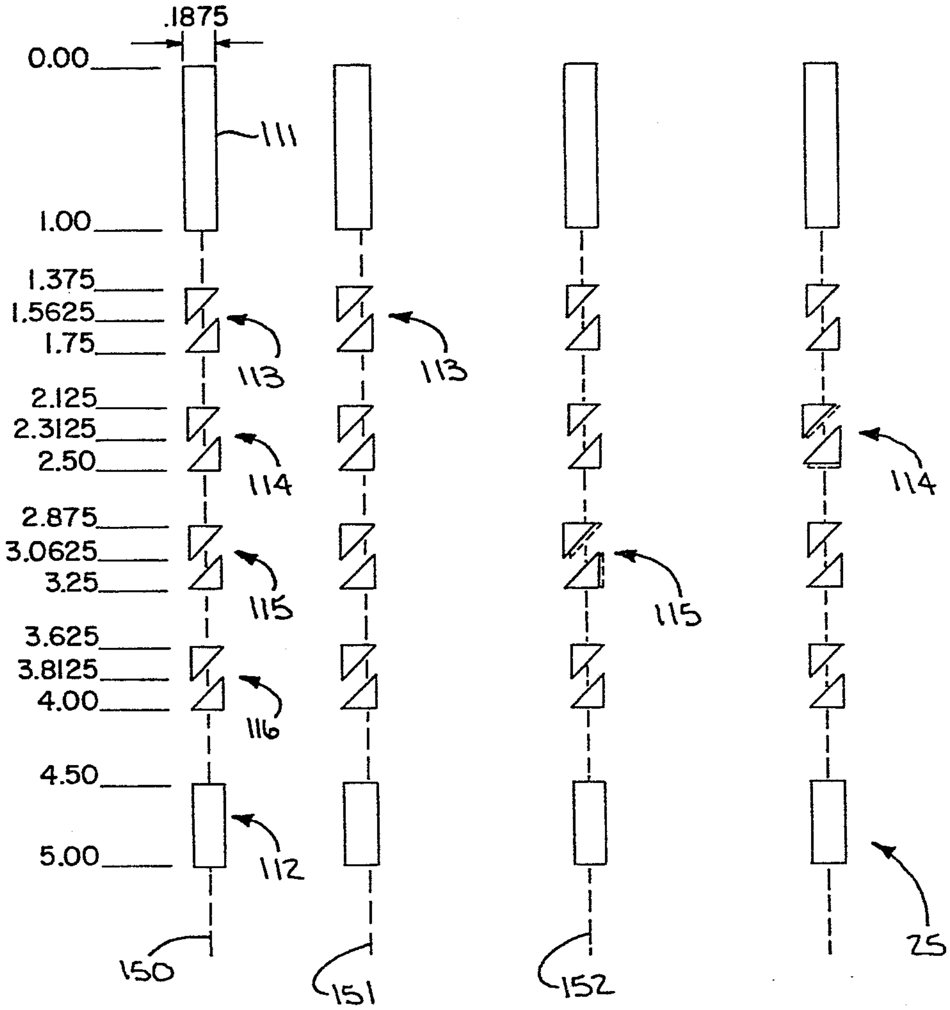
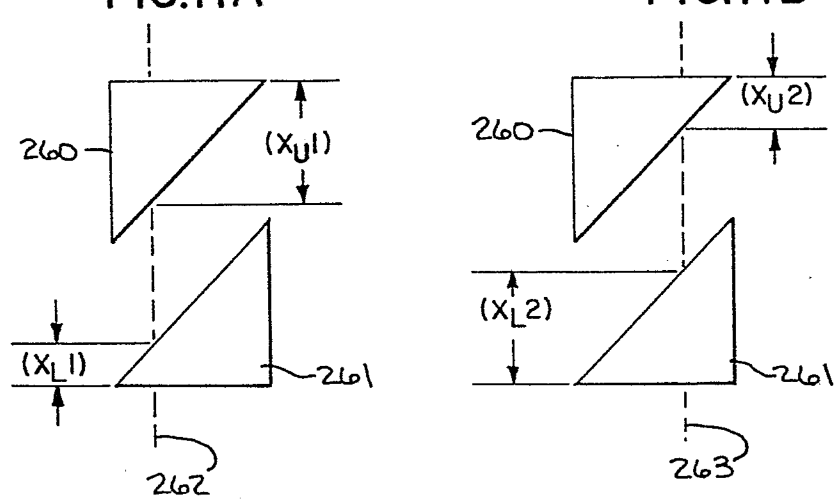


FIG.11A FIG.11B



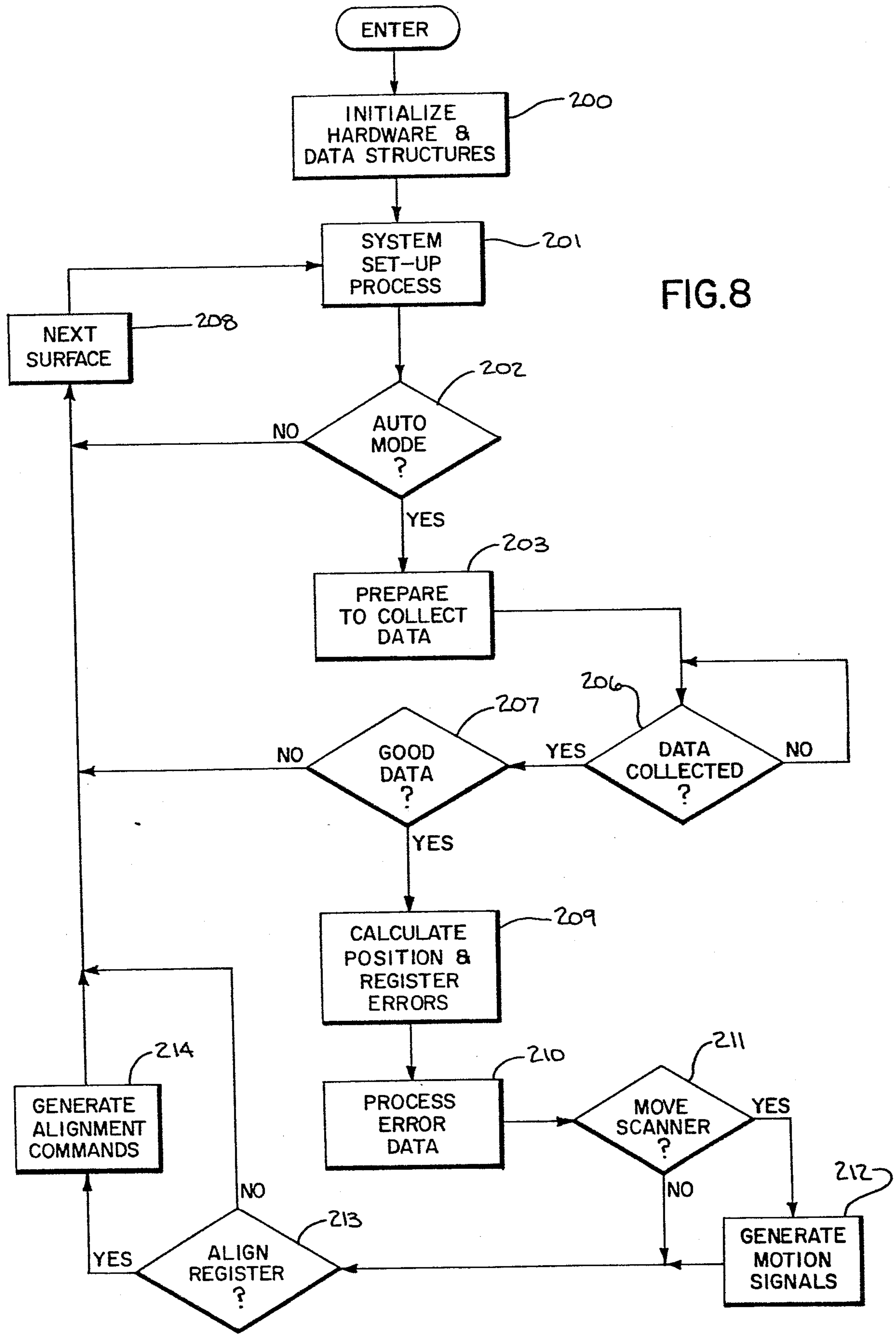

ENTER
INITIALIZE HARDWARE & DATA STRUCTURES
200
SYSTEM SET-UP PROCESS
201
NEXT SURFACE
208
AUTO MODE ?
202
NO
YES
PREPARE TO COLLECT DATA
203
DATA COLLECTED ?
206
YES
NO
GOOD DATA ?
207
NO
YES
CALCULATE POSITION & REGISTER ERRORS
209
PROCESS ERROR DATA
210
MOVE SCANNER ?
211
YES
NO
GENERATE MOTION SIGNALS
212
ALIGN REGISTER ?
213
YES
NO
GENERATE ALIGNMENT COMMANDS
214

FIG.8

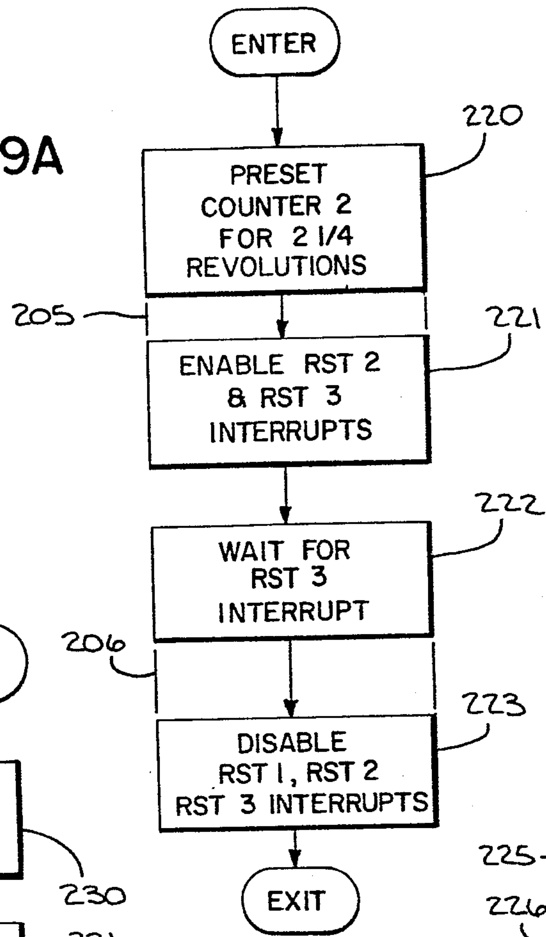


FIG.9A

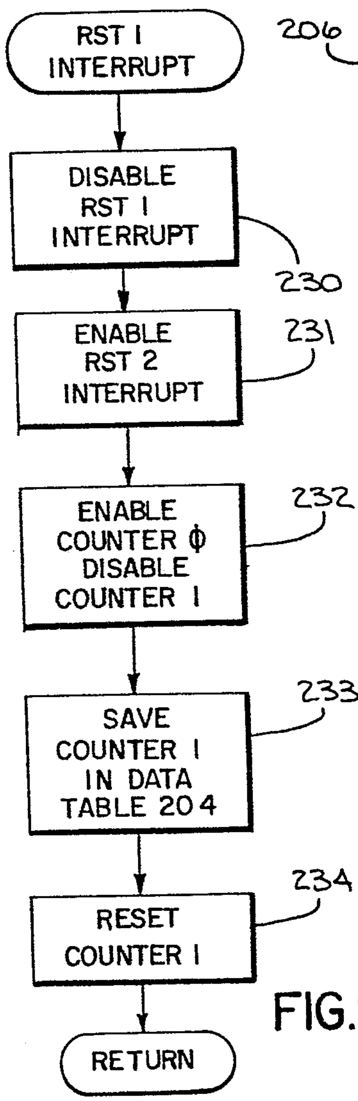


FIG.9B

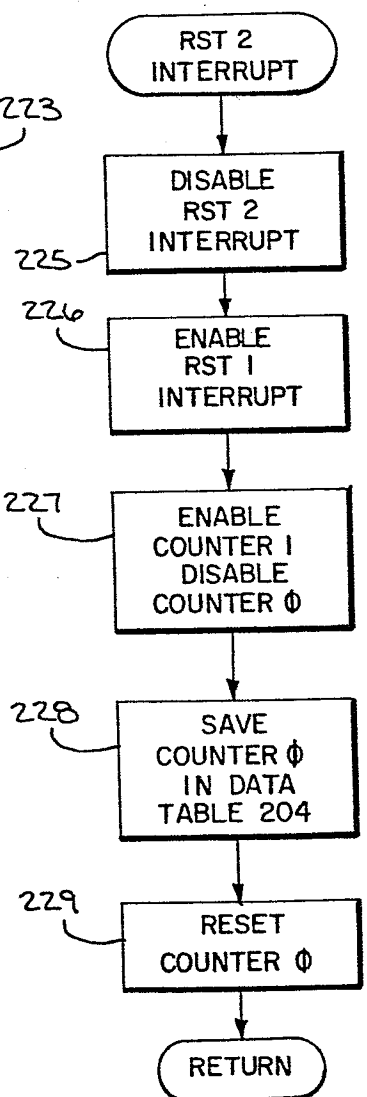
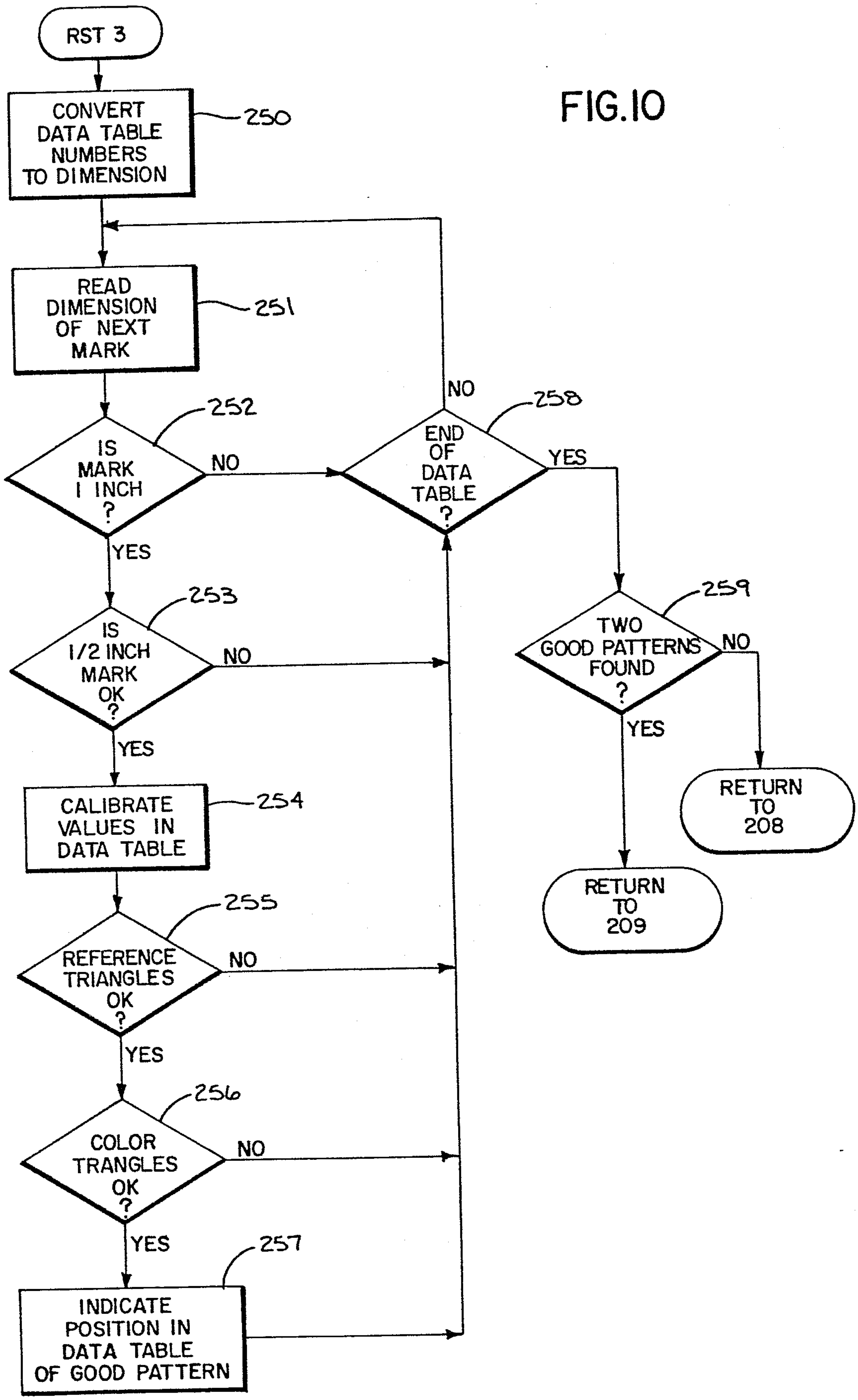


FIG.9C

FIG.10


RST 3
CONVERT DATA TABLE NUMBERS TO DIMENSION
250
READ DIMENSION OF NEXT MARK
251
IS MARK I INCH ?
252
NO
YES
IS 1/2 INCH MARK OK ?
253
NO
YES
CALIBRATE VALUES IN DATA TABLE
254
REFERENCE TRIANGLES OK ?
255
NO
YES
COLOR TRANGLES OK ?
256
NO
YES
INDICATE POSITION IN DATA TABLE OF GOOD PATTERN
257
END OF DATA TABLE ?
258
NO
YES
TWO GOOD PATTERNS FOUND ?
259
NO
YES
RETURN TO 208
RETURN TO 209

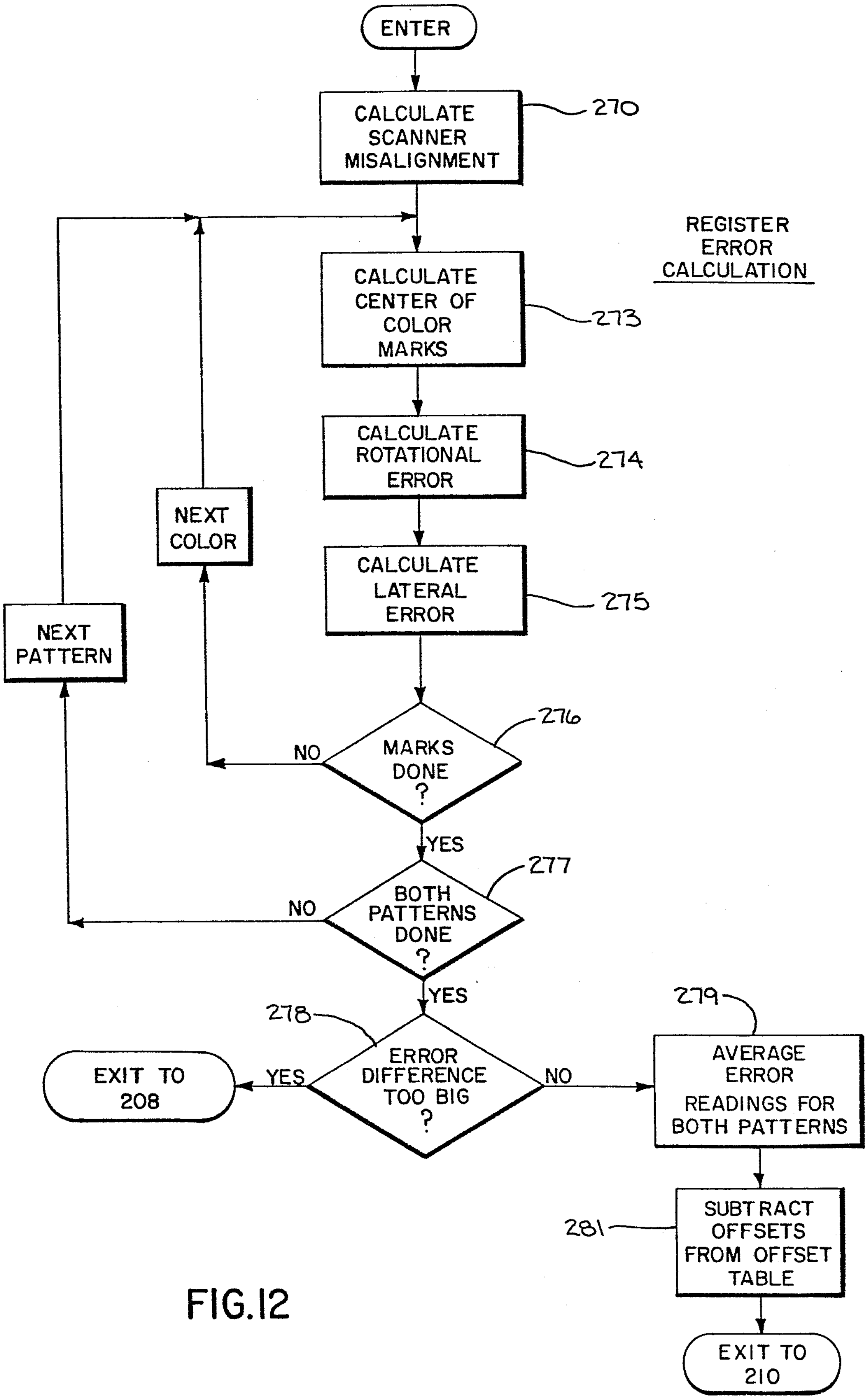

ENTER
CALCULATE SCANNER MISALIGNMENT
270
REGISTER ERROR CALCULATION
CALCULATE CENTER OF COLOR MARKS
273
CALCULATE ROTATIONAL ERROR
274
NEXT COLOR
CALCULATE LATERAL ERROR
275
NEXT PATTERN
MARKS DONE ?
276
NO
YES
BOTH PATTERNS DONE ?
277
NO
YES
278
279
EXIT TO 208
YES
ERROR DIFFERENCE TOO BIG ?
NO
AVERAGE ERROR READINGS FOR BOTH PATTERNS
281
SUBTRACT OFFSETS FROM OFFSET TABLE
EXIT TO 210

FIG.12

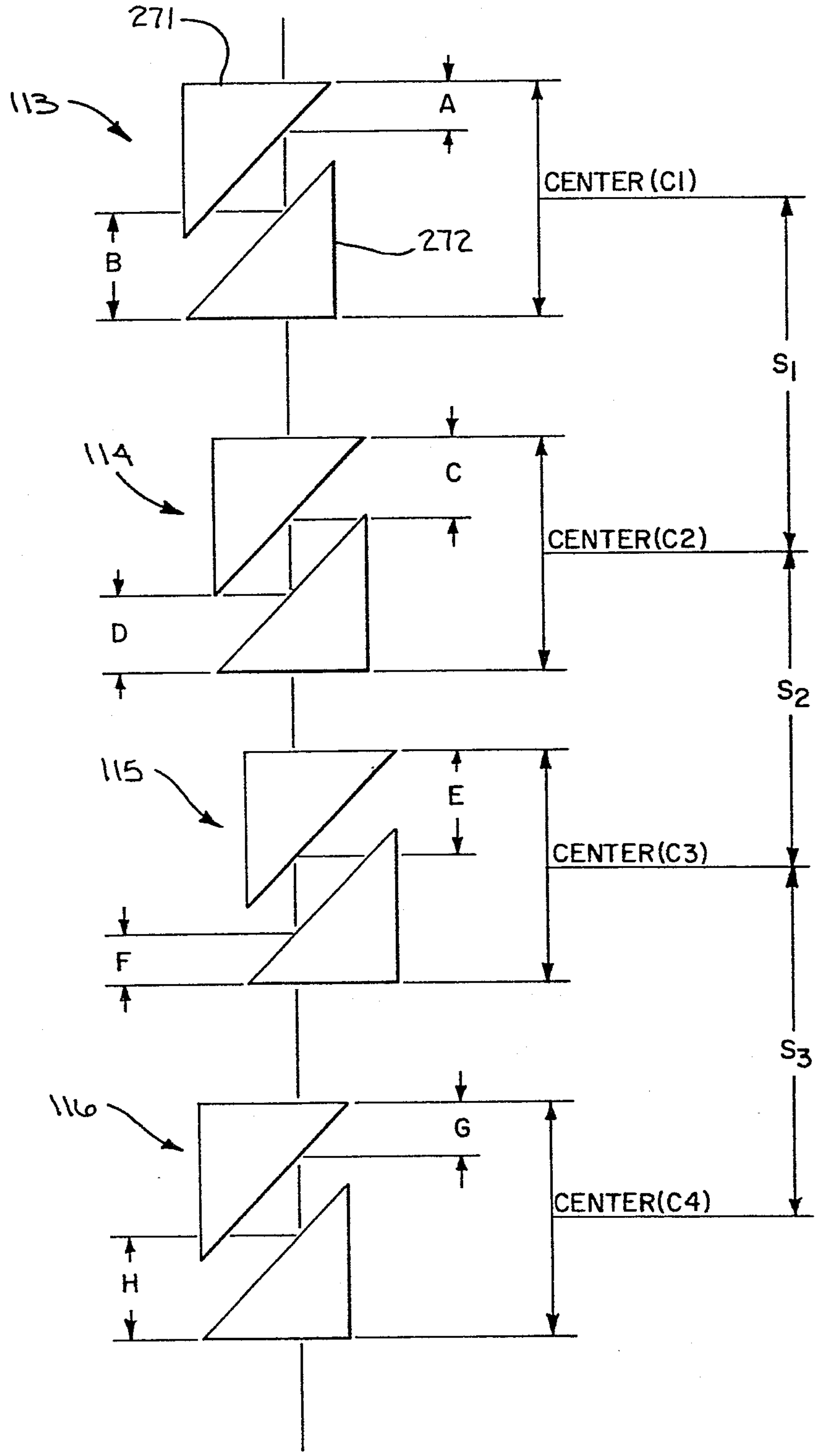
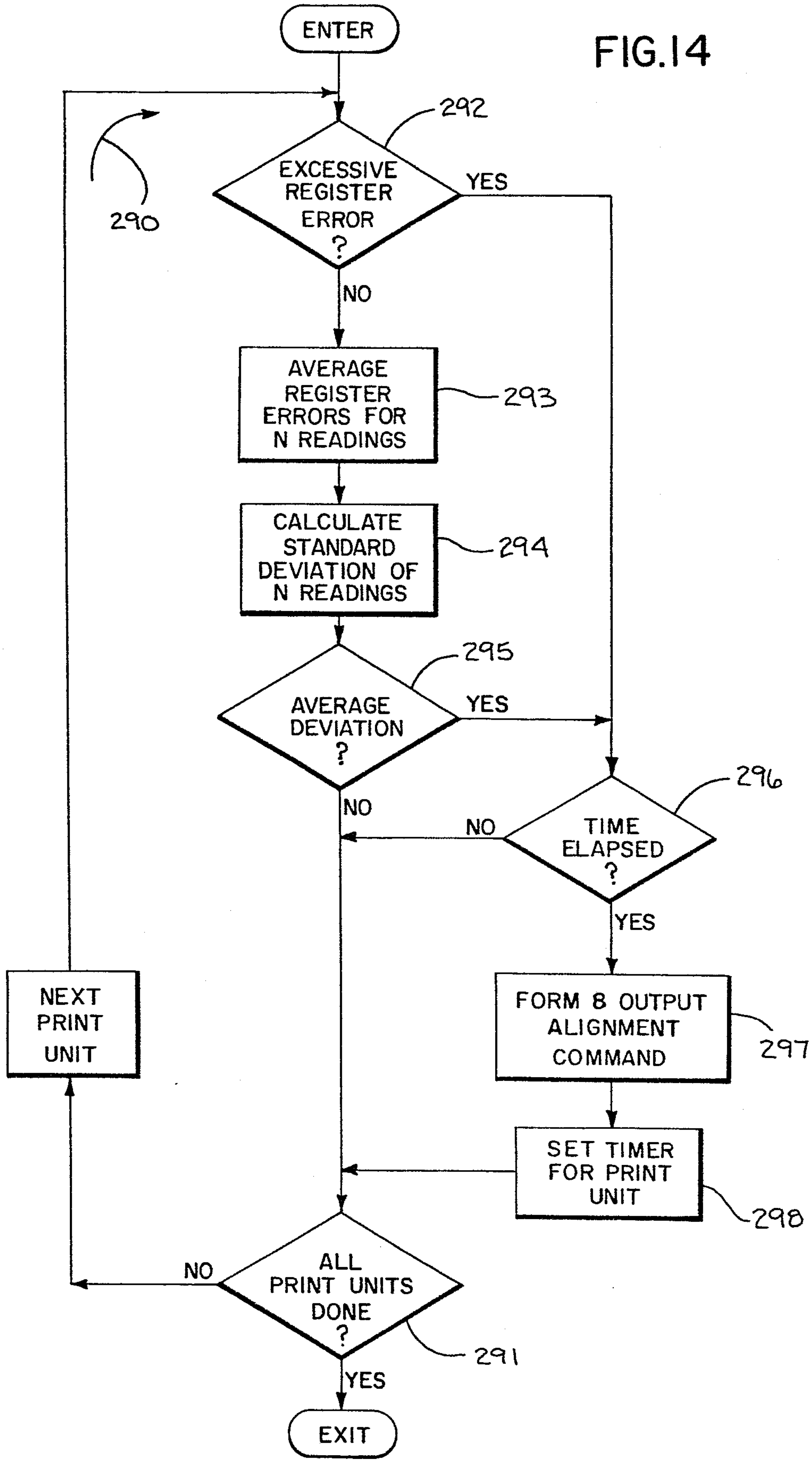

271
113
A
CENTER (C1)
B
272
S1
114
C
CENTER(C2)
D
S2
115
E
CENTER(C3)
F
S3
116
G
CENTER(C4)
H

FIG.13

FIG.14


ENTER
292
290
EXCESSIVE REGISTER ERROR ?
YES
NO
AVERAGE REGISTER ERRORS FOR N READINGS
293
CALCULATE STANDARD DEVIATION OF N READINGS
294
295
AVERAGE DEVIATION ?
YES
NO
296
NO
TIME ELAPSED ?
YES
FORM 8 OUTPUT ALIGNMENT COMMAND
297
NEXT PRINT UNIT
SET TIMER FOR PRINT UNIT
298
NO
ALL PRINT UNITS DONE ?
291
YES
EXIT