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(54) **Burglar alarm system.**

(57) A burglar alarm system includes a number of sensors each of which comprises first and second series-connected resistances and a sensor switch connected in parallel with the first resistance. The sensors are connected in series with one another and are arranged in sets SS1, SS2, where each set contains the same number of sensors and each has the same total resistance. The first resistances of the sensors in a set have values which are different from one another but which are related in a known manner. A sensor switch SC1, SS2 is connected across each set of sensors. A constant current source CS is connected to the series-connected sensors, and the sensor switches SC are opened one at a time by a switch control CC. Output means are provided responsive to the voltage developed across any set of sensors to identify any operated sensor switch.

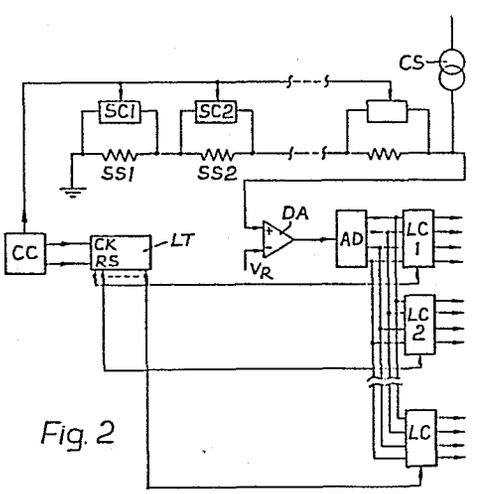

Fig. 2

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BURGLAR ALARM SYSTEM

This invention relates to burglar alarm systems, and particularly to systems of the type described and claimed in my co-pending application No. 82.05783. That application is concerned with a tamper-proof alarm system having a plurality of sensors connected in series. Each sensor comprises first and second series-connected resistors with a sensor switch connected in parallel with the first resistor. Each first resistor in the loop has a value which is different from but related in a known manner to that of every other first resistor. A constant current source supplies a current to the loop, and the identity of any operated sensor can be determined by the associated circuitry. Conveniently, the first resistors may be related in a binary ratio, that is in the ratios 1 : 2 : 4 : 8 : 16 : 32 and so on. However, it is difficult to deal with a large number of sensors as the total loop resistance becomes very high. Even if a binary ratio is not used the same problem arises if each and every operated sensor is to be identified.

It is an object of the present invention to provide a burglar alarm system which may include a large number of sensors and in which each and every operated sensor may be identified.

According to the present invention there is provided a burglar alarm system which includes a plurality of series-connected sensors each comprising a first and second resistances connected in series with one another with a sensor switch connected in parallel with the first resistance, the sensors being arranged in a number of sets each having the same number of sensors and the same total resistance, and the first resistances of the sensors in each set having values which are different from one another but which are related in a known manner, a constant current source connected to the series-connected sensors, switch means connected across each set of sensors, switch control means operable to open the switch means one at a time in a predetermined sequence, and output means responsive to the voltage developed across any one set of sensors to deliver an output indicative of the operation of a sensor switch in the said set.

The invention will now be described with reference to the accompanying drawings, in which :-

Figure 1 shows a schematic circuit diagram of a known alarm system;

Figure 2 is a schematic circuit diagram of a first embodiment of the invention;

Figure 3 is a circuit diagram of part of the arrangement of Figure 2;

Figure 4 shows the control signal waveform used with the circuit of Figure 3;

Figure 5 shows an alternative form of output means; and

Figure 6 illustrates an alternative embodiment of the invention.

Referring now to Figure 1, this shows the main elements of the alarm system described in my copending appliation No. 82.05783. The drawing shows a number of sensors SN1 to SN8, each comprising a first resistance R_A, a second resistance R_B connected in series with resistance R_A, and a sensor switch SW connected across the first resistance R_A. The sensors are connected in series with one another and a constant current source CS is connected to the series-connected sensors. The voltage developed across the series-connected sensors due to the constant current flowing through the resistances is applied to the non-inverting input of a differential amplifier DA. The inverting input of the amplifier is connected to a variable reference voltage V_R, and the output of the amplifier is connected to an eight-bit analogue-to-digital converter AD. The outputs of the converter are connected to suitable indicators such as light-emitting diodes.

In operation, if all the sensor switches SW are of the normally-closed type, then when all switches are closed the resistance in the loop will be the sum of the resistances R_B plus the resistance of the connecting cable. The constant current from the source CS will produce a certain voltage drop due to the loop resistance. The variable reference voltage V_R applied to the amplifier DA is adjusted so as to be equal

to the voltage drop across the loop, so that there is no output from the amplifier DA. The subsequent opening of one or more of the sensor switches SW will increase the loop resistance and hence the voltage drop, producing an output from the amplifier. The first resistances are conveniently related in a binary ratio, as already described, giving identification of each switch which operates.

There is a limit to the number of sensors which may be connected into a loop, since the resistance of the loop rises rapidly as more sensors are added. This makes discrimination between sensors more difficult. The remaining Figures illustrate arrangements which overcome this problem by arranging the sensors in sets, each set containing the same number of sensors and having the same total resistance.

Referring now to Figure 2, this shows a number of sets of sensors connected in series with one another. Each set of sensors is represented by a single resistance SS, but in practice each set comprises a number of sensors connected as in Figure 1. Hence the value of resistor SS1, for example, is the resistance of each resistor R_B and the interconnecting cable making up a set of sensors, assuming the each sensor switch SW is of the normally-closed type as described above. Each of the "equivalent" resistors SS is of the same resistance. Across each set of sensors is connected a normally-closed switch SC. The sets of sensors are connected in series and supplied with current from the a constant source as before. The voltage developed across any one set of sensors is again applied to an amplifier DA where it is offset against a reference voltage. The output of the amplifier is connected to an analogue-to-digital converter AD having a number of outputs equal to the number of sensors in each set of sensors. Each output of the converter AD is connected to a separate latch circuit LC for each set of sensors. Thus if the system has, say, ten sets each of four sensors, the converter AD will have four outputs each of which is connected to ten latch circuits. A control circuit CC is provided which operates the switch SC in sequence so that only one switch is open at a time. When a particular

switch is open the control circuit also activates the latch circuit corresponding to that set of sensors, so that operation of a sensor switch will produce an output from the appropriate latch circuit. A larger number of sets each of more than four sensors may be incorporated.

Figure 3 illustrates one possible form of a switch SC, together with the associated part of the control circuit. The switch itself may conveniently be a VMOS device VM having a low resistance when closed. The gate electrode of the switch VM is connected to one output of a counter CT, say a CD4017, having reset and clock inputs RS and CK respectively. The counter is controlled by a circuit comprising two transistors TR1 and TR2. The base of transistor TR1 is connected through a resistor R1 to a supply line SL, whilst its collector is connected through a resistor R2 to each potential, and to the RS input of counter CT. The emitter of transistor TR1 is connected through a diode D to the base of the other transistor TR2. This has its emitter connected to the supply line SL and its collector connected through a resistor R3 to earth potential and to the CK input of counter CT.

The supply line SL applies both supply voltage and control pulses to the circuit of Figure 4, and has a waveform as shown in Figure 4. The nominal supply voltage is shown, by way of example, as +5 volts. If this falls to +4 volts, then it represents a "reset" pulse, whilst an increase to +6 volts represents a clock pulse. Hence when a switch VM is to be opened, a train of pulses is superimposed on the +5 volts supply as shown in Figure 4. The reset pulse resets are all the counters CT, thus ensuring that all switches V, are in the required state. The subsequent clock pulses cause each counter to advance, and when the clock pulses cease only one counter will have a switch VM connected to its activated output. Each successive train of pulses contains the same number of pulses, and each counter responds to all these pulses. The switch associated with each counter is thus activated only whilst the counter is in the appropriate one of its states, that is once in each pulse train. When any one switch VM is opened the

condition of each sensor switch in that set is detected as before.

The control circuit CC (Figure 2), as well as producing the successive sets of pulses applied to the supply line, also controls a latch counter LT which is reset and clocked at a lower rate, depending upon the number of latch circuits. This counter controls the activation of the latch circuits LC, so that the latch corresponding to a set of sensors is activated when the switch VM across that set of sensors is opened. Hence the operation of each sensor switch is denoted by a different latch output.

In an alternative control arrangement the display of actuated sensors may be simplified from the forty separate indicators provided by the arrangement described above. Figure 5 illustrates the relevant parts of the control system, with the sensor loop omitted. The control circuit and latch counter are provided as before, the latter being connected to a decoder DC which controls a two-digit seven-segment digital display DP. The four outputs of the analogue-to-digital converter AD are each connected to a separate indicator LP. The ten latches of the previous arrangement are no longer required.

In operation, as each set switch SC is opened, the corresponding output of the latch counter LT produces a digital display which identifies the activated set of sensors. Any operated sensor switch causes one or more of the indicators LP to operate.

It will be seen that the system described above allows a large number of sensor switches to be monitored whilst retaining the ability to identify each and every operated sensor switch. Clearly the time-sharing arrangement between the sets of sensors leads to a longer time between operation of a sensor switch and the provision of an alarm indication, but even in a large system this time is still acceptable.

A much simpler arrangement may be employed if only two sets of sensors are present, say up to a total of 18 sensors. As shown in Figure 5, the two sets of sensors are each shunted by a diode, D1 and D2 respectively. The two diodes are

oppositely poled, and the control circuit is required only to reverse the direction of the constant current from the source CS by means of a reversng switch RS. Whatever the direction of current flow, one diode will be reverse biased, acting as an open switch, and the other will be forward biased, acting as a closed switch. Hence reversal of the current flow periodically allows each set of sensors to be checked in turn. Two latch circuits are provided, each being activated in turn as the current flow is reversed.

It will be appreciated that other circuit arrangements may be used to fulfil the same objectives.

The above description and the copending application referred to have made reference to resistor values related by a binary series. It should be appreciated that other non-binary relationships may be used to give the necessary discrimination, though care must be taken to ensure that resistor tolerances do not become too tight. Decoding of the resistor values may require the use of a PROM to identify an operated sensor switch producing a certain change in the loop resistance.

The mode of operation of the system may be changed at any time. For example, the occurrence of an alarm may change the rate of pulsing so that sensors are checked more rapidly. The system may be made to check all sensors in an area adjacent to an operated sensor, and other devices such as television cameras or recorders may be switched on.

The circuit used to provide the control waveform pf Figure 4 has not been described as such circuits are easily devised.

CLAIMS

1. A burglar alarm system which includes a plurality of series-connected sensors each comprising first and second resistances connected in series with one another with a sensor switch connected in parallel with the first resistance, the sensors being arranged in a number of sets each having the same number of sensors and the same total resistance, and the first resistances of the sensors in each set having values which are different from one another but which are related in a known manner, a constant current generator connected to the series-connected sensors, switch means connected across each set of sensors, switch control means operable to open the switch means one at a time in a predetermined sequence, and output means responsive to the voltage developed across any one set of sensors to deliver an output indicative of the operation of any sensor switch in the said set.

2. A system as claimed in claim 1 in which the switch means comprise a separate switch connected across each set of sensors, the switch control means including a separate control for each switch and a central control determining the operation of each separate control.

3. A system as claimed in claim 2 in which each switch comprises a semiconductor switch, each separate control comprising a counter circuit responsive to reset and clock pulses generated by the central control.

4. A system as claimed in claim 1 in which includes two sets of sensors, the switch means comprising two oppositely-poled diodes connected one across each set of sensors, and the switch control means includes means for reversing periodically the direction through the series-connected sensors.

5. A system as claimed in any one of the preceding claims in which the output means includes an analogue-to-digital converter responsive to the voltage developed across an activated set of sensors and having a number of outputs equal to the number of sensors in a set, latch means corresponding one to each set of sensors and activated by the switch control means so as to be activated only when the associated switch means is operated and responsive to the energisation of any output of the said converter, and display means responsive to the outputs of the latch means to identify any activated sensor switch.

6. A system as claimed in any of claims 1 to 4 in which the output means includes an analogue-to-digital converter responsive to the voltage developed across an activated set of sensors and having a number of sensors in a set, counter means controlled by the switch control means, and display means including a digital display responsive to the outputs from the counter means to indicate the identify of the activated set of sensors and means for identifying any activated sensor switch in that set of sensors.

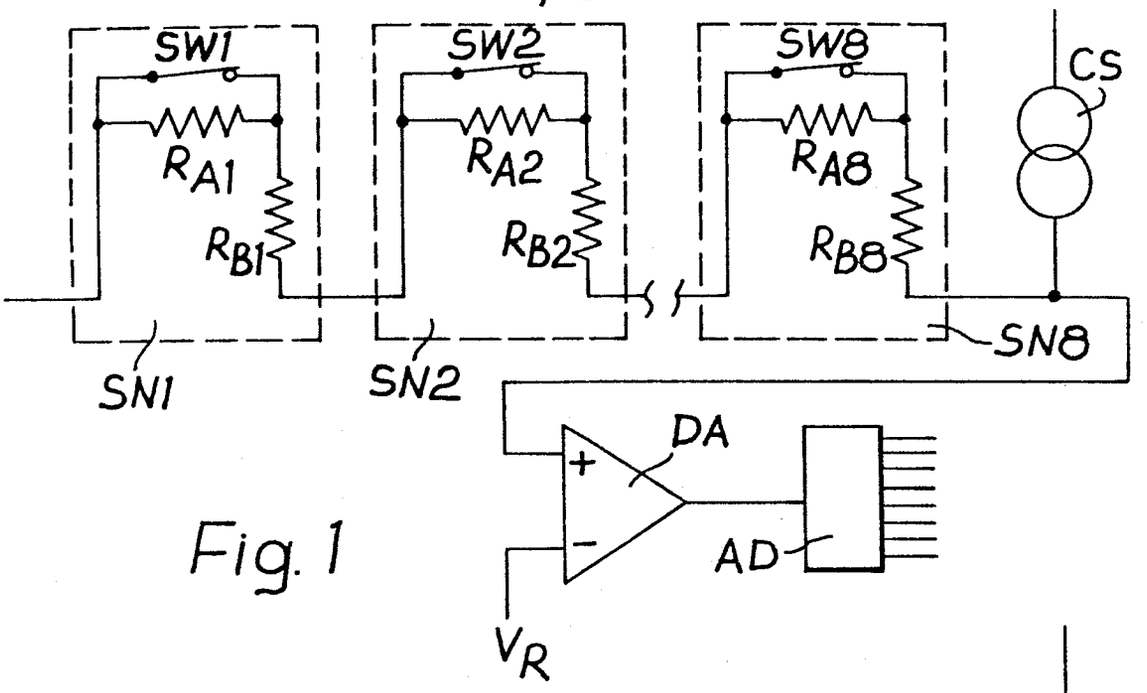
SW1
SW2
SW8
CS
R_{A1}
R_{A2}
R_{A8}
R_{B1}
R_{B2}
R_{B8}
SN1
SN2
SN8
DA
AD
V_R

Fig. 1

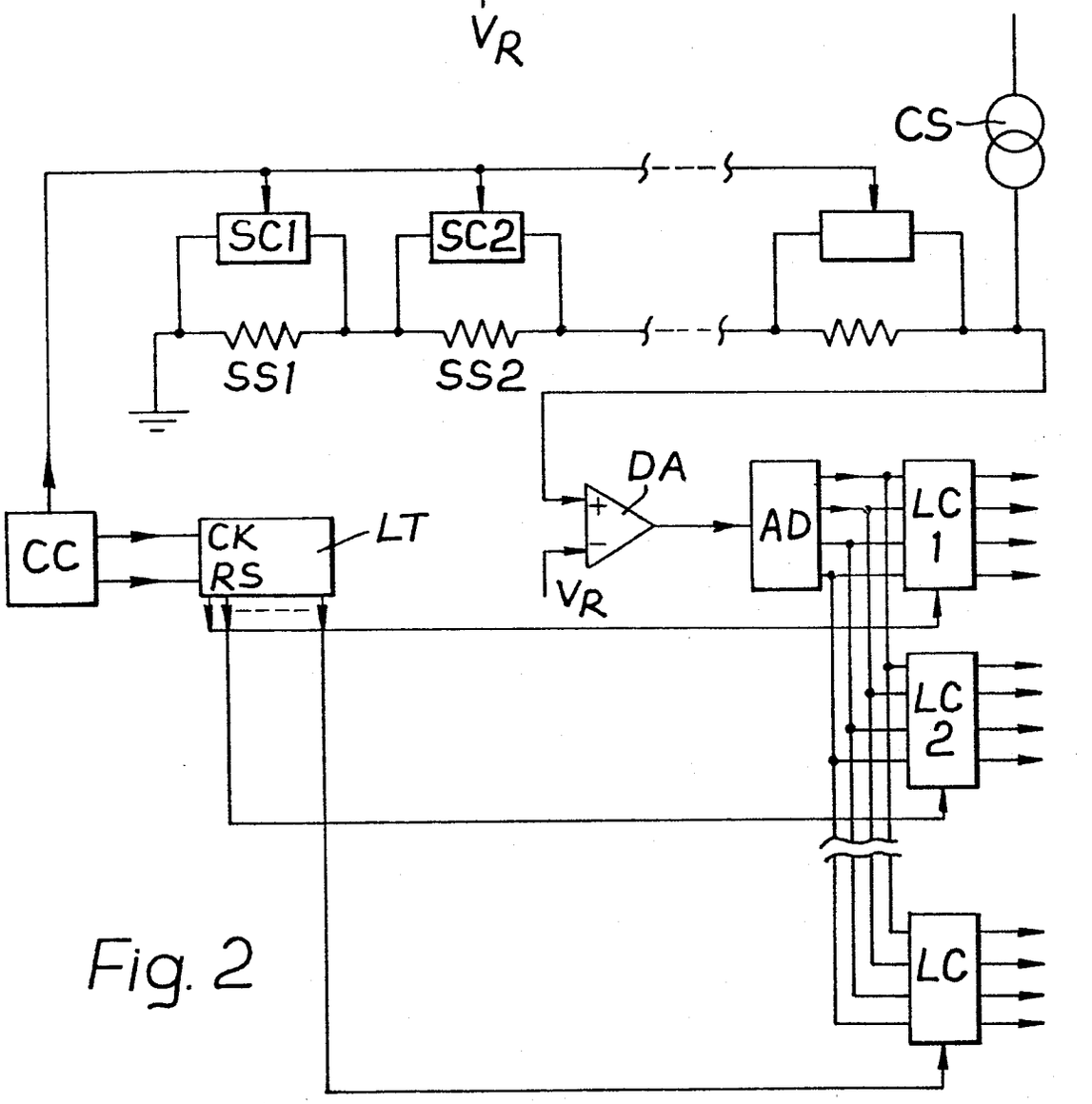
CS
SC1
SC2
SS1
SS2
DA
AD
LC 1
LC 2
LC
CC
CK
RS
LT
V_R

Fig. 2

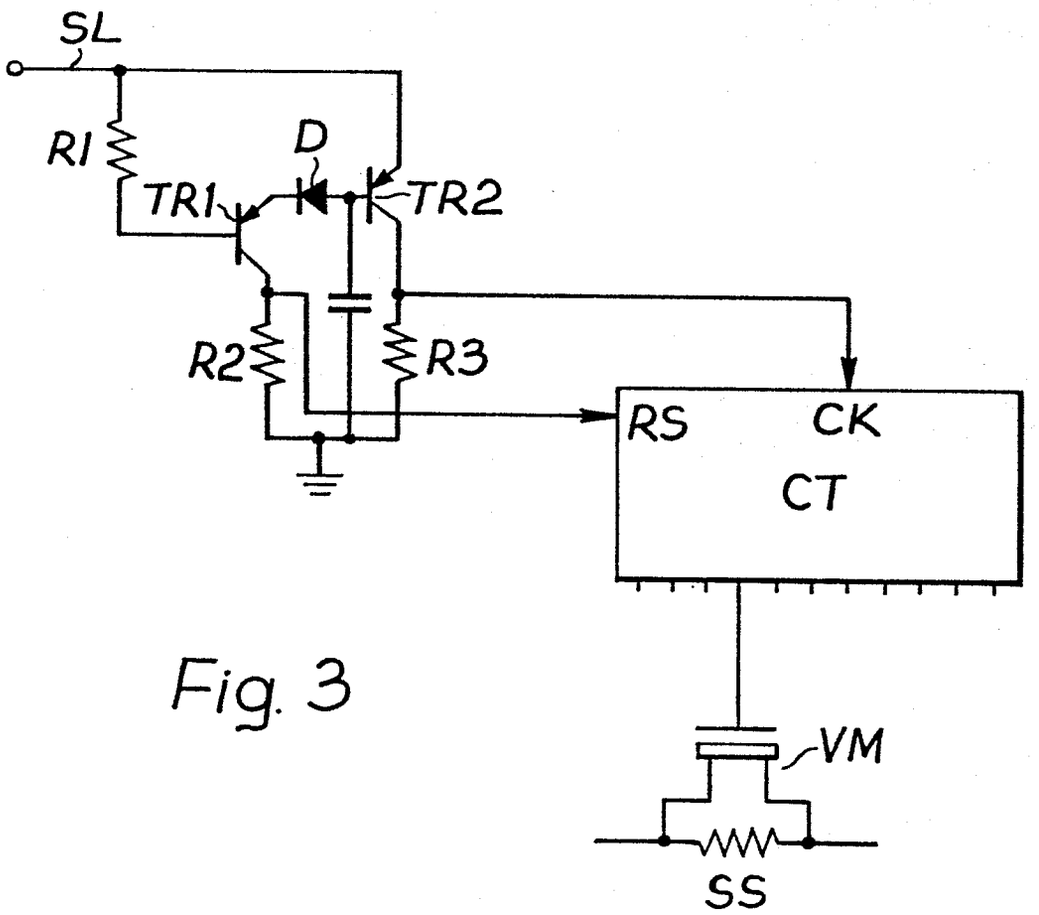

Fig. 3

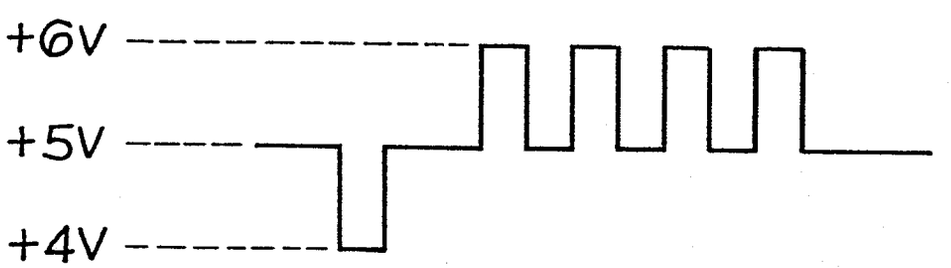

Fig. 4

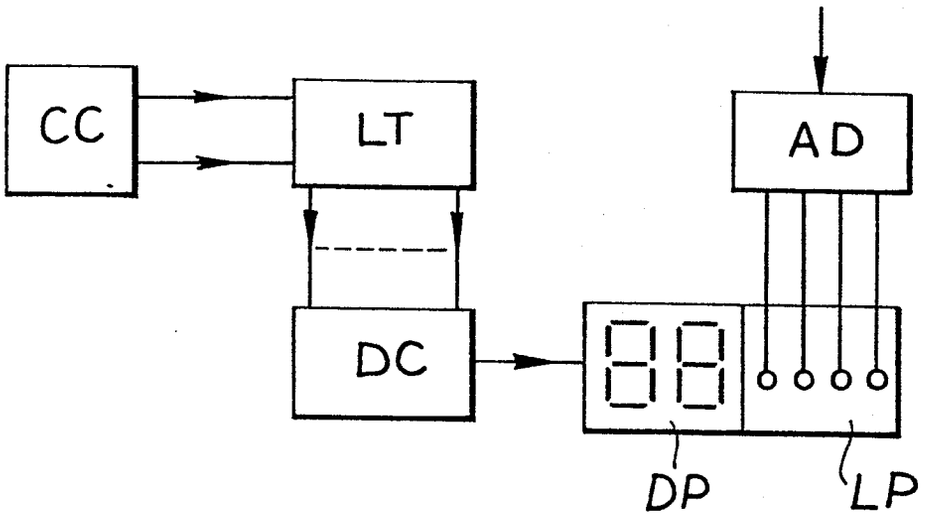

Fig. 5

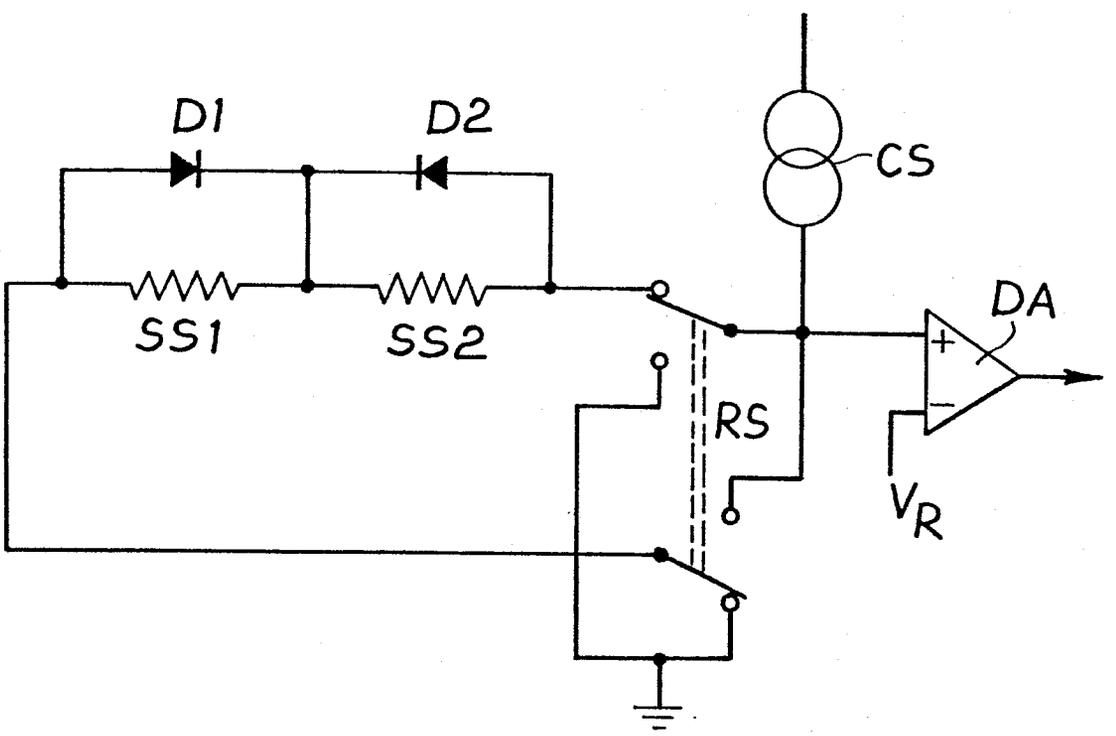

Fig. 6

European Patent Office

EUROPEAN SEARCH REPORT

0125011
Application number

EP 84 30 2290

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
D,P	EP-A-0 088 524 (J.M. MORRISON) * Whole document *	1,5,6	G 08 B 25/00
A	DE-A-2 935 335 (SIEMENS AG) * Page 13, lines 15-17; figure 4; page 10, lines 28-29 *	1	
A	US-A-4 118 700 (T.F. LENIHAN) * Whole document *	1	
A	GB-A-2 032 666 (AMERICAN DISTRICT TELEGRAPH CO.) * Page 1, lines 89-114; page 3, lines 31-65; figures 1, 6 *	1	
A	DE-A-2 239 318 (LEWIS, N. WICKHAM) * Figure 2; claims 16, 17; pages 20, 21 *	1	TECHNICAL FIELDS SEARCHED (Int. Cl. ³) G 08 B G 08 C
A	EP-A-0 052 220 (SIEMENS) * Figure 4; page 8, lines 4-21 *	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	06-07-1984	BEYER F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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