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(54) Data display arrangement with smooth scrolling.

(57) A data display arrangement in which rows of characters are displayed on a CRT, the display information for the characters being provided by stored data which is accessed recurrently for its display in successive scanning fields. Scrolling of the displayed rows of characters is achieved by progressively delaying the start of the addressing of the stored data relative to the start of each scanning field. By using a row mapping memory, the scrolling principle can be extended such that any row of characters can be displayed at any character row position of the display. This, for instance, enables a display not covering the entire screen to be readily centred. Figure 3 shows a block diagram of the scrolling arrangement.

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"IMPROVEMENTS RELATING TO DATA DISPLAY ARRANGEMENTS"

This invention relates to data display arrangements of a type for displaying as an entity on the screen of a CRT (cathode ray tube) or other raster scan display device, a quantity of stored data which is accessed repeatedly for its display in a recurrent cycle of scanning lines which are produced with or without interlaced field scanning.

In a data display arrangement of the above type, the stored data can be in so-called "bit-map" form comprising at least one information bit in respect of each of the pixels or dots which are produced on the screen of the display device by the scanning action. Provided that the information bits for successive dot rows of the display are read out in the same lines of the scanning cycle in each field, the display is a static display.

Alternatively, in a data display arrangement of the above type, the stored data can be in so-called "character based" form. For this alternative, there is stored a library of standard character shapes comprised of patterns of information bits, and the data for display as an entity is in digitally coded form and is used to identify selected character shapes whose information bits are then read out during the scanning action to produce the display. The display is again a static display, provided that the information bits for the successive dot rows occur in the same lines of the scanning cycle in each field.

It is known that a static display as thus produced can be "scrolled" by modifying the read out operation every few fields such that information bits for the dot rows of the display are read in progressively different scanning lines. The displayed data can be cycled/wrapped around if dot rows "lost" at the top of the display are re-inserted at the bottom. However, it is more usual to progressively change the stored data as the scrolling takes place. If the information bits for each dot row are read out in the preceding adjacent scanning line rather than the scanning line in which they were currently being read out, then smooth scrolling occurs because the displayed data is moved (up) only one scanning

line every few fields. The scrolling can be made hard, or less smooth, by reading out the information bits for each dot row for display positions which are not on adjacent scanning lines but which instead are positioned a number of scanning lines apart. Where the stored data is in character based form as mentioned above, this hard scolling can be on a character row basis where a character row is made up to a number of immediately successive dot rows. The speed at which the scrolling (smooth or hard) is effected is determined by how frequently the scanning lines for reading out the information bits for the dot rows are changed.

In a data display arrangement of the type set forth above, presently known scrolling means for effecting either smooth or hard scrolling are relatively inflexible in that they require an offset register in which is stored an offset number which is indicative of the display offset, together with an adder which adds the stored offset number to the scanning line numbers used to read out the information for the dot rows, so as to advance them relative to the actual scanning lines in which the display of the dot rows occurs. The stored offset number is incremented periodically to achieve the scrolling effect.

It is an object of the present invention to provide a scrolling means which dispenses with the need for an adder for incrementing the scanning line offset, and which, moreover, is of greater flexibility.

According to the present invention there is provided in a data display arrangement of the type set forth above a scrolling arrangement by which displayed data can be progressively shifted (vertically) on the screen of the display device, which scrolling arrangement is characterised by comprising a delay count register in which can be stored a delay count number, a logic circuit for modifying said delay count number periodically, a delay counter which is connected to receive the stored count number from said register, and which is also connected to receive a recurrent cycle of scanning line pulses and is operable to produce a start signal after a number of these pulses corresponding to said count number,

and a dot row counter which is connected to receive pulses at the line scan frequency and is operable to produce a dot row address in respect of each received pulse following the application to the dot row counter of said start signal, the dot row addresses being used for the read out of information bits for the dot rows of the display.

In applying a scrolling arrangement according to the invention to a data display arrangement in which the stored data for display is in bit-map form, the dot row counter would arranged to provide a recurrent cycle of dot row addresses having one address for each scanning line in the recurrent cycle of scanning lines.

In applying a scrolling arrangement according to the invention to a data display in which the stored data for display is in character-based form, the dot row counter would be arranged to provide a recurrent cycle of dot row addresses having one address for each scanning line in a group thereof, as required for the display of a row of characters, and the arrangement would further comprise a character row counter connected to be stepped one step for each cycle of dot row addresses, to produce a cycle of character row addresses which pertain respectively to character rows for display in respective groups of scanning lines, the scrolling arrangement further comprising a row map memory which is connected to receive the character row addresses and is operable in accordance with its memory content to map them into different character row addresses which pertain to other character rows, said different character row addresses being used for the selection of stored characters from which information bits are to be read out for the display.

The row map memory is preferably a random access memory the content of which can be modified as required by the logic circuit.

The start of the delay counter operation in each scanning cycle of the display can be controlled by a "field" sync. pulse.

In order that the invention may be more fully understood, reference will now be made by way of example to the accompanying drawings, of which:-

Figures 1 and 2 show diagrammatically respective known forms of scrolling arrangement;

Figure 3 shows diagrammatically a scrolling arrangement conforming to the invention, and

Figure 4 shows diagrammatically a video display terminal having a data display arrangement in which a scrolling arrangement conforming to the invention can be embodied.

Referring to the drawings, the known scrolling arrangement shown in Figure 1 is for a data display arrangement in which the stored display data is in bit-map form in a memory 1. The stored information bits that make up the display data can be considered to be stored as a matrix comprising y bit rows each containing x bits. It is assumed that this size of matrix stores a quantity of data which is to be displayed as an entity. A display device 2 of the arrangement is assumed to be a conventional CRT arranged for 625-line interlaced scanning at 25 fields per second. The display in each field can then be composed of, say, 256 scanning lines L0 to L255. If each of these scanning lines contains 256 pixels or dots, then for the memory 1, $x = 256$ and $y = 256$.

A signal fl of line frequency drives the CRT for each line scan and a signal ff of field frequency drives the CRT for each field scan. A signal fd of dot frequency drives a pulse generator 3 which applies dot pulses to a dot counter 4 having a modulo-256 count. The dot counter 4 produces a recurrent cycle of 256 dot addresses D0-D255 which are used to address the $x = 256$ bit positions in each of the $y = 256$ bit rows of the memory 1. Once per cycle of the counter 4, which occurs at the line frequency fl, a dot pulse is applied to a row counter 5, which also has a modulo-256 cycle, to produce a recurrent count of 256 row addresses R0-R255. The signal ff synchronises the counter 5 with the scanning action of the display device. The arrangement also includes an adder 6, an offset register 7 and a logic circuit 8.

Assuming that an offset number applied to the adder 6 from the register 7 is initially 0, then the row addresses R0-R255 as produced by the row counter 5 will be applied directly to the memory 1 to address the y bit rows in turn, starting from the first

row. As each bit row is being addressed, all of the bit positions thereof are being addressed in turn by the dot addresses D0-D255 to read out the dot information for display by the display device 2. Since the signals fl and ff are used to drive the display device 2, the line and field scans will be in synchronisation with the dot information read-out. Thus, bit rows addressed by row addresses R0-R255 will have their information displayed in scanning lines L0-L255, respectively.

However, when the offset number applied to the adder 6 from the register 7 is not 0, then the number of each row address by which the memory 1 is being addressed at any time no longer corresponds to the scanning line occurring at that time. For instance, if the offset number is 1, then row address R0 (+ 1 = R1) will be used to address the second bit row of the memory 1, and the dot information in this bit row will be read-out and displayed in the first scanning line L0. The third bit row is then read out by row address R1 (+ 1 = R2) and displayed in the second scanning line L1, and so on, with the last bit row being read out by row address R254 (+ 1 = R255) and displayed in scanning line L254. The dot information contained in the first bit row R0 can be read out in the last scanning line L255, or it can be "lost" to leave scanning line L255 blank, or it can be replaced by new dot information which is displayed in scanning line L255. Under the control of the logic circuit 8, the offset number in the offset register 7 will be incremented periodically. Assuming that the offset number is incremented by 1's, then the offset becomes 2 when the first increment occurs. As a result, for the first scanning line L0 the dot information in bit row R0 (+ 2 = R2) is now read out and displayed, for the next scanning line L1 the dot information in bit row R1 (+ 2 = R3) is read out and displayed, and so on. Thus, by incrementing the offset number periodically, the visual effect of scrolling the displayed data is achieved. An offset increment of 1 as described above will produce a smooth scroll, the speed of which is determined by the frequency at which incrementing occurs. For instance, an increment every 5 field scans (i.e. every 100ms) will

result in a slow scroll. It will be apparent that the scrolling can be made less smooth by increasing the offset increment.

The other known scrolling arrangement shown in Figure 2, is for a data display arrangement in which the stored display data is character based. In this instance, the data for display as an entity is in a digitally coded form stored in a display memory 9 and is read out in synchronism with the scanning action of a CRT display device 10, which is driven by line and field frequency signals fl and ff, to address a character memory 11 which contains dot information for a plurality of characters which are available for display. The characters are defined by selected dots of a dot matrix which constitutes a character format for the characters. For instance, the character format can be a 12 x 10 dot matrix comprising 10 dot rows of 12 dots each, with the dot rows being intended for display on groups of 10 scanning lines, each such group having 40 character positions 12 dots wide to form a character row. There may be 24 character rows. The addressing of the memories 9 and 11 for the character display (when there is no scrolling) would be so organised that for each row of characters to be displayed, all the characters of the row are built up scanning line-by-scanning line as a whole one dot row for each character in succession, and the rows of characters are built up in succession. Thus, for the first scanning line in each group (of 10), there would be supplied by the memories 9 and 11 the dot information from the first dot row for the first character of the row of characters, then the dot information from the first dot row for the second character of the row of characters, and so on for the successive characters of the row. For the second scanning line of the group the dot information from the second dot row for each character of the row would be supplied in turn, and so on for the remaining scanning lines of the group.

For the addressing of the memories 9 and 11, there is provided a pulse counting chain comprising a number of counters 12, 13, 14 and 15 which is fed by dot pulses of frequency fd from a pulse generator 16. The first counter 12 is a modulo-12 column counter

which produces column addresses C0 to C11 that are used to address the twelve dot columns of the character matrices in the character memory 11. The counter 13, which receives a stepping pulse once per cycle of the counter 12, is a modulo-40 character counter that produces character position addresses P0 to P39 which identify the 40 character positions of a character row. These addresses are used in conjunction with character row addresses R0' to R23' (to be considered) to read out the character codes from the display memory 9 to address the character matrices in the character memory 11. The counter 14, which receives a stepping pulse once per cycle of the counter 13, is a modulo-10 row counter that produces dot row addresss DR0 to DR9 that correspond to successive groups of ten line scanning pulses of the display device 10. The counter 14 receives the field sync. signal ff to synchronise it with the scanning action of the display device 10. As will be described, the dot row addresses DR0 to DR9 are modified to provide dot row addresses DR0'to DR9' which are used to address the ten bit rows of the character matrices in the character memory 11. The counter 15, which receives a stepping pulse once per cycle of the counter 14, is a modulo-24 row counter that produces character row addresses R0 to R23. These character row addresses are modified (as will be described) to provide the addresses R0' to R23' which correspond to the character rows and, as aforesaid, are applied to the display memory 9. The combination of the character position addresses P0 to P39 and the character row addresses R0' to R23' serve to identify all the digital codes in the display memory 9. The counter 15 is also synchronised by the signal ff with the scanning action of the display device.

In order to produce scrolling of the displayed data, two adders 17 and 18 with respective offset registers 19 and 20 are provided. A logic circuit 21 controls the incrementing of offset numbers in the registers 19 and 20. Because the display is character based and comprises character rows made up of bit rows on respective groups of scanning lines, the offset numbers which are provided for the scrolling function are on a combined bit row/line

and row basis, rather than on a continuous line basis as in Figure 1. A line offset number of from zero to 10 lines can be fed to the adder 17 from the register 19. Assuming, for example, an increment of 1, then the offset number in the register 19 will be incremented by one, 10 times, to progressively scroll a character row into the space occupied by the preceding character row in the display. The incremented dot row addresses DR0' to DR9' are used to address the character memory 11 and once per cycle thereof the row counter 15 is stepped one step to introduce the next character row address to the display memory 9. Alternatively or additionally, the row addresses R0 to R23 can be incremented (to provide the addresses R0' to R023') by the adder 18 in accordance with offset numbers applied from the register 20. It will be apparent that an offset number which is incremented by 1 periodically will scroll the display a character row at a time (i.e. a hard scroll). As in Figure 1, the speed at which the offset numbers are incremented determines the speed at which the display is scrolled. Also, as in Figure 1, the display (character rows) scrolled out of the display at the top can be re-displayed at the bottom or replaced by new display data.

The scrolling arrangement according to the invention shown in Figure 3, is equivalent to that shown in Figure 2 in that it is adapted for scrolling a character based display. For the sake of convenience in description, some circuit elements in Figure 3 have the same reference numbers as the corresponding circuit elements in Figure 2. The arrangement of Figure 3 differs from the arrangement of Figure 2 in that the adders (17, 18) and associated registers (19, 20) have been replaced by a delay counter 22, a delay count register 23 and a row mapping memory 24. The dot row counter 14 is driven, as in Figure 2, to produce the dot row addresses DR0 to DR9. However, the response of the counter 14 is now under the control of a start pulse SP from the delay counter 22. A pulse produced once per cycle of the counter 13 (or equivalently the line frequency signal f1) is applied to the delay counter 22 which is set to count a number of these pulses before producing the start

pulse SP. The setting of the counter 22 is determined by a count number fed to the register 23 by the logic circuit 21. The start of the operation of the counter 14 is therefore in this instance simply delayed for a number of dot row (or scanning line) periods. This count number is progressively incremented in the register 23 by the logic circuit 21 to produce the scrolling effect. Also, as in Figure 2, the counter 15 is stepped one step once per cycle of the counter 14. The character row addresses R0 to R23 are now used to address the mapping memory 24.

In this memory 24 is stored mapping data by which each of the character row addresses R0 to R23 can be "mapped" so as to pertain to any character row. This provides a good degree of flexibility in the addressing of character codes in the display memory 9, so that any row of characters, as stored, can be displayed in any character row on the display device. Thus, not only traditional scrolling, but also other character row positioning can be achieved. One advantage of this is that display data which does not fill the entire display screen can be easily centred. Preferably, the memory 24 is a random access memory, so that the mapping data therein can be varied as required by the logic circuit 21. The broken line 25 signifies this preference

It will be apparent that the invention can also readily be applied to a scrolling arrangement for data stored in bit-map form. For this application, the arrangement of Figure 1 would be modified by replacing the adder 6 and offset register 7, with a delay counter (22) and a delay count register (23). The start of the dot row counter (5) would then be dependent on a start pulse (SP) from the delay counter, as in the arrangement of Figure 3. No mapping memory would be required.

The video display terminal shown diagrammatically in Figure 4 has a data display arrangement in which a scrolling arrangement according to the invention can be embodied. This data display arrangement is for displaying data represented by digital codes, the displayed data being composed of discrete characters the shapes of which are defined by selected dots of a dot matrix which

constitutes a character format for the characters. This video display terminal can be provided in a data display system which is used in conjunction with telephone data services that offer a telephone subscriber having the terminal at his premises the facility of access over the public telephone network to data sources from which data can be selected and transmitted in digitally coded form to the subscriber's premises for display on a television receiver. Examples of such telephone data services are the British and German videotex services Prestel and Bildschirmtext.

The video display terminal comprises a modem 26 by which the terminal has access over a telephone line 27 (e.g. via a switched public telephone network) to a data source 28. A logic and processor circuit 29 provides the signals necessary to establish the telephone connection to the data source 28. The circuit 29 also forms part of a decoder for receiving and processing serial data from the telephone line 27. A command keypad 30 provides user control instructions to the circuit 29. A commmon address/data bus 31 interconnects the circuit 29 with a display memory 32 and a character memory 33. Under the control of the circuit 29, digital codes derived from the serially received data representing characters for display are parallel-loaded onto the data bus 31 and assigned to an appropriate location in the display memory 32. Thereafter, addressing means in the circuit 29 accesses the display data stored in the display memory 32 and uses it to address selectively the character memory 33 to produce character dot information. Shift registers 34 receive this character dot information and use it to drive a colour look-up table 35 to produce therefrom digital colour codes which are applied to a digital-to-analogue converter 36. The output signals from the converter 36 are the R, G, B character generating signals required for driving a television receiver 37 to display on the screen thereof the characters represented by the display data. There is also provided attribute logic 38 which contains control data relating to different display attributes, such as "flashing",

"underlining", and "colour choice". Data which identifies the various attributes to be applied to displayed characters is included in the received data and stored in the display memory 32 along with the character data. The circuit 29 is responsive to the stored attribute data in the display memory 32 to initiate the relevant attribute control by the attribute logic 38, as the characters are displayed, to implement the attribute(s) concerned. A timing circuit 39 provides the timing control for the data display arrangement.

CLAIMS:-

1. In a data display arrangement for displaying as an entity on the screen of a raster scan display device, a quantity of stored data which is accessed repeatedly for its display in a recurrent cycle of scanning lines, a scrolling arrangement by which displayed data can be progressively shifted (vertically) on the screen of the display device, which scrolling arrangement is characterised by comprising a delay count register in which can be stored a delay count number, a logic circuit for modifying said delay count number periodically, a delay counter which is connected to receive the stored count number from said register, and which is also connected to receive a recurrent cycle of scanning line pulses and is operable to produce a start signal after a number of these pulses corresponding to said count number, and a dot row counter which is connected to receive pulses at the line scan frequency and is operable to produce a dot row address in respect of each received pulse following the application to the dot row counter of said start signal, the dot row addresses being used for the read out of information bits for the dot rows of the display.

2. A scrolling arrangement as claimed in Claim 1, in a data display arrangement in which the stored data for display is in bit-map form, characterised in that the dot row counter is arranged to provide a recurrent cycle of dot row addresses having one address for each scanning line in the recurrent cycle of scanning lines.

3. A scrolling arrangement as claimed in Claim 1, in a data display arrangement in which the stored data for display is in character based form, characterised in that the dot row counter is arranged to provide a recurrent cycle of dot row addresses having one address for each scanning line in a group thereof, as required for the display of a row of characters, and the arrangement further comprises a character row counter connected to be stepped one step for each cycle of dot row addresses, to provide a cycle of character row addresses which pertain respectively to character rows for display in respective groups of scanning lines, the

scrolling arrangement further comprising a row map memory which is connected to receive the character row addresses and is operable in accordance with its memory content to map them into different character row addresses which pertain to other character rows, said different character row addresses being used for the selection of stored characters from which information bits are to be read out for the display.

4. A scrolling arrangement as claimed in Claim 3, characterised in that the row map memory is a random access memory the content of which can be modified as required by the logic circuit.

5. A scrolling arrangement as claimed in Claim 3 or Claim 4, characterised in that the character row counter is also connected to receive the start signal from the delay counter.

6. A scrolling arrangement as claimed in any preceding Claim, characterised in that the delay counter operation in each scanning cycle of the display is synchronised by a (field) synchronising signal for the display device.

7. A data display arrangement embodying a scrolling arrangement according to any preceding Claim.

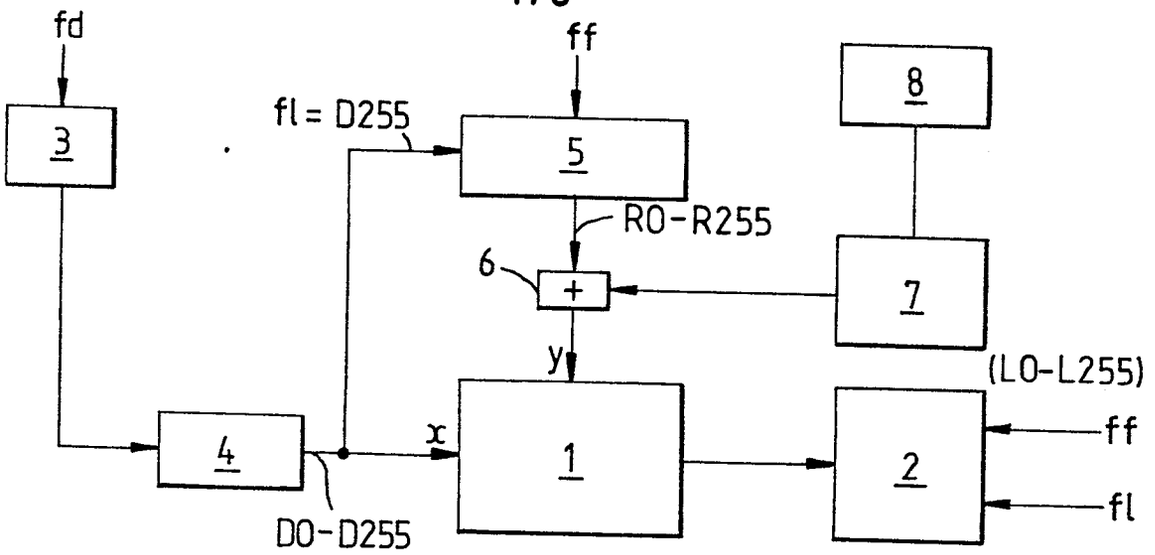

fd
ff
fl = D255
3
5
8
RO-R255
6
+
7
y
(LO-L255)
4
x
1
2
ff
fl
DO-D255

Fig.1.

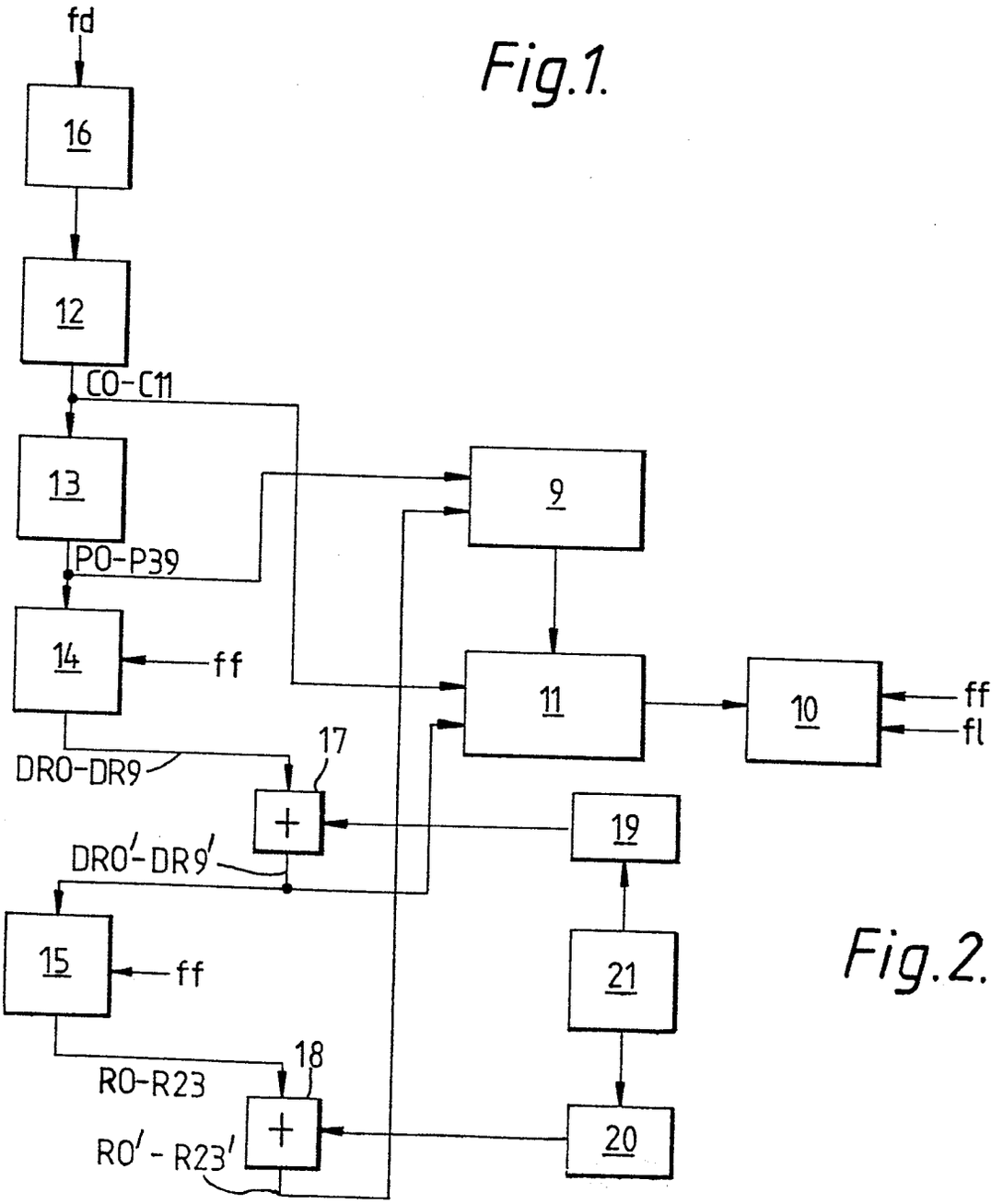
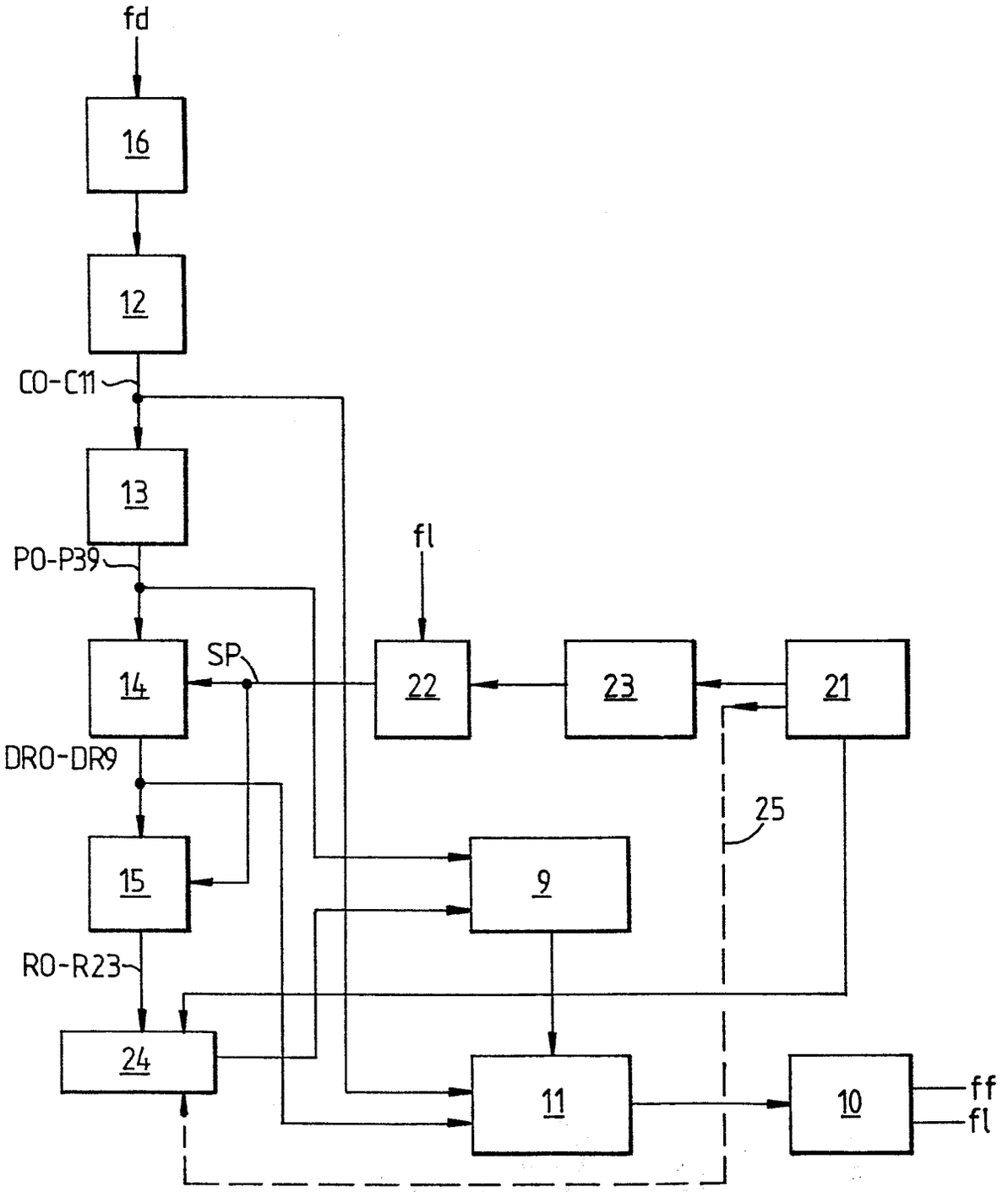

fd
16
12
CO-C11
13
9
PO-P39
14
ff
11
10
ff
fl
17
DRO-DR9
+
19
DRO'-DR9'
15
ff
21
18
RO-R23
+
20
RO' - R23'

Fig.2.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16
12
C0-C11
13
P0-P39
fl
14
SP
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21
DR0-DR9
25
15
9
R0-R23
24
11
10
ff
fl

Fig. 3.

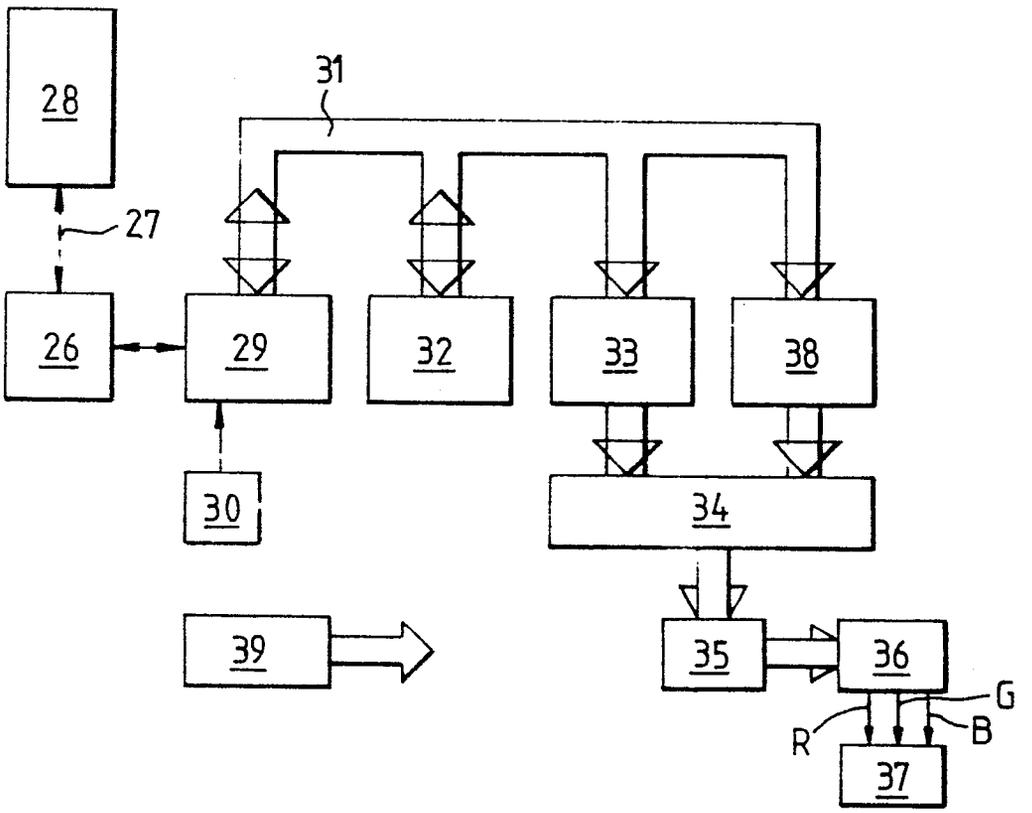

Fig.4.