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(54) Variable dwell I.C. engine ignition system.

(57) A dwell control for an ignition system of the general type including a closed loop control which operates to vary the instant after each spark at which energy storage is commenced for the next spark. At low speeds the closed loop control is overridden and the circuit output (Q44) is operated at constant duty ratio. Switch over between the two modes of operation is effected under the control of a bistable circuit (Q_{18}, Q_{19}) which is set to one state in which a variable timer (C_1, Q_2, Q_3, Q_4) incorporated in the closed loop control determines the instant of energy storage commencement, whenever the time duration for which the energy stored exceeds a threshold in less than a predetermined duration. The bistable is set to its other state, to provide fixed duty cycle operation, whenever the timer period exceeds a limiting value, or when a pulse arrives at the circuit input (Q_1) from a transducer (10) before the expiry of the timer period. This control scheme for the bistable prevents undesirable hunting between the two operating modes.

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VARIABLE DWELL I.C. ENGINE IGNITION SYSTEM

This invention relates to a variable dwell i.c. engine ignition system.

Generally speaking i.c. engine ignition systems operate by building up a store of energy for a period and then releasing the energy quickly to provide a spark. The conventional contact-breaker/coil ignition system utilises a contact breaker driven by the engine to control the flow of current in a coil primary. Energy release is provided by interrupting the coil current at the required instant of ignition. The phase of the ignition sparks is varied mechanically by the contact breaker in accordance with engine parameters such as speed and air intake mainfold pressure and the mechanical arrangement for speed and vacuum timing control have become very sophisticated over a long period of development.

More recently there have been many proposals for controlling the timing of the ignition sparks electronically and in such proposals, mechanical vacuum and speed timing control is unnecessary. However, there exists a demand for hybrid systems in which timing control is effected mechanically, but electronic circuits control the actual coil current. Thus, for example, the conventional contact breaker may be replaced by a transducer which is driven by the engine and which incorporates conventional speed and vacuum timing controls. Such a transducer may be, for example, one relying on variable reluctance, on Hall effect, or on other "non-contact" switching arrangements, the transducer providing a pulse train of constant duty ratio with the "trailing edges" of the pulses marking

the desired instants of ignition. Clearly, such a transducer simulates the conventional contact breaker, but avoids its mechanical problems such as contact bounce, wear, contact erosion, etc.

Because of the fixed duty ratio of the transducer pulse train, if the "leading edge" of each pulse is used to turn the coil current on, (as with a conventional contact breaker system) the coil on-time will be a fixed proportion of the cycle time and hence will reduce as speed increases. This involves making a compromise between very inefficient operation at low speed and an inadequate on-time at high speeds. To overcome this problem it has already been proposed, e.g. in UK-A-2113761 to vary the coil duty ratio in accordance with the duration of the interval between the transducer pulses so as to increase the fractional coil on-time as speed increases. A closed-loop correction system was employed to provide a relatively slow correction to maintain the proportion of each cycle for which the coil current was above a set level substantially constant in steady running.

The previously proposed apparatus was found to be too sensitive to the jitter which was found to occur when a chain drive from the engine to the transducer was used, particularly if the chain was improperly tensioned.

It is an object of the present invention to provide a variable dwell i.c. engine ignition spark ignition system which can operate satisfactorily when in the presence of substantial timing jitter and which also is relatively insensitive to supply voltage variations.

In accordance with the invention there is provided a dwell control for an ignition system employing a

transducer driven by the engine and producing a pulse train of approximately constant duty ratio and including mechanical means for varying the phase of the pulse train relative to the engine cycle in accordance with engine operating conditions, energy storage means controlled by said transducer for releasing energy to create ignition sparks in synchronism with specific events in said pulse train, means sensitive to different specific events in said pulse train for commencing an energy storage period in each ignition cycle at relatively low engine speeds, timer means operating at relatively high engine speeds and operating under the control of said transducer to commence said energy storage period at an instant in each cycle earlier than said different specific event, the timing period of said timer being determined by closed loop control means so as to regulate the fractional time during which the energy stored by said energy storage means exceeds a threshold value, characterised by mode selection bistable switch means for determining whether or not said timer or said different specific event is to cause commencement of said energy storage period, said bistable switch means being switched to a state in which said timer causes commencement of said energy storage period whenever the time duration for which the energy stored by said energy storage means exceeds a threshold value is less than a predetermined duration and to its other state in which said different specific events cause commencement of the energy storage period either when timing period of the timer exceeds a limiting value or when said different specific event occurs before expiry of the timing period of said timer.

Where the energy storage means is a coil, the energy storage period is commenced by completing a path for

coil current and, in this case, the closed loop control means senses the coil current and determines the timer timing period so that the coil current is above a threshold level for a predetermined proportion of the cycle duration.

The accompanying drawing is an electrical circuit diagram of one example of a variable dwell i.c. engine ignition system in accordance with the invention.

The system shown includes a transducer 10 which senses the angular position of a conventional mechanically timed ignition distributor. The transducer may be a Hall-effect device, a variable reluctance device or any other known "no-contact" device which provides, in well known manner, a pulse train of fixed duty ratio and with the trailing edges of the pulses in the pulse train coinciding with the desired instants of sparks. Since transducers of this type are generally known no further description is given herein. The transducer is designed, in the present case, to provide a duty ratio of about 15%.

The output of the transducer 10 is connected by a pull-up resistor R_1 to a supply rail 11 to which a regulated voltage is applied by a known regulator circuit 12. The transducer output is also connected by a resistor R_2 to the base of an npn transistor Q1, which has its emitter connected to a ground rail 13, so that transistor Q_1 is conductive whenever the output of the transducer 10 is high. A resistor R_3 connects the base of transistor Q_1 to the ground rail 13. The collector of the transistor Q_1 is connected to the cathodes of two diodes D_1 and D_2. The anode of diode D_1 is connected to one side of a capacitor C_1, the other side of which is connected to the collector of a pnp

transistor Q_2 which has its base connected to a bias voltage source V_1 and its emitter connected by a resistor R_4 to the rail 11. The emitter of the transistor Q_2 is also connected by a resistor R_5 to the collector of a pnp transistor Q_3 which has its emitter connected to rail 11 and its base connected to the collector of an npn transistor Q_4, the emitter of which is connected by a resistor R_6 to the ground rail 13 and the base of which is connected to said other side of the capacitor C_1. the anode of the diode D_2 is connected to the rail 11 by a resistor R_7.

Another diode D_3 has its anode connected to the anode of diode D_2 and its cathode connected by a resistor R_8 to rail 13. The cathode of diode D_3 is connected to the base of an npn transistor Q5, the collector of which is connected by two resistors R_9, R_{10} in series to the rail 11. The emitter of the transistor Q_5 is connected to the collector of an npn transistor Q_6 the emitter of which is connected to the junction of two resistors R_{11} and R_{12} in series between rails 11 and 13. The base of transistor Q_6 is connected by a resistor R_{13} to said other side of capacitor C_1.

The anode of the diode D_1 is connected to the emitters of two pnp transistors Q_7 and Q_8. Transistor Q_7 has its base connected to the bias voltage source V_1 and its collector connected by a resistor R_{14} to rail 13. An npn transistor Q_9 has its base connected to the collector of transistor Q_7, and its emitter grounded to rail 13. The emitter of transistor Q_8 is connected by a constant current source S_1 to the rail 11 and its collector is grounded to rail 13. the base of transistor Q_8 is connected by another current source S_2 to rail 11 and to the emitter of a pnp transistor Q_{10}. The collector of transistor Q_{10} is connected to the

collector of transistor Q_8 and to rail 13 and its base is connected to the collectors of an npn transistor Q_{11} and a pnp transistor Q_{12}. Transistor Q_{11} has its base connected to another bias voltage source V_2 and its emitter grounded to rail 13 via a resistor R_{15}. The transistor Q_{12} has its base connected to the bias voltage source V_1 and its emitter connected by a resistor R_{16} to the rail 11. The base of transistor Q_{10} is also connected by a resistor R_{17} and a capacitor C_2 in series to the rail 11. The base of transistor Q_{10} is also connected to the cathode of a diode D_4, the anode of which is connected by a resistor R_{18} to the rail 11. Anode of diode D_4 is also connected to the anode of a diode D_5, the cathode of which is connected to the transducer output, and to the collector of an npn transistor Q_{13} which has its emitter grounded to rail 13.

A pnp transistor Q_{14} has its emitter connected to that of transistor Q_{12} and its collector connected to the emitter of transistor Q_{11}. The base of transistor Q_{14} is connected by a resistor R_{19} to rail 11 and by a resistor R_{20} to the collector of transistor Q_1, so that transistor Q_{14} turns on whenever transistor Q_1 is conductive and so directly connects the emitters of transistors Q_{11}, Q_{12} together.

The emitter of transistor Q_{12} is also connected to the anode of a diode D_6, the cathode of which is connected to the collector a pnp transistor Q_{16} and to ground via a current sink S_3. The emitter of transistor Q_{16} is connected to rail 11 and a resistor R_{21} connects the base of transistor Q_{16} to that rail. The base of transistor Q_{16} is also connected to the collector of an npn transistor Q_{15}, the emitter of which is connected to the emitter of transistor Q_{11} and the base of which is grounded via a resistor R_{22}. A resistor R_{23} connects

the base of transistor Q_{15} to the anode of a diode D_7, the cathode of which is connected to ground by a resistor R_{24}. The emitter of an npn transistor Q_{17} is connected to the cathode of diode D_7 and the base of transistor Q_{17} is connected to the junction of two resistors R_{25}, R_{26} connected in series between the rails 11, and 13.

An npn transistor Q_{18} has its emitter connected to rail 13 and its collector connected by two resistors R_{27}, R_{28} in series to rail 11. The junction of these resistors R_{27}, R_{28} is connected to the base of a pnp transistor Q_{19}, the emitter of which is connected to rail 11 and the collector of which is connected by three resistors R_{70}, R_{29}, R_{30} in series to rail 13, with the junction of resistors R_{29}, R_{30} connected to the base of transistor Q_{18}. Transistor Q_{18}, Q_{19} form a bistable switch, turned on as hereafter explained by turning on transistor Q_{19} and turned off, as also explained by turning off transistor Q_{18}. The collector of the transistor Q_{19} is also connected via a resistor R_{31} to the base of transistor Q_{13}, and by a resistor R_{32} to the anode of a diode D_8, the cathode of which is connected to the base of the transistor Q_5. The collector of transistor Q_9 is connected to the junction of resistors R_{70} and R_{29} so that when transistor Q_{19} turns on it sinks any current being passed by transistor Q_{19} and causes transistor Q_{18} to turn off.

An npn transistor Q_{20} has its collector connected to the junction of resistor R_{17} and capacitor C_2, its base connected to the bias voltage source V_2 and its emitter connected by a resistor R_3 to the collector of another npn transistor Q_{21}, the emitter of which is grounded to rail 13. A diode D_9 has its anode connected to the collector of the transistor Q_{19} and its cathode

connected to the junction of resistors R_{70} and R_{29}. Transistor Q_{21} has its base connected to the junction of two resistors R_{33}, R_{34} connected in series between the collector of a pnp transistor Q_{22} and rail 11. Transistor Q_{22} has its emitter connected to the base of a pnp transistor Q_{23}, the emitter of which is connected to rail 11. The base of transistor Q_{22} is connected to the junction of two resistors R_{35} and R_{36} which are in series between the rail 11 and the output of the transducer 10. The junction of these two resistors R_{35} and R_{36} is also connected to the collector of a pnp transistor Q_{24} which has its emitter connected to rail 11 and its base connected to the collector of transistor Q_{23} which is also connected to ground by a resistor R_{37}.

An npn transistor Q_{25} has its emitter grounded to rail 11 and its collector connected to the collector of transistor Q_9. The base of transistor Q_{25} is connected to rail 13 by a resistor R_{38} and also to the collector of a pnp transistor Q_{26}. Transistor Q_{26} has its base connected by a resistor R_{39} to rail 13, and by two resistors R_{40}, R_{41} in series to rail 11. The junction of resistors R_{40}, R_{41} is connected to the anode of a diode D_9, the cathode of which is connected to rail 13 by a current sink S_4. An npn transistor Q_{27} has its emitter connected to that of transistor Q_{26} and by a resistor R_{42} to rail 11 and its collector connected by a resistor R_{43} to the rail 13. A transistor Q_{28} has its base connected to the collector of the transistor Q_{27}, its emitter grounded to rail 13 and its collector connected to the base of the transistor Q_{27}. A current sink S_5 also connectes the base of transistor Q_{27} to ground rail 11.

A capacitor C_3 is connected at one side to the base of

transistor Q_{27} and at the other side to the anode of a diode D_{10} the cathode of which is connected to the cathode of diode D_9. These two cathodes are connected to the collector of a pnp transistor Q_{29} which has its emitter connected to rail 11, and its base connected by a resistor R_{44} to rail 11, by a resistor R_{45} to the collector of transistor Q_{17} and by a resistor R_{46} to the anode of a diode D_{11}, the cathode of which is connected to the collector of the transistor Q_{20}. The anode of diode D_{10} is connected to ground rail 11 by a current sink S_6, to the base of a pnp transistor Q_{30} and to the collector of a pnp transistor Q_{31}. Transistor Q_{31} has its emitter connected to rail 11 and its base connected by a resistor R_{47} to the rail 11.

The collector of transistor Q_{30} is connected by a current sink S_7 to rail 13 and its emitter is connected by a resistor R_{48} to rail 11. The collector of transistor Q_{30} is also connected to the base of an npn transistor Q_{32}, the emitter of which is grounded to rail 13 and the collector of which is connected by a resistor R_{50} to the emitter of the transistor Q_{30}. An npn transistor Q_{33} has its base and emitter connected to the collector of transistor Q_{32} and its emitter connected by a resistor R_{51} to ground.

An npn transistor Q_{34} has its base connected to the junction of two resistors R_{52}, R_{53} in series between collector of a pnp transistor Q_{35} and rail 13. Transistor Q_{35} has its emitter connected to rail 11 and its base connected to the junction of the resistors R_9 and R_{10}. The emitter of transistor Q_{34} is connected to rail 13 and its collector is connected by a resistor R_{54} to rail 11 and by a resistor R_{55} to the base of an npn transistor Q_{36}, which has emitter grounded to rail 13. Transistor Q_{36} has its collecter connected by two

resistors R_{56}, R_{57} in series to rail 11, and by another two resistors R_{58}, R_{59} in series to the rail 11. The junction of the latter two resistors is connected to the cathode of a diode D_{12}, the anode of which is connected to the base of the transistor Q_{23}. The junction of the two resistors R_{56}, R_{57} is connected to the base of a pnp transistor Q_{37} which has its emitter connected by a resistor R_{60} to rail 11 and its collector connected by a resistor R_{61} to rail 13. the collector of the transistor Q_{37} is also connected by a capacitor C_4 and two resistors R_{62}, R_{63} in series to the rail 13, the junction of these resistors being connected to the base of an npn transistor Q_{38}, the emitter of which is connected to the base of the transistor Q_{36} and the collector of which is connected by a resistor R_{64} to the base of the transistor Q_{19}.

The emitter of transistor Q_{37} is connected to the base of a pnp transistor Q_{39}, the emitter of which is connected to rail 11 and the collector of which is connected by a resistor R_{65} to the collector of an npn transistor Q_{40}, the base of which is connected to the collector and base of the transistor Q_{33}. The collector of transistor Q_{39} is also connected to the base of a pnp transistor Q_{41}, which has its emitter connected to rail 11 by a current source S_8, and its collector connected by a resistor R_{66} to the anode of a diode D_{13}, the cathode of which is connected to the collector of a transistor Q_{40}. The emitter of transistor Q_{41} is connected to the base of a pnp transistor Q_{42} which has its emitter connected to rail 11 and its collector connected by a current sink S_9 to rail 13. The collector of transistor Q_{42} is connected to the base of an npn transistor Q_{43}, which has its collector connected to rail 11 and its emitter connected by two resistors R_{67}, R_{68} in series to rail 13. The junction

of resistors R_{67}, R_{68} is connected to the base of an npn integrated Darlington type output transistor Q_{44} which has its emitter connected to rail 13 by a current sensing resistor R_{69} and its collector connected via the ignition coil primary winding 14 to the raw supply 15. The emitter of transistor Q_{40} is connected to the emitter of transistor Q_{44} so that transistor Q_{40} starts to turn off whenever the voltage across resistor R_{69} rises to that across resistor R_{51}.

A pnp transistor Q_{45} has its emitter connected to rail 11, its base connected to the junction of two resistors R_{72}, R_{71} in series between the emitter of transistor Q_{43} and rail 11, and its collector connected to the anode of diode D_7.

In operation transistor Q_1 operates to invert the negative-going output pulses from the transducer 10. Thus following each transducer pulse capacitor C_1 has the potential of its said one side pulled down to approximately one diode voltage drop above ground, cutting off transistors Q_8 and Q_6 in consequence. At low and medium speeds this has the effect of cutting off transistors Q_3 and Q_4 and capacitor C_1 subsequently discharges linearly via transistor Q_2 acting as a constant current source, until transistor Q_4 turns on, whereupon transistor Q_3 shunts the emitter resistor R_4 of transistor Q_2. This increases the charging rate of capacitor C_1, which charges up by about 1 volt more, after which its "other side" becomes clamped when transistor Q_6 turns on, at which point the timer constituted by the capacitor C_1 and various transistors controlling its charge, has timed out. During the transducer pulse, the potential of the "other side" of capacitor C_1 remains clamped whilst that of the "one side" rises until clamped by transistor Q_8 which forms part of a Darlington voltage

follower driven by the voltage on capacitor C_2. This voltage therefore controls the delay between the transducer pulse trailing edge and the turning on of the transistor Q_6, this delay increasing in response to increases in the control voltage. At sufficiently low values of the control voltage, the potential of the "other side" of capacitor C_1, is not lowered sufficiently to turn off transistor Q_4; hence the augmented charging rate provided by transistor Q_3 is operative throughout the timer's action. This enables the coil off time to be controlled over a sufficiently wide range of non-zero values.

Under normal operating conditions of the timer transistor Q_7 is non-conductive. During dwell control operation (to be described hereinafter) however, when the voltage across capacitor C_2 approaches the value at which maximum time delay is produced, transistors Q_7 and Q_9 turn on to provide detection of a "timer outranged" condition.

When transistor Q_{13} is conductive (ie in a timer controlled turn on condition), diode D_4 is non-conductive, and the voltage on capacitor C_2 is controlled by transistors Q_{11} and Q_{12}. Both of these are held off by transistor Q_{14} except during the transducer pulses. Transistor Q_{12} is held off unless transistor Q_{16} is saturated, i.e. unless transistor Q_{15} is on. This condition is met during transducer pulses only if the current limit (to be explained hereinafter) is in control; hence transistor Q_{12} acting as a constant current source is turned on only when the current limit is in control during transducer pulses. Transistor Q_{11}, which acts as a constant current sink, is held off when transistor Q_{15} is conducting, so that it is operative only when the current limit is not in control during transducer pulses.

The magnitudes of the sink and source currents have a ratio of about 2:1, so that in steady state the current limit is in operation for about two thirds of the transducer pulse duration, i.e. about 10% of the ignition cycle period.

When the dwell control loop is not in operation the voltage on capacitor C_2 is pre-conditioned by means of transistor Q_{13} and diode D_4. Diode D_5 prevents pre-conditioning from being applied during transducer pulses, thereby leaving the dwell control voltage undisturbed if the timer is pre-empted by the transducer pulse as a result of rapid acceleration at low engine speeds in dwell control.

Under engine running conditions, transistors Q_{30}, Q_{32} are held off and current passing via diode strapped transistor Q_{33} provides a reference voltage for the current control loop. This loop is gated by transistor Q_{39} which when off enables the current control loop transistors Q_{40}, Q_{41}, Q_{42}, Q_{43} and Q_{44}, which all operate in saturation until coil current has risen to a value at which the voltage across resistor R_{69} causes these stages to desaturate in succession as the current limit comes into control. When transistor Q_{43} is unsaturated, transistor Q_{45} is switched on, thereby signalling when the output stage is either in current limit or not conducting at all.

Capacitor C_5 and resistor R_{73} control the high frequency gain of the current limit amplifier.

The command signal for coil switching operates via transistors Q_{34}, Q_{36}, Q_{37} and Q_{39}, with transistor Q_{38} providing a brief hold-off pulse lasting about 0.3mS in order to prevent spurious coil turn-on due to spark

interference. This hold-off pulse is also used to turn on the mode control switch (Q_{18}, Q_{19}), and it also ensures that transistor Q_{31} is held on despite spark interference, thereby assuring undisturbed measurement of current limit duration by the associated circuit.

Transistor Q_{31} conducts only when the coil is off. Consequently, during each transducer pulse, transistor Q_{31} is off and transistors Q_{27} and Q_{28} are latched on, thereby holding off transistors Q_{26} and Q_{25}. The "lower" side of capacitor C_3 is therefore held near ground potential as it discharges, initially at about 1μA. If the mode control bistable switch is off, transistor Q_{29} turns off when current limit is reached, causing capacitor C_3 to be discharged additionally at about 100μA. If the period of this augmented discharge falls short of about 1mS, transistors Q_{27} and Q_{28} remain on when transistor Q_{31} turns on, and capacitor C_3 is recharged rapidly. If the 1mS threshold is exceeded, the base potential of the transistor Q_{27} is raised above that of transistor Q_{26} when transistor Q_{31} turns on, resulting in transistors Q_{27} and Q_{28} turning off and transistors Q_{26} and Q_{25} turning on. In this event capacitor C_3 recharges relatively slowly, enabling a modest excess of current limit duration above the threshold value to produce an output from transistor Q_{25} outlasting the coil hold-off pulse.

At a voltage on capacitor C_3 lower than the threshold for switching off transistors Q_{27}, Q_{28} the augmented discharge current resulting when transistor Q_{29} is non-conducting is removed by means of diodes D_9, D_{10}, and capacitor C_3 continues to discharge at about 1μA. After about 300mS, transistors Q_{30} and Q_{32} turn on and follow the voltage of capacitor C_3, shutting down the current limit control reference and thereby smoothly

turning off the coil current without creating a spark. The coil current thus turns off under control and without a spark being created following an engine stall.

The transistors Q_{22}, Q_{23} and Q_{24} form a bistable circuit which delivers an output from transistor Q_{22} if the negative going transducer pulse applied to its base occurs before it is shorted out by the positive going coil turn-on signal applied via diode D_{12}. If transistor Q_{22} is turned on by the transducer pulse occurring first, then transistor Q_{23} is held on, thereby sustaining the output until the end of the transducer pulse. The output is used via transistor Q_{21} to turn off the mode control bistable switch (Q_{18}, Q_{19}) for the duration of any transducer pulse which pre-empts the timer. It also provides for this period, a discharge current via transistor Q_{20} for capacitor C_2, affording a "forcing" dwell control correction.

The leading edge of the transducer pulse turns on transistor Q_{22} directly, but it turns on transistor Q_{24} via the turn-off delays of overdriven transistors Q_1, Q_{36} and Q_{23}. Thus, the "race" condition is reliably "won" by transistor Q_{22} whenever the timer is pre-empted.

As mentioned above transistors Q_{18} and Q_{19} form a complementary bistable mode control switch which when on enables timed turn-on by means of transistor Q_5. When the mode control switch is off, transistor Q_5 conducts only during transducer pulses, giving direct coil control by the transducer signal.

The arrangements described ensure that the mode control switch is not turned to "off" (direct control) when spurious sparks could result. Three separate means are

provided for turning the mode control switch off and two of these, viz the "timer outranged" detector and the "timer-pre-empted" detector both have outputs which are effectively gated by the transducer pulse. The switch is turned on, if not already on, by the coil hold-off pulse, and is turned off immediately afterwards if a more persistent output is received from the current limit duration detector.

Mode change due to falling speed with negligible jitter is normally caused by "timer outranged" detection at, for example, about 700 rpm engine speed.

Jitter-induced hunting between modes is avoided since at speeds high enough for mode change to timer operation, the timed turn-on is early enough to avoid being pre-empted despite substantial jitter (up to 6% with typical value of coil-current growth time).

For optimum dynamic performance in following engine acceleration, the magnitudes of the sink and source currents passed by transistors Q_{11} and Q_{12} are chosen in relation to the capacitor C_2 and in relation to the time constants of the timer circuit to ensure that the dwell time error in any given cycle is approximately matched by the resultant timer delay correction in the next cycle at speeds at which transistors Q_3, Q_4 turn off. At high speeds the reduced coil off time can result in residual coil energy at coil turn on, causing random variations in the coil current growth time. Under these circumstances a reduced correction per cycle provides desirable smoothing of the response when transistors Q_4 and Q_3 remain on.

If necessary, a voltage limiting protective zener diode feedback circuit of known kind may be associated with transistor Q_{44}.

CLAIMS

1. A dwell control for an ignition system employing a transducer (10) driven by the engine and producing a pulse train of approximately constant duty ratio and including mechanical means for varying the phase of the pulse train relative to the engine cycle in accordance with engine operating conditions, energy storage means (14) controlled by said transducer for releasing energy to create ignition sparks in synchronism with specific events in said pulse train, means (Q22) sensitive to different specific events in said pulse train for commencing an energy storage period in each ignition cycle at relatively low engine speeds, timer means (C_1, Q_2, Q_3 and Q_4) operating at relatively high engine speeds and operating under the control of said transducer to commence said energy storage period at an instant in each cycle earlier than said different specific event, the timing period of said timer being determined by closed loop control means so as to regulate the fractional time during which the energy stored by said energy storage means exceeds a threshold value, characterised by mode selection bistable switch means (Q18, Q19) for determining whether or not said timer or said different specific event is to cause commencement of said energy storage period, said bistable switch means being switched to a state in which said timer causes commencement of said energy storage period whenever the time duration for which the energy stored by said energy storage means exceeds a threshold value is less than a predetermined duration and to its other state in which said different specific events cause commencement of the energy storage period either when the timing period of the timer exceeds a limiting value or when said different specific event occurs before expiry of the timing period of said timer.

2. A dwell control as claimed in claim 1 in which the energy storage means is an ignition coil (14), current in the coil being sensed by the closed loop control means.

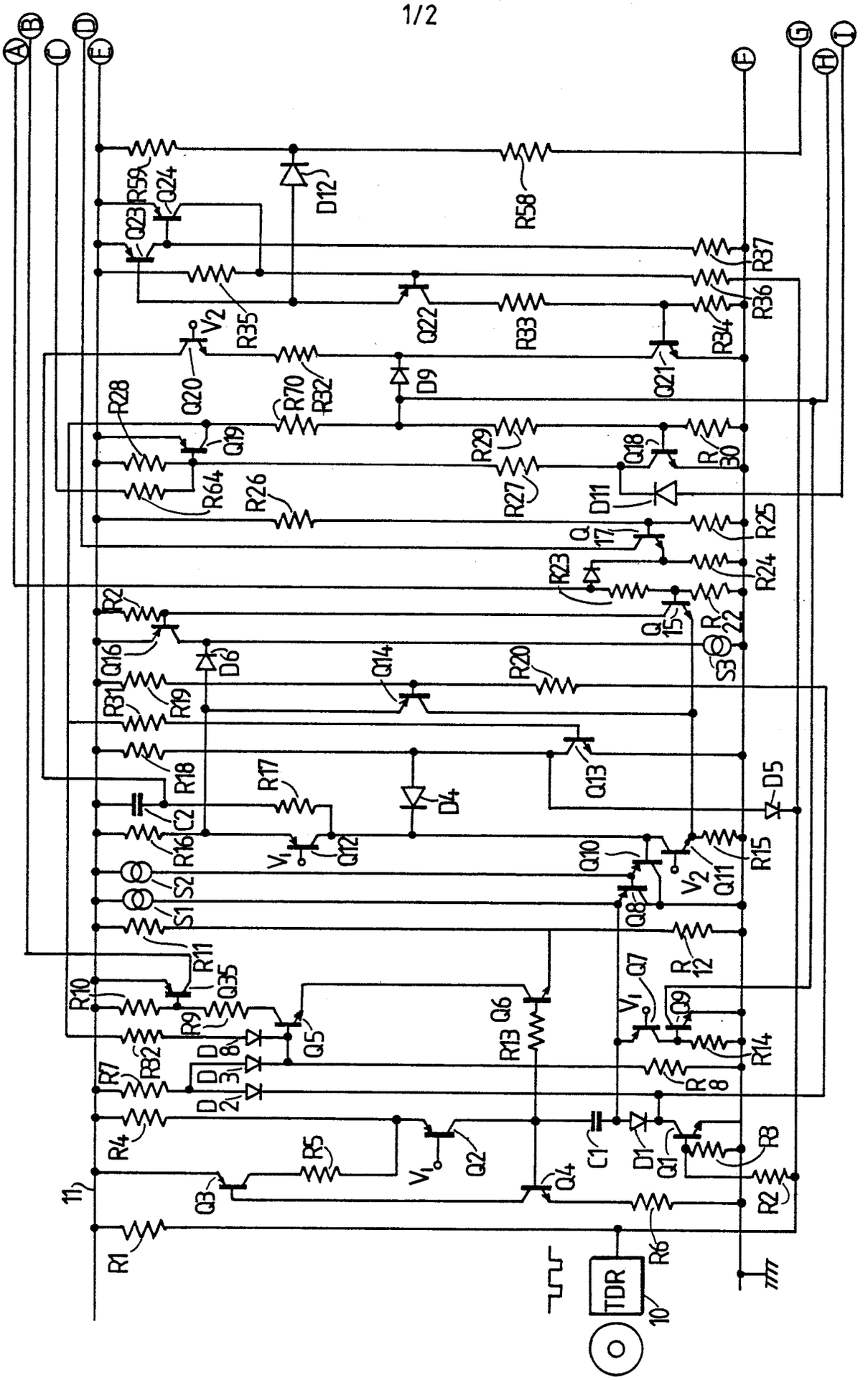
3. A dwell control as claimed in claim 2 comprising a semiconductor switch device (Q_{44}) and a current sensing element (R69) in series with the coil (14), a drive amplifier (Q_{37}, Q_{39}, Q_{41}, Q_{42}, Q_{43}) for providing drive current to said switch device (Q_{44}), current limit semiconductor means (Q_{40}) connected to said current sensing element (R_{69}) and to the drive amplifier and operating to reduce the current supplied to the switch device (Q_{44}) when the coil current exceeds a threshold level and means (Q_{45}) connected to the drive amplifier and providing a feedback signal to the closed loop control means when the current limit semiconductor means (Q_{40}) is in operation.

4. A dwell control as claimed in any preceding claim in which a capacitor (C_3) is employed in a timer circuit (Q_{27}, Q_{28}) for detection of when the time duration for which the energy stored by the energy storage means exceeds a threshold value is greater than said predetermined duration.

5. A dwell control as claimed in claim 4 in which said capacitor (C_3) preserves a charge signalling such detections until after spark interference has subsided, which charge then determines whether the mode selection bistable switch means (Q_{18}, Q_{19}) is switched from said first-mentioned state to said other state.

6. A dwell control as claimed in claim 4 or 5 in which said capacitor (C_3) also operates so as smoothly to turn off the coil current when necessary after the transducer signal has ceased.

7. A dwell control as claimed in claim 6 in which said capacitor (C_3) is connected to said closed loop control means so as to provide a signal thereto representing said threshold value which reduces gradually as said capacitor (C_3) discharges following cessation of the transducer signal.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Q10
V2
Q11
R15
S2
S1
Q8
R11
R12
R10
Q35
Q7
V1
Q9
R9
Q5
Q6
R13
R14
D
8
D
3
D
2
R7
R32
R8
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11
R1
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TDR
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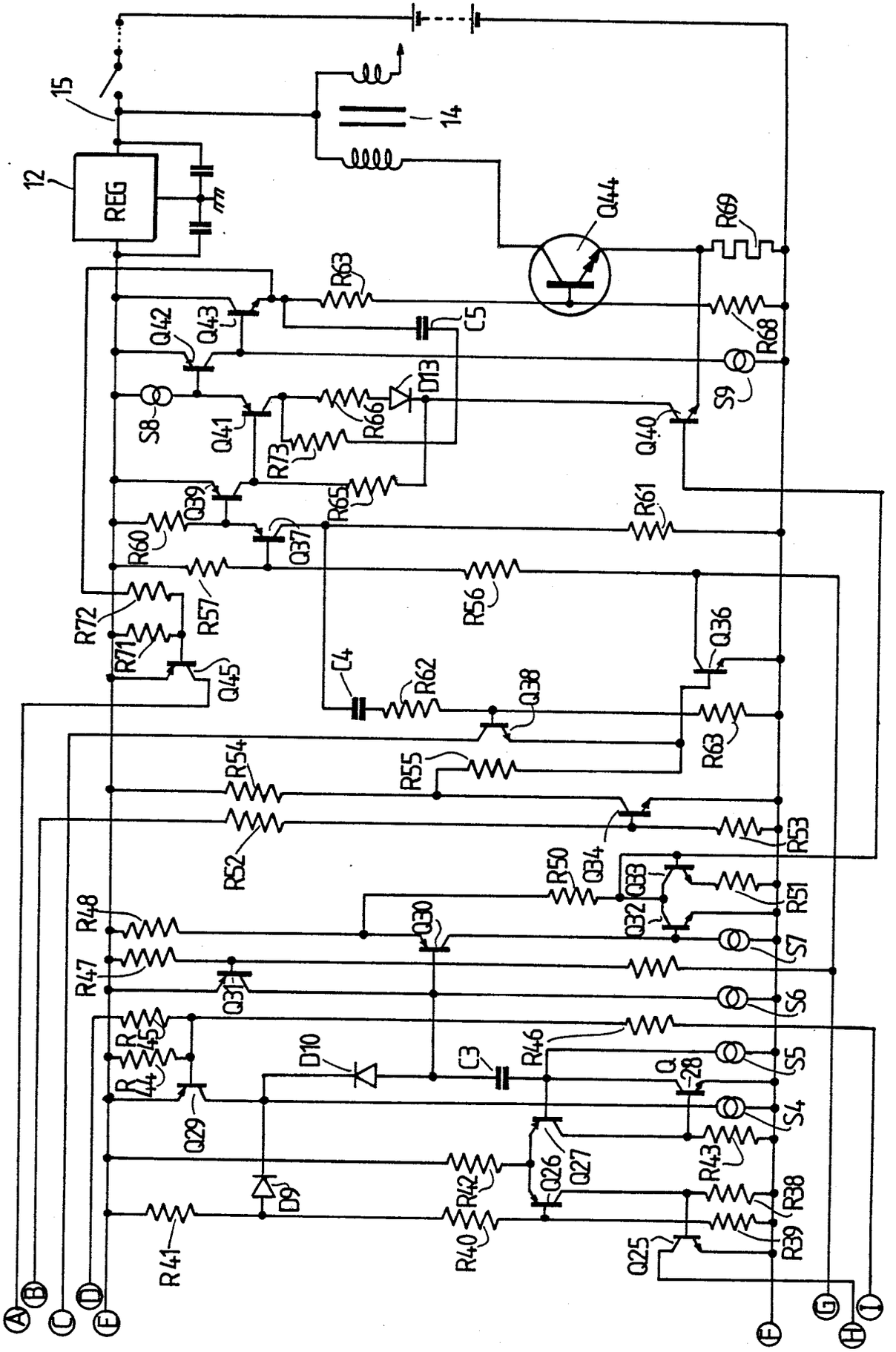
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R73
Q39
R65
R61
R60
Q37
R57
R56
R72
R71
Q45
C4
R62
Q38
Q36
R63
R54
R55
R52
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Q33
Q32
R51
R48
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Q31
S6
R45
R44
D10
C3
R46
Q28
S5
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S4
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D9
R42
R38
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R40
Q25
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A
B
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