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Description

The present invention relates to a distributed processing system, and more particularly to a distributed processing system which includes mutually related subsystems in which a fault in one subsystem may adversely affect to other subsystems and in which a system-down is prevented and a degree of the failure is diagnosed to improve a reliability.

In Fig. 1, the detection and diagnostic of the fault and recovery processing based on a result of the diagnostic in a prior distributed processing system are compared with recovery processing in the present invention to be described later in detail. The ordinate in Fig. 1 represents an object item to be detected and diagnosed, and the abscissa represents object to be recovered based on the result of the detection and diagnosis.

In Fig. 1, an apparatus which detects a fault in its own subsystem and recovers the fault in its own subsystem or faults in other subsystem based on the result of the detection of the fault is called a self-diagnostic tester. In the self-diagnostic tester, each subsystem is configured on the presumption that "other subsystems perfectly detect and diagnose all faults and recover the faults based on the result of the diagnostic". Accordingly, if the subsystem fails to detect, diagnose or recover the fault or makes a mistake, the other subsystems are influenced and a system-down is caused. An apparatus which detects and diagnoses a fault in other subsystems and recovers the fault in the other subsystems based on the result of the diagnosis is called a centralized tester. The failure or the mistake in the detection, diagnosis or recovery in the centralized tester also directly affects other subsystems and causes the system-down.

In the present invention, on the other hand, an autonomous tester which detects and diagnoses faults in other subsystems and protects a subsystem of its own from the faults of the other subsystems based on the result of the diagnosis is used. The functions of those three types of testers are illustrated in Figs. 2 and 3.

The self-diagnostic tester includes two types shown in Figs. 2A and 2B. A tester in a subsystem 1 instructs recovery processing 21 to the subsystem 1 of its own or recovery processing 22 or 22' to other subsystems 2 or 3 based on a result of detection and diagnosis 11 or 12 of a fault in its own subsystem. If the processing is not correctly done (symbol x in Figs. 3A and 3B, the other subsystems 2 and 3 are affected (31, 32 or 32') and faults are caused therein.

In the centralized tester (Fig. 2D), the tester in the subsystem 1 detects and diagnoses (14, 14') faults in the other subsystems 2 and 3 and instructs recovery processings 24 and 24' to the subsystems 2 and 3 based on the result of the diagnosis. Accordingly, the fault in the subsystem 1 directly affects (34, 34') to the other subsystems 2 and 3.

On the other hand, in the autonomous tester (Fig. 2C), the tester in the subsystem 1 detects and diagnoses (13, 13') the faults in the other subsystems 2 and 3 and conducts recovery processing 23 to protect its own subsystem from being affected by the faults in the other subsystem based on the result of the diagnosis. Accordingly, the failure or the mistake in the detection, diagnosis or recovery processing for the fault in the subsystem 1 does not affect to the other subsystems 2 and 3.

In the prior art distributed processing system, particularly in a system having a plurality of processors coupled through transmission lines, when a transient fault occurs, there is no means to determine whether it is a temporary fault or it highly probably becomes a permanent fault.

A distributed processing system with the features included in the first part of claim 1 is known from IEEE 1982, Twenty-Fourth IEEE Computer Society International Conference, Digest of Papers, Spring Compcon 82, San Francisco, February 22 to 25, 1982, pages 192-195. The paper describes a double-loop network system in which the data transmission is switched from one loop to the other through bypass links when a fault is detected. The detection of the fault and the reconfiguration of the transmission path may be initiated by any of the control processors connected to the system.

It is an object of the present invention to provide a distributed processing system which is capable of diagnosing the nature of any faults detected and predicting permanent faults.

This object is met by the invention as characterized in claim 1. According to the invention, because a permanent fault can be recognized before it has actually established, countermeasures can be taken more rapidly and "system-down" periods can be prevented.

The present invention will be apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

Fig. 1 illustrates classes of functions of various testers;

Figs. 2A - 2D and 3A - 3D diagramatically illustrate functions of the various testers;

Figs. 4 and 5 show a configuration of one embodiment of the present invention;

Figs. 6A - 6G, and 7A and 7B show operations in the embodiment;

Fig. 8 shows an address train;

Figs. 9 and 10 show an overall system of a second embodiment;

Figs. 11 and 12 show structures of NCP and a

host, respectively;

Figs. 13A - 13D show operations;

Fig. 14 illustrates a degree of fault;

Fig. 15 illustrates a principle of the present invention; and

Fig. 16 is a processing flow chart of BIT which is a main portion of the embodiment of the present invention.

In the following embodiments, the present invention is applied to a loop transmission system.

[First Embodiment]

Fig. 4 shows an overall configuration of a distributed processing system in accordance with a first embodiment of the present invention. The present system comprises paired network control processors arranged on dual loop transmission lines of opposite transmission directions. The paired network control processors 100 and 110, 200 and 210 ... are interconnected by bypass routes 100A, 110A; 200A, 210A; ... . Broken lines show areas of subsystems. For example, a subsystem 1 comprises the network control processor 100, a loop transmission line 1200 and the bypass route 100A, and a subsystem 2 comprises the network control processor 200, a loop transmission line 2300 and the bypass route 200A. The subsystem 1 is connected to only the subsystems 2, 4 and 5.

Fig. 5 shows a detail of the subsystem 1. A processor (host) 1000 is connected to the paired network control processors 100 and 110 through paired host transmission lines 111 and 211. The network control processors 100 and 110 and the processor 1000 contain testers (BIT) 100B, 110B and 1000B, respectively. The BIT performs the detection, diagnosis and recovery of the faults of other subsystems among the functions of the network control processor. The processor 1000 also contains a tester (EXT) 1010 to identify a fault location in the system. As will be described later, the EXT 1010 supplies a fault location information to a display 1020 to inform a service man. While not shown, the other subsystems 2, 3, ... are constructed identically to the subsystem 1.

The operations of the testers BIT 100B, 110B and 1000B and the EXT 1010 are now explained in detail with reference to Figs. 6A - 6G, 7 and 8. In the following description, it is assumed that the network control processors (NCP's) 400 and 410 are down.

It is assumed that the NCP 200 sends out a message 201 on the transmission line (loop) 2300. If the message is not returned to the sending source NCP 200 within a predetermined time period T_1, the NCP 200 retransmits the same message for confirmation. If the number of times of the retransmission reaches a predetermined number N_1, the BIT 200B determines that a fault has occured on the transmission line (see Fig. 6A). Then, the BIT 200B sends out a minor loop check signal 202 to check if the message can be transmitted to the NCP 300 of the adjacent subsystem. When the BIT 300B of the NCP 300 receives the minor loop check signal 202 from the transmission line 2300, it determines that a fault has occured somewhere on the transmission line and sends the minor loop check signal 202 to the paired NCP 310 and also sends out a minor loop check signal 302 to the transmission line 3400.

When the NCP 310 receives the minor loop check signal 202 from the bypass route 300A, it sends out the minor loop check signal 202 to the loop 3200. When the BIT 210B of the NCP 210 receives the minor loop check signal 202 from the loop 3200, it transmits the minor loop check signal 202 to the paired NCP 200. In this manner, when the minor loop check signal 202 is returned to the sending source NCP 200, the BIT 200B determines that it can transmit the message to the adjacent NCP 300 and sends out the message to the loop 2300.

On the other hand, the BIT 200B informs the BIT 210B of the NCP 210 that the fault may have occurred on the inner loop. Thus, the BIT 210B sends out a minor loop check signal 212 to the loop 2100 as the BIT 200B did. When the BIT of the NCP receives the minor loop check signal, it checks the minor loop in the same manner as described above. Since it was assumed in the present example that the NCP 400 and 410 are down, the minor loop check signal is not returned to the BIT 300B and 110B.

As a result, the BIT 300B constitutes the bypass route 300A and the BIT 110B constitutes the bypass route 110A and they send out the received messages not to the loops 3400 and 1400, respectively, but only to the bypass routes 300A and 110A, respectively (see Fig. 6B).

The BIT's 300B and 110B which constituted the bypass routes send out bypass route constitution broadcast signals 303 and 113, respectively. When the NCP 100 or 110 connected to an EXT 1010 receives the bypass route constitution broadcast signal 303 or 113, it transmits the signal 303 or 113 to the processor 1000 (see Fig. 6C).

The EXT 1010 of the processor 1000 diagnoses that a fault location is at 113' (hatched area in Fig. 6D) based on the bypass route constitution broadcast signal 113 and a fault location is at 303 (right hatched area in Fig. 6D) based on the bypass route constitution broadcast signal 303. The EXT 1010 combines the results of diagnoses and determines that the fault location is somewhere in the areas 113' and 303' and displays it on the display

1020.

The BIT's 300B and 110B which constituted the bypass routes alternately and cyclically send out the minor loop check signals 302 and 112 (Fig. 6B) and major loop check signals 304 and 114 (Fig. 6E) to check if the fault has been recovered. Since the major loop check signal is not bypassed by any NCP, if the major loop check signal 304 circulates through the loop and returns to the sending source, the BIT 300B determines that the fault on the loop has been recovered and releases its own bypass route 300A. When the minor loop check signal sent out by the BIT 300B or 110B returns to the sending source BIT, it releases its own bypass route (see Fig. 6E).

After the BIT 300B has released the bypass route, it sends out a bypass route release broadcast signal 305. When the NCP 100 connected to the EXT 1010 receives the bypass route release broadcast signal 305, it transmits the signal 305 to the EXT 1010 (see Fig. 6F).

The EXT 1010 cancels the bypass route broadcast signal 303 from the BIT 300B based on the bypass route release broadcast signal 305 for the diagnosis results 113' and 303', and it also cancels the fault diagnosis result on the loop 4100 to narrow the fault location range to an area 113'' (see Fig. 6G).

In order for the transmission to be correctly carried out, it is essential that the addresses of the respective NCP's are set without overlap. To this end, each BIT checks if the other NCP's have the same address as that of its own when the power is turned on. Assuming that when the NCP 100 is started, the NCP's 200, 300, 310, 210 and 110 have already been started (see Fig. 7A), the BIT 100B of the started NCP 100 sends out an address train 106 to be described later. The address train 106 is sequentially received by the respective NCP's and sent out after the registration of the address. After the address train 106 has been circulated twice on the transmission line, it is transferred to the EXT 1010 by the sending source BIT 100. A process of formation of the address train as it passes the respective NCP's is shown in Fig. 8. Each BIT registers the address 106A and sets a bypass flag 1068 to "1" if the bypass route is being constituted.

The BIT 100B receives the address train 106B after it circulated twice on the transmission line, and if the addresses of the other subsystem between its own addresses 100 in the first run and the second run are not equal, it determines that there is an overlapped address and stops further transmission. The NCP 100 connected to the EXT 1010 reads in the address train 106 and informs it to the EXT 1010. The EXT 1010 checks the bypass flag and the address in the address train 106 and determines the configuration of the system as 106' (see Fig. 7B) and displays it on the display 1020.

When the transmission to the NCP 100 (or 110) is not permitted, the BIT in the processor switches the transmission direction to the paired NCP 110 (or 100).

While the present invention is applied to the loop transmission system in the above embodiment, the present invention is not limited thereto but it may be applied to other distributed processing system such as line or mesh distributed processing system.

For the detail of the operation of the above embodiment, reference may be made to U.S. Patent 4,380,061 "Loop Transmission System" and Japanese Patent Laid-Open Publication 200951/82.

[Second embodiment]

In the first embodiment described above, there is a problem that it is not possible to determine whether the transient fault detected is becoming a permanent fault or not, and a degree of the fault. This will now be explained in detail.

Fig. 9 shows an overall configuration of the loop transmission system. Numerals 71 and 72 denote loop transmission lines for transmitting information in opposite directions to each other, and network control processors (NCP's) 711 - 716 and 721 - 726 are arranged on the loop transmission lines 71 and 72. The paired NCP's are interconnected by bypass routes 741 - 746 and 751 - 756. Processors (HOST's) 731 - 736 are connected to the paired NCP's through bilateral transmission lines 761 - 766 and 771 - 776.

Fig. 10 shows an arrangement of testers. The NCP's 711 - 716 and 721 - 726 and the HOST's 731 - 736 contain built-in testers (BIT's) 7101 - 7106, 7201 - 7206 and 7501 - 7506. As will be explained later, since each BIT detects, diagnoses and recovers the faults in other subsystems, the transmission is not interrupted but continued even if a fault occurs in the subsystem.

Fig. 11 shows an internal configuration of the NCP. While the NCP 716 is specifically shown, the other NCP's have the same configuration.

The NCP 716 comprises a processor 7160, an interface 7162 to the loop transmission line 71, an interface 7163 to the HOST 736 and the paired NCP 726, a receiving buffer 7164 for storing a message received from the loop transmission line 71 and the paired NCP 726, a transmission buffer 7165 for storing a message received from the HOST 736, an input content code table 7166 for storing a content code of a message to be read in by the NCP 716, a timer T_1 7167 for monitoring a fault in the transmission, a bypass status register 7168 for detecting a bypass status of its own unit,

a timer T_2 7169 for periodically checking a time variation of a transient fault and a fault history buffer 7170 for storing a history of the fault status. An operation program of the BIT is stored in a memory 7161.

Fig. 12 shows an internal configuration of the HOST. While the HOST 732 is specifically shown, the other HOST's have the same structure except the external testers and the displays to be described later.

The HOST 732 comprises a processor 7320, an interface 7321 to the NCP's 712 and 722, a receiving buffer 7322 a transmission buffer 7323, and timers T_1 and T_2, 7330 and 7331 having the same functions as those described above, flags 7324 and 7325 for indicating permission or non-permission of transmission to the NCP's 712 and 722, a memory 7326 for storing a BIT operation program and a buffer 7327 for storing a result of BIT operation.

An external tester EXT 7602 for discriminating a fault location of the system to maintain the system is provided in the HOST 732. The EXT 7602 outputs the fault location to the display 7702 to inform it to a service man. The operation program of the EXT 7602 is stored in the memory 7328 and the buffer 7329 stores the result of the operation.

A fault prediction diagnosis operation when a transient fault caused by a noise on the transmission line gradually grows is explained with reference to Figs. 13A to 13D.

Fig. 13A shows an operation when a transient fault has occurred on the loop transmission line 71 between the NCP's 714 and 715. When the NCP 716 transmits a message on the loop transmission line 71, the transmitted message is not returned even after a predetermined time period T_1 and hence the NCP 716 retransmits the same message. If the message does not circulate because of the transient fault after the repetition of a predetermined number N_1 of times of the retransmission, the BIT 7106 of the NCP 716 determines that the fault exists on the loop transmission line 71.

The BIT 7106 then sends out a minor loop check signal 7302 to check if it can transmit the message to the adjacent NCP 715 as shown in Fig. 138. When the BIT 7105 of the NCP 715 receives the minor loop check signal 7302 from the loop transmission line 71, it transmits the received minor loop check signal 7302 to the paired NCP 725 and also sends out a minor loop check signal 7301. When the BIT 7205 of the NCP 725 receives the minor loop check signal 7302 from the bypass route 755, it sends out the minor loop check signal 7302 to the loop transmission line 72.

When the BIT 7206 receives the minor loop check signal 7302 from the loop transmission line 72, it transmits the minor loop check signal 7302 to the paired NCP 716. If the minor loop check signal 7302 circulates and returns to the sending source NCP 716, the BIT 7106 can transmit the message to the adjacent NCP 715 and determines that there exists no fault and subsequently sends out the message to the loop transmission line 71.

It is assumed that the minor loop check signal 7301 sent out from the BIT 7105 does not return because of the transient fault in the loop transmission line. In this case, the BIT 7105 constitutes a bypass route 755 and does not subsequently send out the received message to the loop transmission line 71 but sends it out only to the bypass route 755. On the other hand, the BIT 7106 informs to the BIT 7206 that there may exist a fault on the loop transmission line 72 and the BIT 7206 sends out a minor loop check signal 7303 as the BIT 7106 did.

The BIT's 7201, 7202, 7203 and 7204 sequentially check the minor loops in the same manner. Assuming that the minor loop check signal 7307 does not return to the BIT 7204 because of the transient fault, the BIT 7204 constitutes the bypass route 744 as shown in Fig. 13B and subsequently sends out the received message not to the loop transmission line 72 but only to the bypass route 744.

The BIT's 7105 and 7204 which constituted the bypass routes send out bypass route constitution broadcast signals 7308 and 7309. When the EXT 7602 receives the bypass route constitution broadcast signals from the NCP's 712 and 722, it displays the fault location on the display 7702 (see Fig. 13C).

The BIT's 7105 and 7204 which constituted the bypass routes alternately and cyclically send out a major loop check signal which is not bypassed by any NCP and the minor loop check signal in order to check if the fault has been recovered. If one of those signals returns, the BIT 7105 or 7204 regards that the previously detected fault has been recovered and releases the bypass route and subsequently sends out the received message to the loop transmission line.

Since the fault between the NCP's 715 and 714 is the transient fault, the minor loop check signal sent out by the BIT 7105 may return. In this case, in the diagnosis system in the prior art loop transmission system, the EXT 7602 determines that the system is normal (see Fig. 13D). Thus, although the transient fault still exists, the maintenance to the transient fault may not be carried out.

In the second embodiment of the present invention, in order to resolve the above problem, a degree of the transient fault is stored, and when necessary, it is determined if the transient fault will shift to a permanent fault or not based on a time variation of the degree of the fault, and if it is

determined that the fault will shift to the permanent fault, it is informed to a man-machine system to enhance a maintenability. In this manner, a loop transmission system capable of predicting and diagnosing the fault is provided.

To this end, in the second embodiment, a dual loop transmission system having two loop transmission lines for transmitting data in opposite directions to each other, NCP's paired with the transmission lines and bypass routes for bilaterally transmitting the data between the paired NCP's, is provided with means for storing a degree of the fault detected on the transmission line.

The second embodiment will be explained in detail with reference to the drawings. In the present embodiment, the above object is achieved by adding a new function to the BIT described above. The new function uses a program operation of a microprocessor.

Fig. 14 shows a time variation of the degree of the fault on the transmission line. The ordinate represents a ratio TR (transient rate), which is obtained by dividing the number of times (RC) of feedback of the minor loop check signal in a predetermined time period by the number of times (SC) of send-out, as the degree of the fault, and the abscissa represents time. That is,

$$TR = RC/SC$$

Symbols o indicate a pattern in a normal state, symbols • indicate a pattern in the permanent fault and symbols △ indicate a pattern in the transient fault. It is considered that the degree of the transient fault tends to gradually increase with time.

Fig. 15 illustrates a principle of the present invention. Ordinate and abscissa represent the same contents as those in Fig. 14 respectively. The time axis scale in the abscissa is shown by a check interval, and the RC and SC described above are cleared to zero at every check interval. The time (fault prediction time) t_T at which the fault is estimated to become the permanent fault is calculated only when the TR value which indicates the degree of the fault is below a value Nmin (for example, Nmin = 0.5) which indicates that the fault clearly exists on the transmission line.

If the degree of the fault TR (NOW) is below N_{min} at time T_4 shown in Fig. 15, differences between the degrees of fault in adjacent generations $\Delta X(1)$, $\Delta X(2)$ and $\Delta X(3)$ are calculated based on the degrees of fault in the three past generations TR(3), TR(2) and TR(1) and the degree of fault in the current generation TR(NOW), and an average thereof ΔX is calculated.

The prediction time t_T can be represented as a relative time to the current time as follows.

$$t_T = TR(NOW) \times t_{fix}/\Delta X$$

where t_{fix} is the check interval.

The operation of the BIT in the NCP will be now explained by a processing flow chart shown in Fig. 16. Since all BIT's in the subsystems have the same algorithm, only the BIT 7106 of the NCP 716 is explained.

The BIT 7106 is operated cyclically and checks if the timer T_2 times up (8000). The check interval t_{fix} has been set in the timer T_2 at the time of the previous check, and the content is decremented as the time elapses. When the timer T_2 times up, the next check is started. If the timer does not time up, the check is not carried out.

When the timer T_2 times up, a check interval t is newly set in the timer T_2 (8100). It is checked if the SC is zero or not (8200). If the SC is zero, no operation is carried out, and if the SC is not zero, the current degree of fault TR (NOW) is calculated by the following equation.

$$TR(NOW) = RC/SC$$

The RS and SC are then initialized (8400) and it is checked if the current degree of fault TR-(NOW) is below the reference N_{min} (8500). If the current degree of fault TR(NOW) is not below N_{min}, the history of the degree of fault is updated (9300), and if it is below N_{min}, three-generation history of the degree of fault is read out from the fault history buffer and the following calculations are performed (8600).

$$\Delta X(1) = TR(1) - TR(NOW)$$
$$\Delta X(2) = TR(2) - TR(1)$$
$$\Delta X(3) = TR(3) - TR(2)$$

An average ΔX of $\Delta X(1)$, $\Delta X(2)$ and $\Delta X(3)$ is calculated (8700). The sign of the average ΔX is examined, and if $\Delta X > 0$, it is determined that the degree of fault of the transient fault grows with time, and if $\Delta X \leqq 0$, it is determined that the degree of fault does not grow (8800). When $\Delta X > 0$, the prediction time t_T at which the current transient fault will become a permanent fault is calculated by the following equation.

$$t_T = TR(NOW) \times t_{fix}/\Delta X$$

A message to inform the result of calculation to the EXT 7602 is prepared, and the NCP address (SA) of its own, the time (relative time to the current time) t_T at which the transient fault will become the permanent fault and the current degree of fault TR(NOW) are set in a data field of the message (9000), and the data is sent out to the EXT.

When the degree of fault of the transient fault does not grow ($\triangle X \leqq 0$), a message to the EXT 7602 is prepared, and the NCP address (SA) of its own and the current degree of fault TR(NOW) are set in a data field of the message (9100), and the data is sent out to the EXT.

In any case, after the data has been sent out, the past history of the degree of fault is updated (9300).

When the EXT 7602 receives the data, it displays the data on the display 7702. A service man of the system observes it and can determine whether there is a transient fault, the degree of fault and the prediction time at which the transient fault will become a permanent fault so that he or she can predict and diagnose the transient fault.

While the operation of the BIT in one NCP of the second embodiment has been described above, the BIT's of the other subsystems operate in the same manner except the BIT in the HOST which checks the acceptance or non-acceptance of the transmission to the two NCP's instead of the minor loop to detect the transient fault.

In accordance with the second embodiment of the present invention, the dual loop transmission system having the two loop transmission lines for transmitting data in the opposite directions, the paired NCP's on the transmission lines and the bypass routes for transmitting the data bilaterally between the paired NCP's, is provided with the means for storing the degree of fault on the transmission lines. In one mode, the content of the memory means is read out as required to output the time variation of the degree of fault, in other mode, the possibility of the change of the transient fault to the permanent fault is predicted, and in the still other mode, the time at which the transient fault will change to the permanent fault is predicted.

As described hereinabove, in accordance with the present invention, there is provided the distributed processing system having a plurality of interconnected subsystems of equal level, in which each subsystem has the function to diagnose the faults in the other subsystems and protects its own subsystem based on the result of the diagnosis of the faults of the other subsystems. Accordingly, the system-down in the distributed processing system is prevented and the reliability of the system is improved. In the second embodiment, the means for storing the degree of fault on the transmission line is provided. Accordingly, when the transient fault occurs, the time variation of the degree of the transient fault and the change of the transient fault to the permanent fault can be informed to the man-machine system to improve the maintenability. Thus, the loop transmission system which can be readily prediction-diagnosed for the fault is provided.

Claims

1. A distributed processing system having a plurality of subsystems (1, 2, 3, 4, 5) interconnected through at least one transmission path (1200, 2300, 3400, 4100), each subsystem comprising:

means for applying a diagnosis signal to said transmission path to diagnose a fault in other subsystems and/or transmission paths connected to its own subsystem,

means for judging the fault in the other subsystems and/or transmission paths on the basis of the response to said diagnosis signal,

first storing means (7168) for storing network status data produced by said judging means, and

means for controlling the transmission through said transmission paths on the basis of the stored network status data, so as to prevent the detected fault from extending,

characterized in that each subsystem further comprises:

means for generating a signal (TR) representing a degree of fault in the other subsystems and/or transmission paths, the degree of fault being based on the number of times (RC) said diagnosis signal returns with respect to the number of times (SC) it is sent out,

second storing means (7170) for storing said generated signal as a history of the fault,

means for outputting the contents of said second storing means, and

means for predicting a permanent fault on the basis of the contents of said second storing means.

2. The system of claim 1, wherein said diagnosis signal includes a major loop check message and a minor loop check message.

3. The system of claim 1 or 2, wherein each subsystem further includes means for sending out an address train message and means for registering an address of its own in said address train message.

4. The system of any of claims 1 to 3, wherein said second storing means (7170) further stores a time variation ($\triangle X$) of said generated signal (TR).

5. The system of any of claims 1 to 4, wherein said predicting means provides an indication that the detected fault will become permanent when said generated signal (TR) is below a

predetermined value.

Patentansprüche

1. Verteiltes Verarbeitungssystem mit mehreren über mindestens einen Übertragungsweg (1200, 2300, 3400, 4100) miteinander verbundenen Untersystemen (1, 2, 3, 4, 5), deren jedes umfaßt:

   eine Einrichtung zum Anlegen eines Diagnosesignals an den Übertragungsweg, um einen Fehler in anderen Untersystemen und/oder in an das eigene Untersystem angeschlossenen Übertragungswegen zu erkennen,

   eine Einrichtung zur Beurteilung des Fehlers in den anderen Untersystemen und/oder den Übertragungswegen aufgrund der Antwort auf das Diagnosesignal,

   eine erste Speichereinrichtung (7168) zur Speicherung von von der Beurteilungseinrichtung erzeugten Netzwerk-Zustandsdaten, und

   eine Einrichtung zur Steuerung der Übertragung über die Übertragungswege aufgrund der gespeicherten Netzwerk-Zustandsdaten derart, daß eine Ausbreitung des ermittelten Fehlers verhindert wird,

   dadurch gekennzeichnet, daß jedes Untersystem ferner umfaßt:

   eine Einrichtung zur Erzeugung eines Signals (TR), das ein Maß für den Fehler in den anderen Untersystemen und/oder den Übertragungswegen angibt, wobei das Fehlermaß auf der Anzahl (RC) von Rückkehrungen des Diagnosesignals, bezogen auf die Anzahl (SC) seiner Aussendungen, beruht,

   eine zweite Speichereinrichtung (7170) zur Speicherung des erzeugten Signals als Fehlerhistorie,

   eine Einrichtung zur Ausgabe des Inhalts der zweiten Speichereinrichtung, und

   eine Einrichtung zur Vorhersage eines dauerhaften Fehlers aufgrund des Inhaltes der zweiten Speichereinrichtung.

2. System nach Anspruch 1, wobei das Diagnosesignal eine Hauptschleifen-Prüfnachricht und eine Unterschleifen-Prüfnachricht umfaßt.

3. System nach Anspruch 1 oder 2, wobei jedes Untersystem ferner eine Einrichtung zum Aussenden einer Adreßzug-Nachricht und eine Einrichtung zum Registrieren einer eigenen Adresse in der Adreßzug-Nachricht umfaßt.

4. System nach einem der Ansprüche 1 bis 3, wobei die zweite Speichereinrichtung (7170) ferner eine zeitliche Änderung (ΔX) des erzeugten Signals (TR) speichert.

5. System nach einem der Ansprüche 1 bis 4, wobei die Vorhersageeinrichtung dann, wenn das erzeugte Signal (TR) unter einem vorgegebenen Wert liegt, eine Anzeige erzeugt, daß der ermittelte Fehler dauerhaft wird.

Revendications

1. Système de traitement réparti possédant une pluralité de sous-systèmes (1,2,3,4,5) interconnectés par l'intermédiaire d'au moins une voie de transmission (1200, 2300, 3400, 4100), chaque sous-système comprenant:

   des moyens pour appliquer un signal de diagnostic à ladite voie de transmission pour diagnostiquer un défaut dans d'autres sous-systèmes et/ou d'autres voies de transmission raccordées à son propre sous-système,

   des moyens pour évaluer le défaut dans les autres sous-systèmes et/ou voies de transmission sur la base de la réponse audit signal de diagnostic,

   des premiers moyens de mémoire (7168) pour mémoriser des données d'état du réseau produites par lesdits moyens d'évaluation, et

   des moyens pour commander la transmission dans lesdites voies de transmission sur la base des données mémorisées d'état du réseau, afin d'empêcher une extension du défaut détecté,

   caractérisé en ce que chaque sous-système comprend en outre:

   des moyens pour produire un signal (TR) représentatif d'un degré de défaut dans les autres sous-systèmes et/ou voies de transmission, le degré de défaut étant basé sur le nombre de fois (RC) où ledit signal de diagnostic revient, par rapport au nombre de fois (SC) où ce signal est délivré,

   des seconds moyens de mémoire (7170) pour mémoriser ledit signal produit en tant qu'historique du défaut,

   des moyens pour délivrer le contenu desdits seconds moyens de mémoire, et

   des moyens pour prédire un défaut permanent sur la base du contenu desdits seconds moyens de mémoire.

2. Système selon la revendication 1, dans lequel ledit signal de diagnostic comprend un message de contrôle de boucle principale et un message de contrôle de boucle secondaire.

3. Système selon la revendication 1 ou 2, dans lequel chaque sous-système comprend en outre des moyens pour délivrer un message formé d'un train d'adresses et des moyens pour enregistrer une adresse qui lui est propre dans

ledit message formé de trains d'adresses.

4. Système selon l'une quelconque des revendications 1 à 3, dans lequel lesdits seconds moyens de mémoire (7170) mémorisent en outre une variation dans le temps (△X) dudit signal produit (TR).

5. Système selon l'une quelconque des revendications 1 à 4, dans lequel lesdits moyens de prédiction délivrent une indication du fait que le défaut détecté devient permanent lorsque ledit signal produit (TR) est inférieur à une valeur prédéterminée.

FIG. 1

OBJECT TO BE RECOVERED / OBJECT TO BE DIAGNOSED	OWN SUBSYSTEM	OTHER SUBSYSTEM
OWN SUBSYSTEM	SELF-DIAGNOSTIC	
OTHER SUBSYSTEM	AUTONOMOUS	CENTRALIZED

FIG. 2A

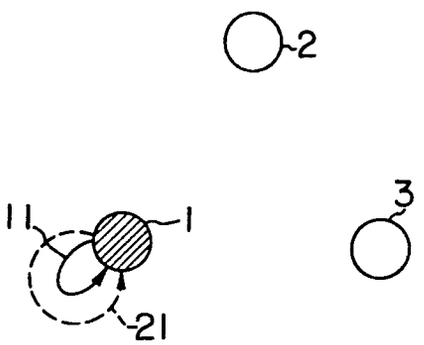


FIG. 2B

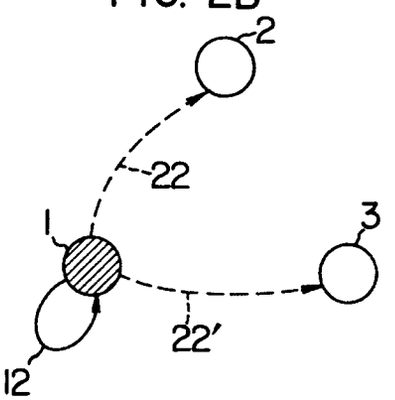


FIG. 2C

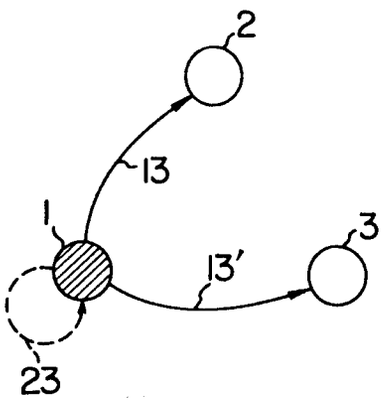


FIG. 2D

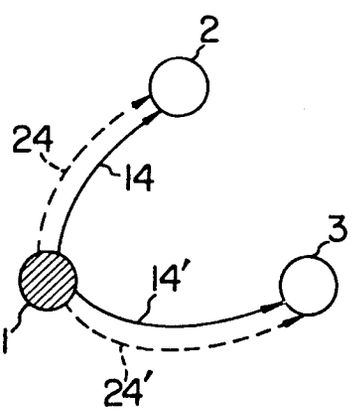


FIG. 3A

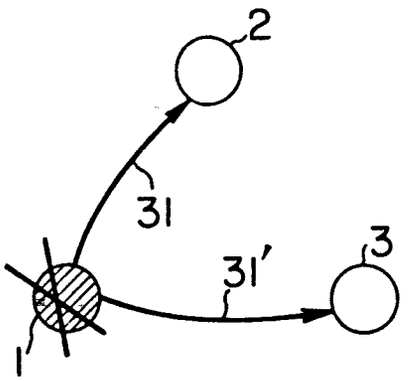


FIG. 3B

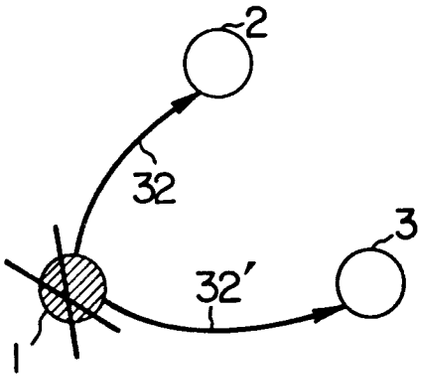


FIG. 3C

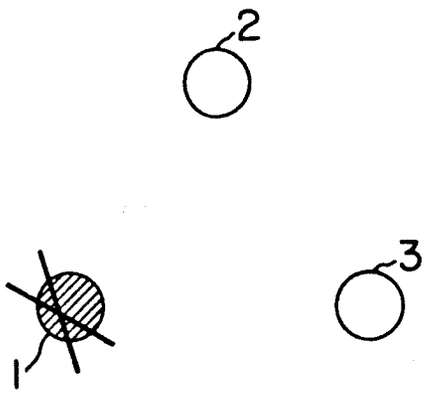


FIG. 3D

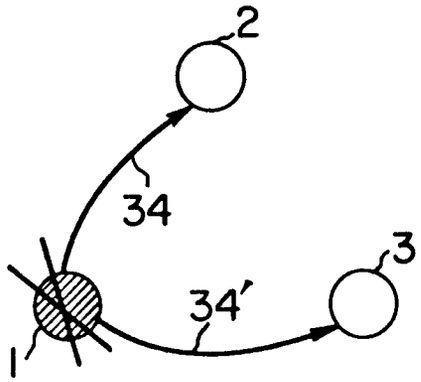


FIG. 4

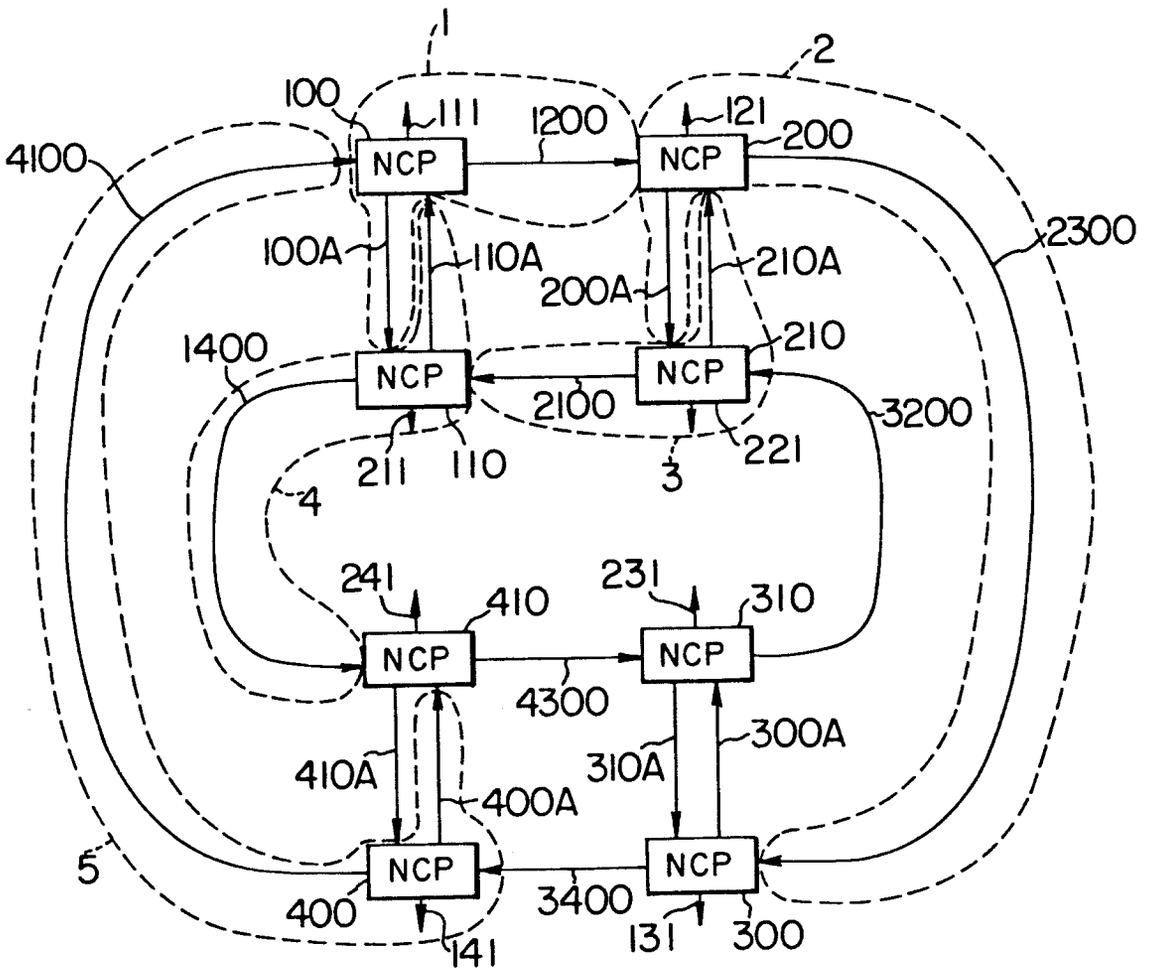

1
2
100
111
1200
121
200
4100
NCP
NCP
2300
100A
110A
200A
210A
1400
210
NCP
NCP
2100
3200
211
110
3
221
4
241
410
231
310
NCP
NCP
4300
300A
410A
310A
400A
5
NCP
NCP
400
3400
131
300
141

FIG. 5

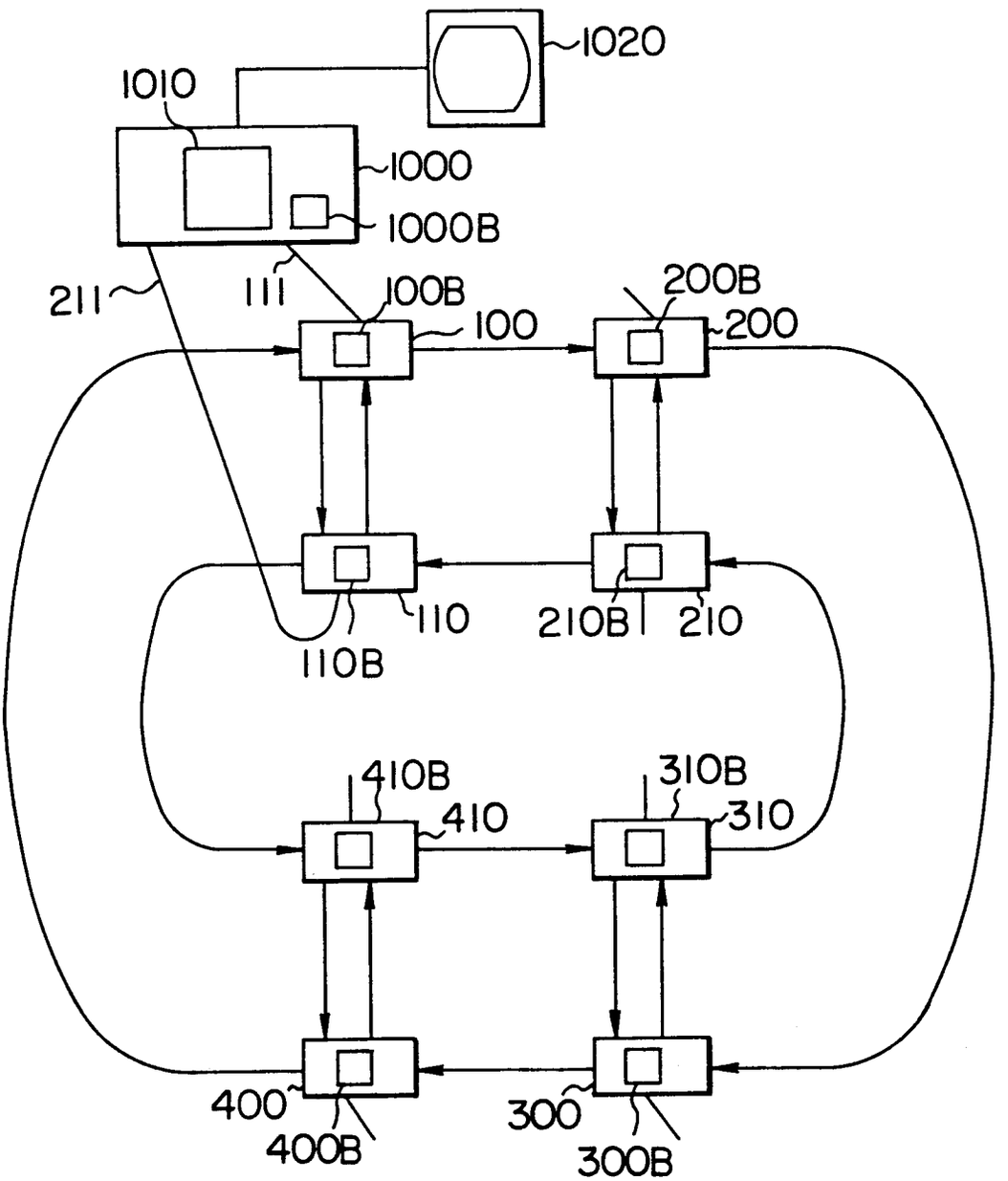

1020
1010
1000
1000B
211
111
100B
100
200B
200
110
110B
210B
210
410B
410
310B
310
400
400B
300
300B

FIG. 6A

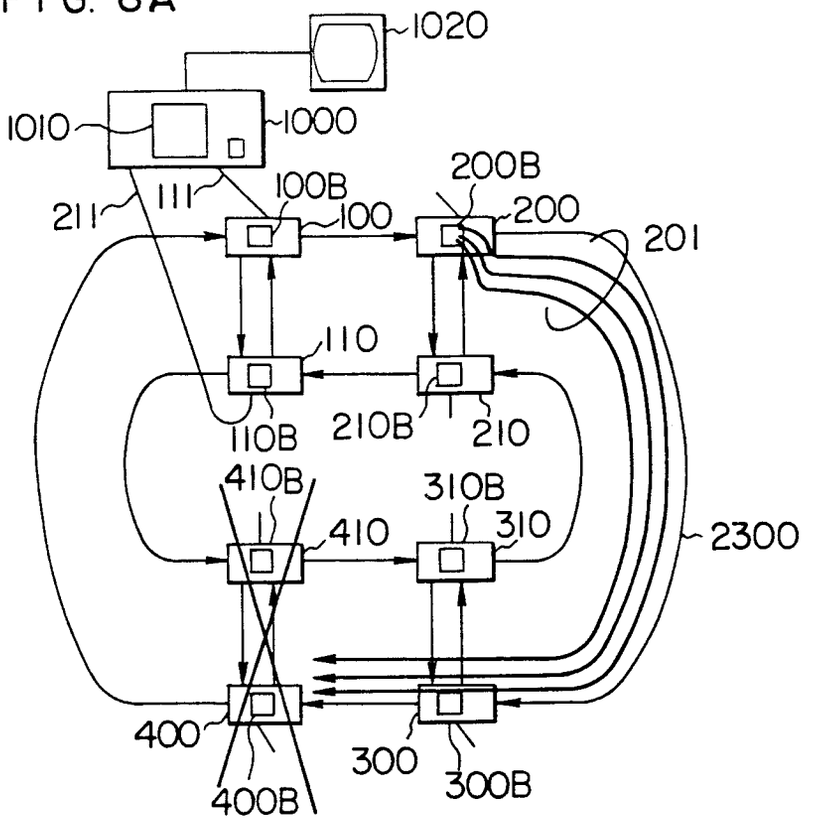

1020
1010
1000
200B
111
100B
211
100
200
201
110
110B
210B
210
410B
310B
410
310
2300
400
300
400B
300B

FIG. 6B

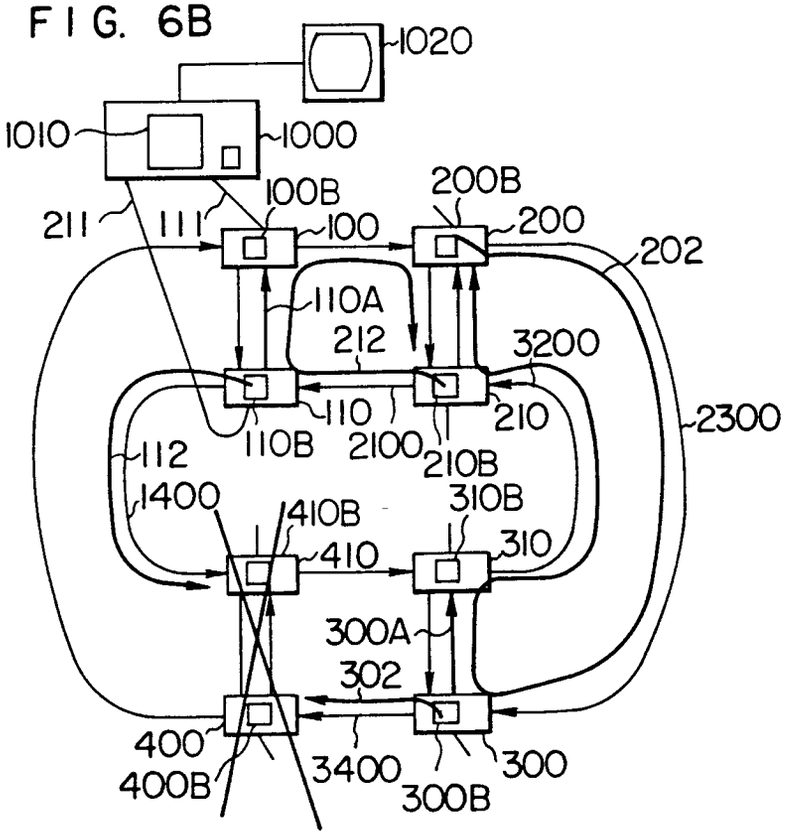

1020
1010
1000
200B
100B
211
111
100
200
202
110A
212
3200
110
210
2300
110B
2100
210B
112
1400
410B
310B
410
310
300A
302
400
400B
3400
300
300B

FIG. 6C

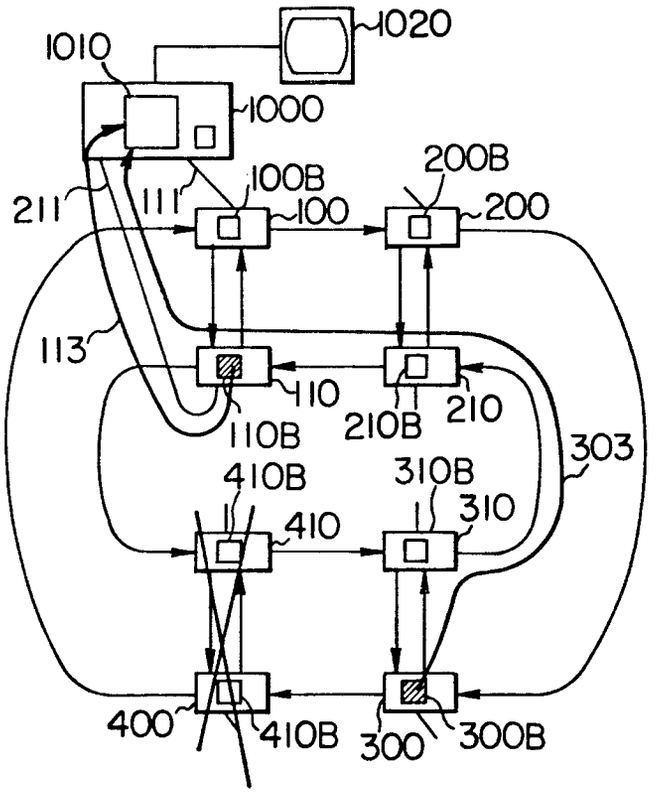

1020
1010
1000
200B
100B
211
111
100
200
113'
110
210B
210
110B
303
410B
310B
310
410
400
410B
300
300B

FIG. 6D

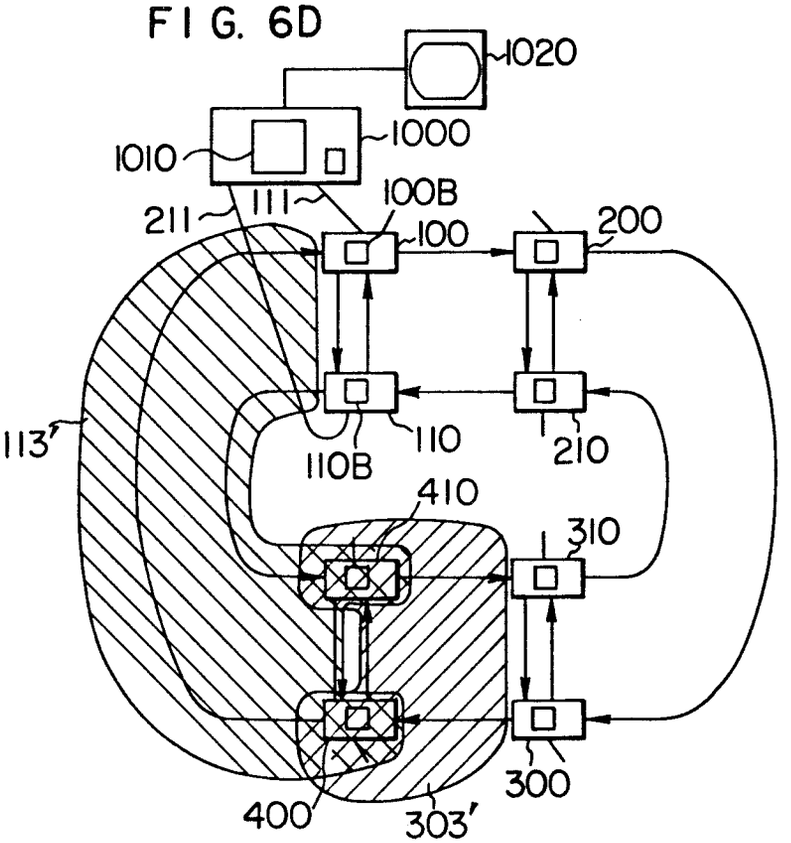

1020
1000
1010
111
100B
211
100
200
113'
110B
110
210
410
310
300
400
303'

FIG. 6E

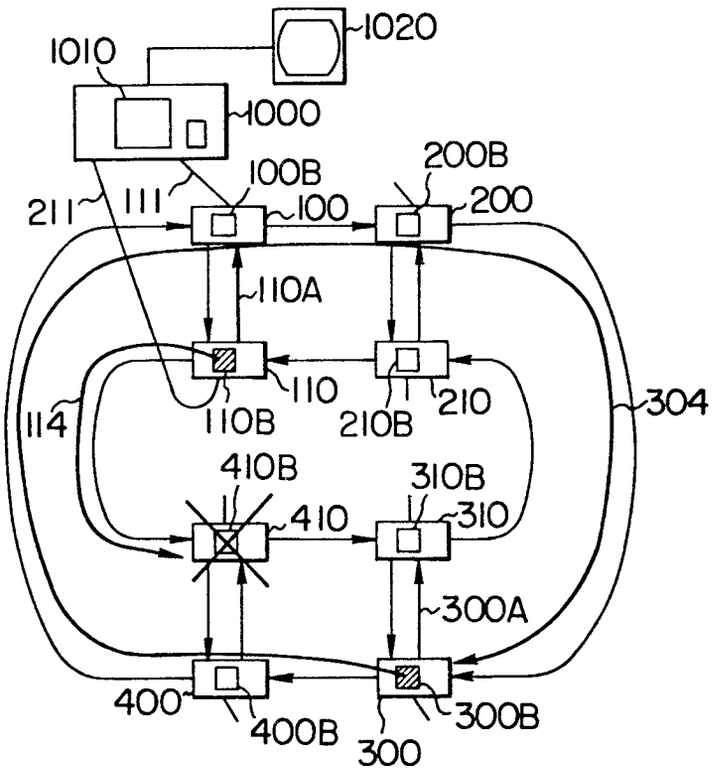

1020
1010
1000
200B
100B
211
111
100
200
110A
110
210
114
110B
210B
304
410B
310B
410
310
300A
400
400B
300B
300

FIG. 6F

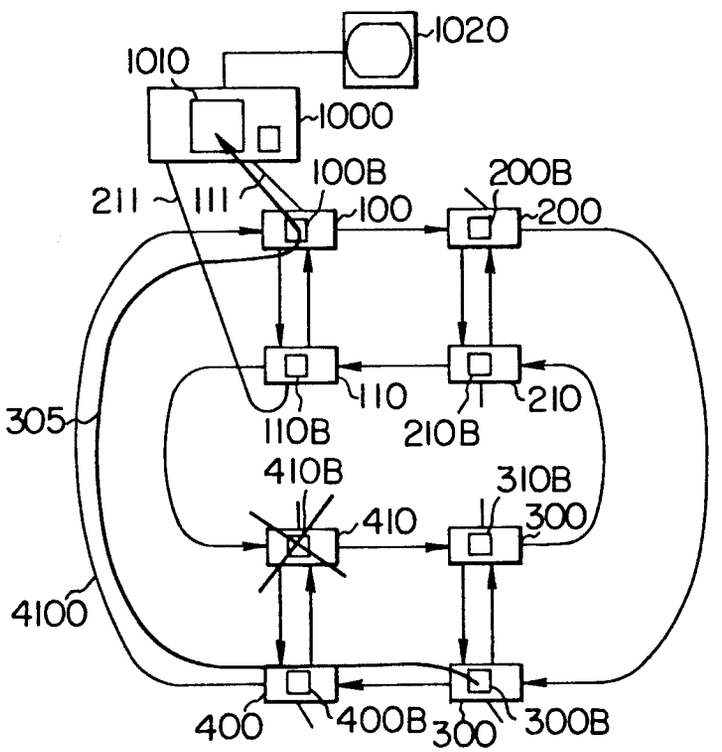

1020
1010
1000
100B
200B
211
111
100
200
110
210
305
110B
210B
410B
310B
410
300
4100
400
400B
300
300B

FIG. 6G

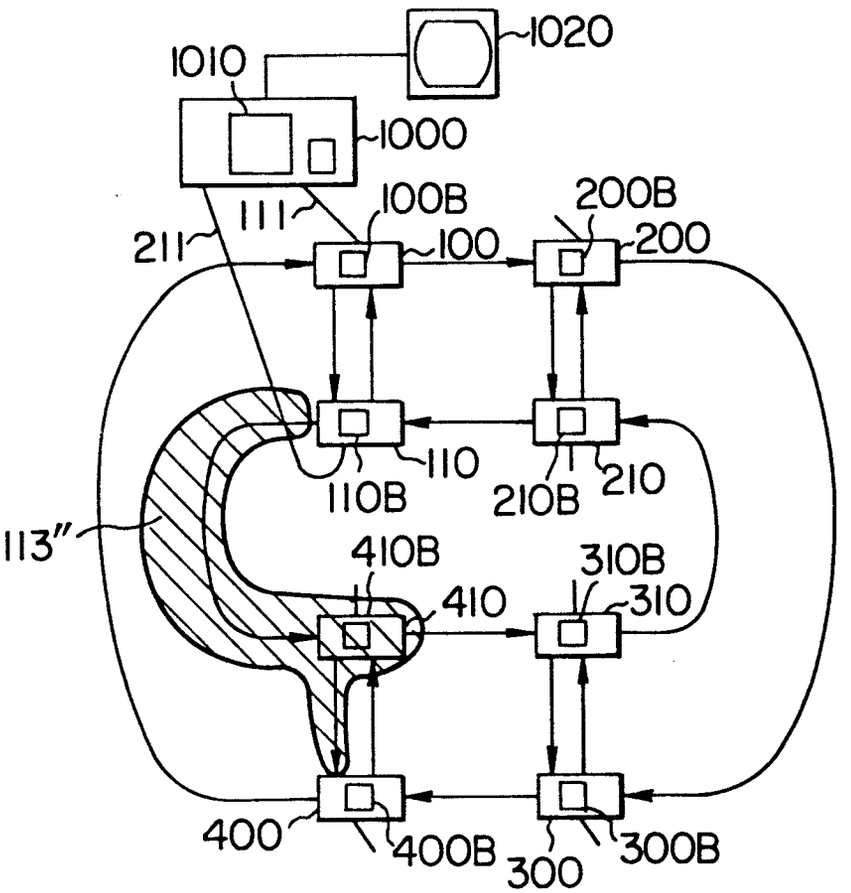

1020
1010
1000
111
100B
200B
211
100
200
110
110B
210B
210
113"
410B
310B
410
310
400
400B
300
300B

FIG. 7A

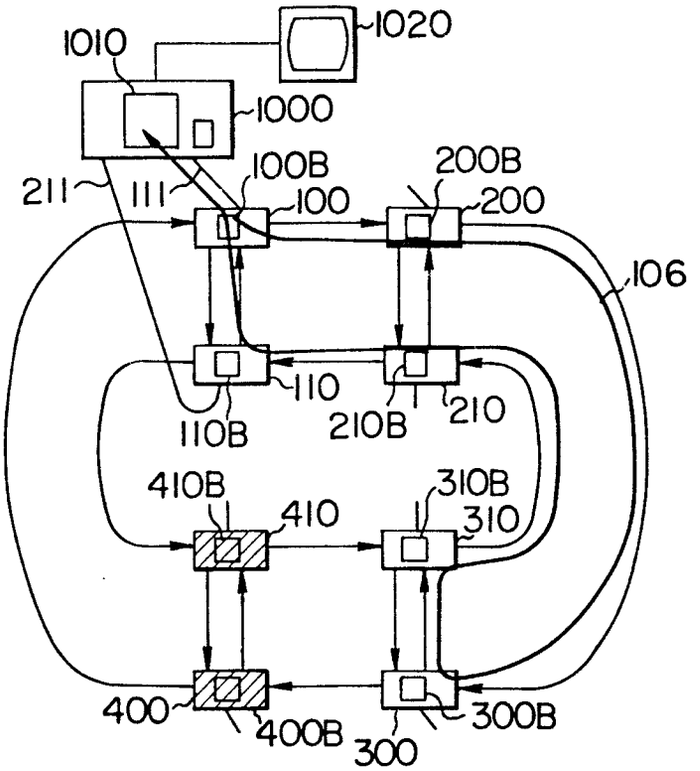

1020
1010
1000
100B
200B
211
111
100
200
106
110
210
110B
210B
410B
310B
410
310
400
400B
300
300B

FIG. 7B

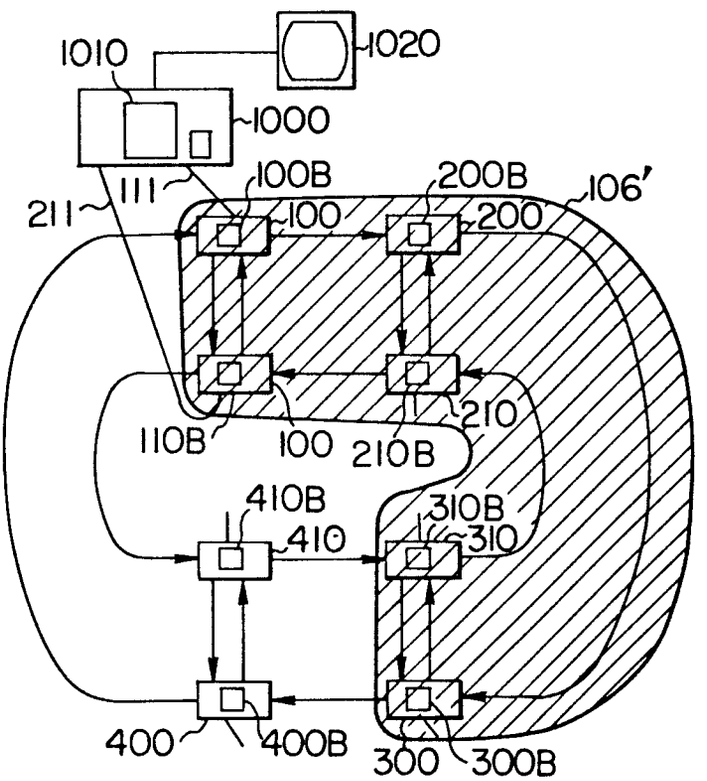

1020
1010
1000
100B
200B
106'
211
111
100
200
210
110B
100
210B
410B
310B
410
310
400
400B
300
300B

FIG. 8

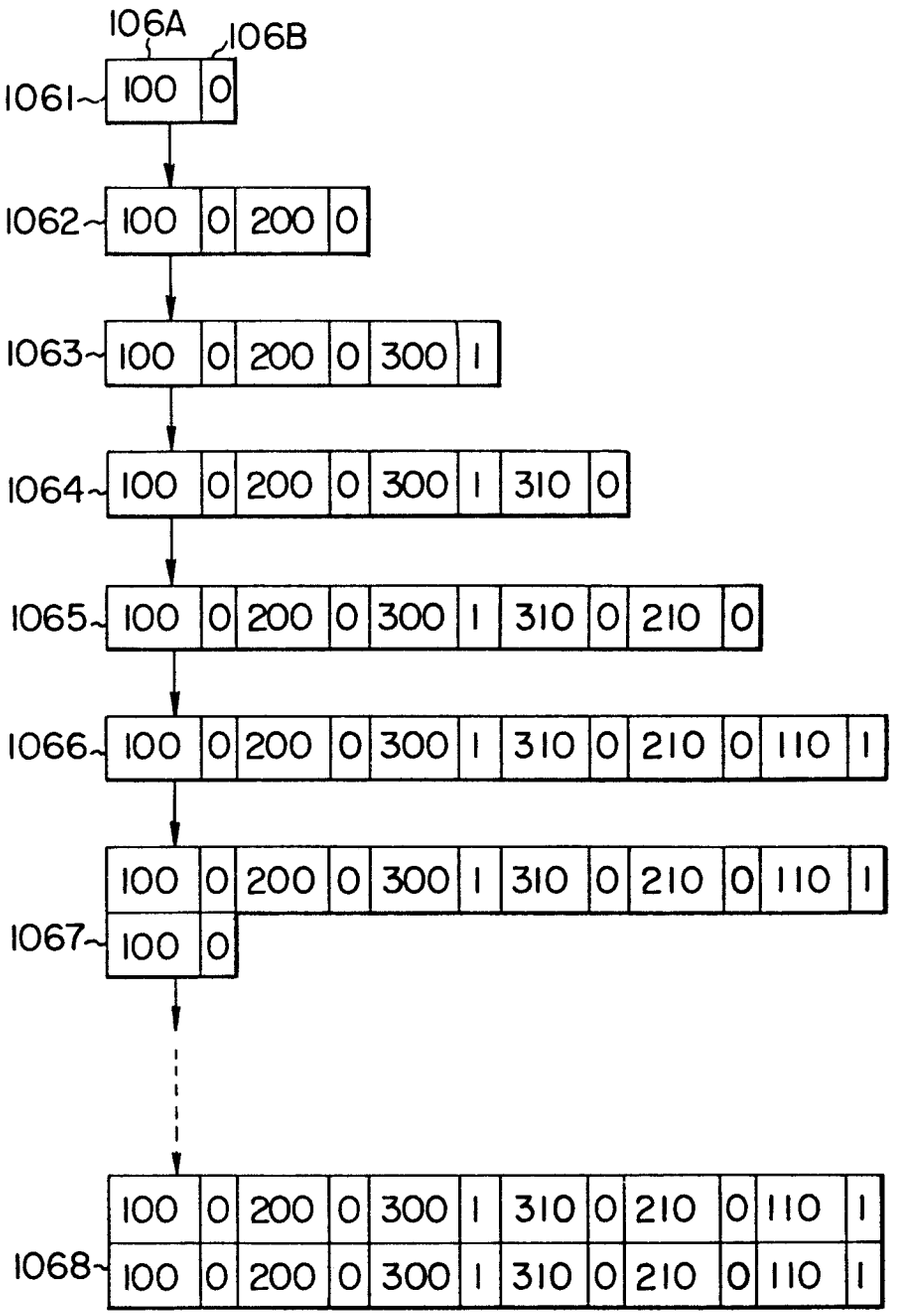

106A
106B
1061
100 0
1062
100 0 200 0
1063
100 0 200 0 300 1
1064
100 0 200 0 300 1 310 0
1065
100 0 200 0 300 1 310 0 210 0
1066
100 0 200 0 300 1 310 0 210 0 110 1
1067
100 0 200 0 300 1 310 0 210 0 110 1
100 0
1068
100 0 200 0 300 1 310 0 210 0 110 1
100 0 200 0 300 1 310 0 210 0 110 1

FIG. 9

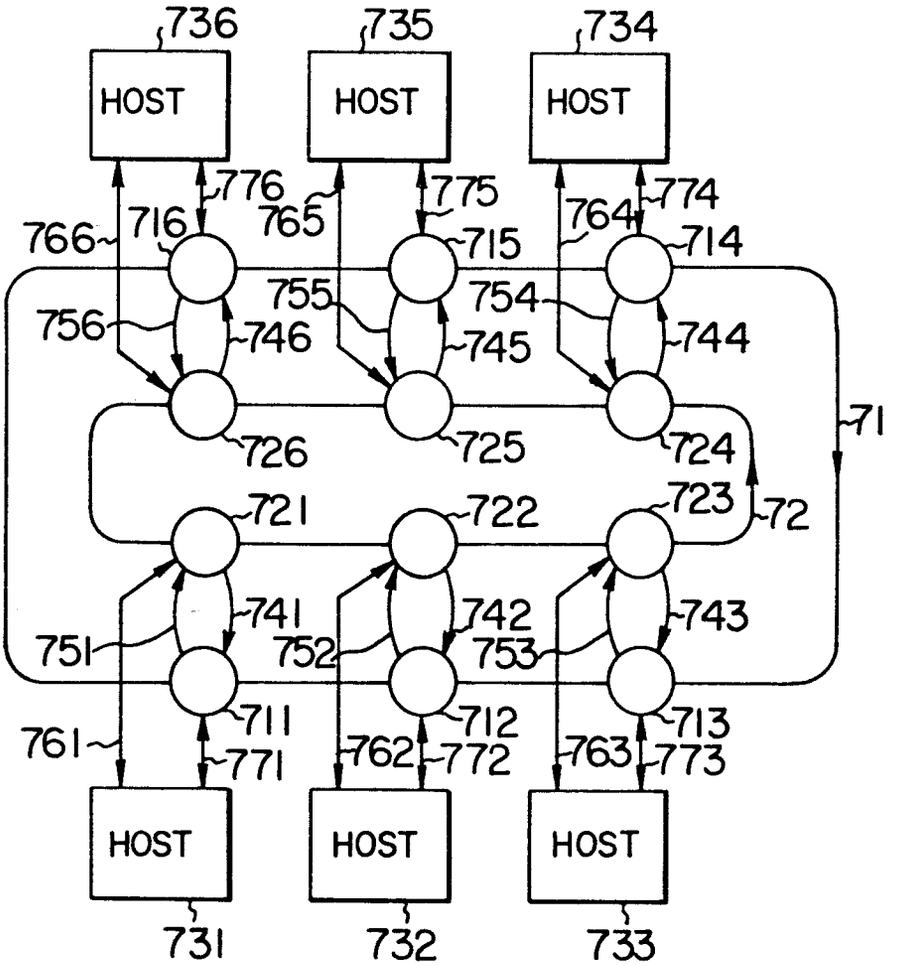

736
735
734
HOST
HOST
HOST
776
775
774
766
716
765
715
764
714
755
754
756
746
745
744
726
725
724
71
721
722
723
72
741
742
743
751
752
753
711
712
713
761
771
762
772
763
773
HOST
HOST
HOST
731
732
733

FIG. 10

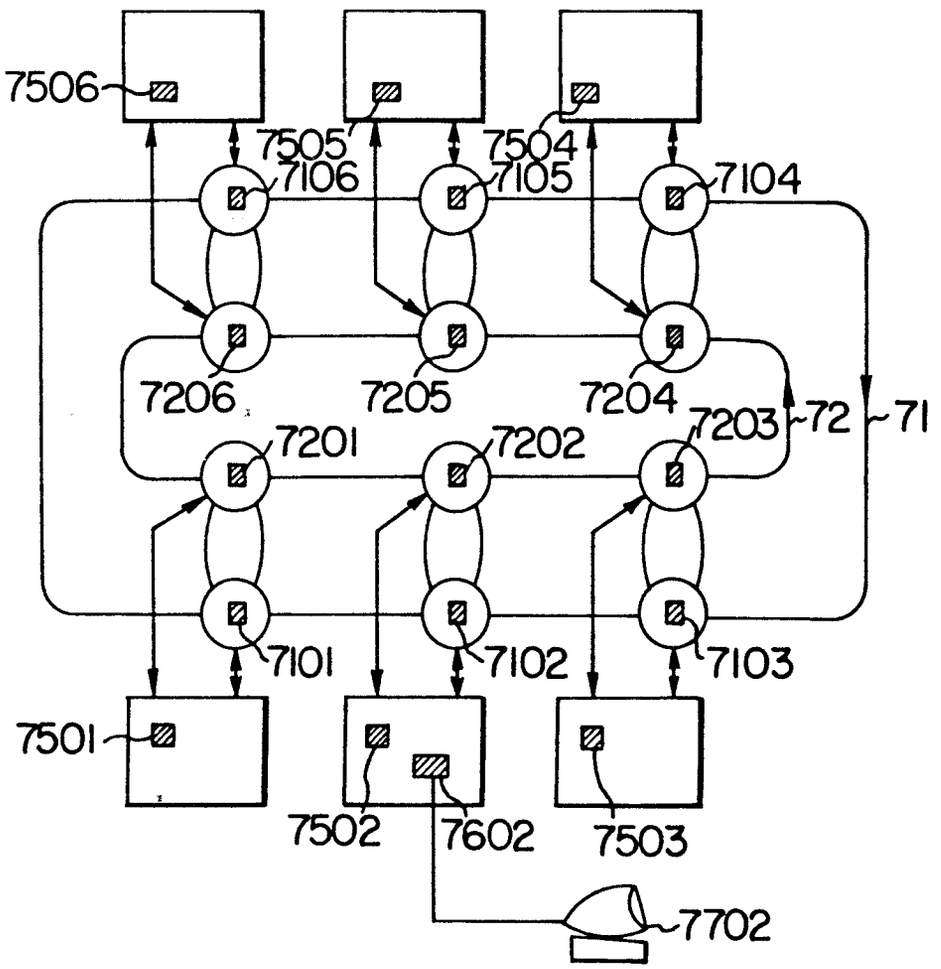

7506
7505
7504
7106
7105
7104
7206
7205
7204
7203
72
71
7201
7202
7101
7102
7103
7501
7502
7602
7503
7702

FIG. 11

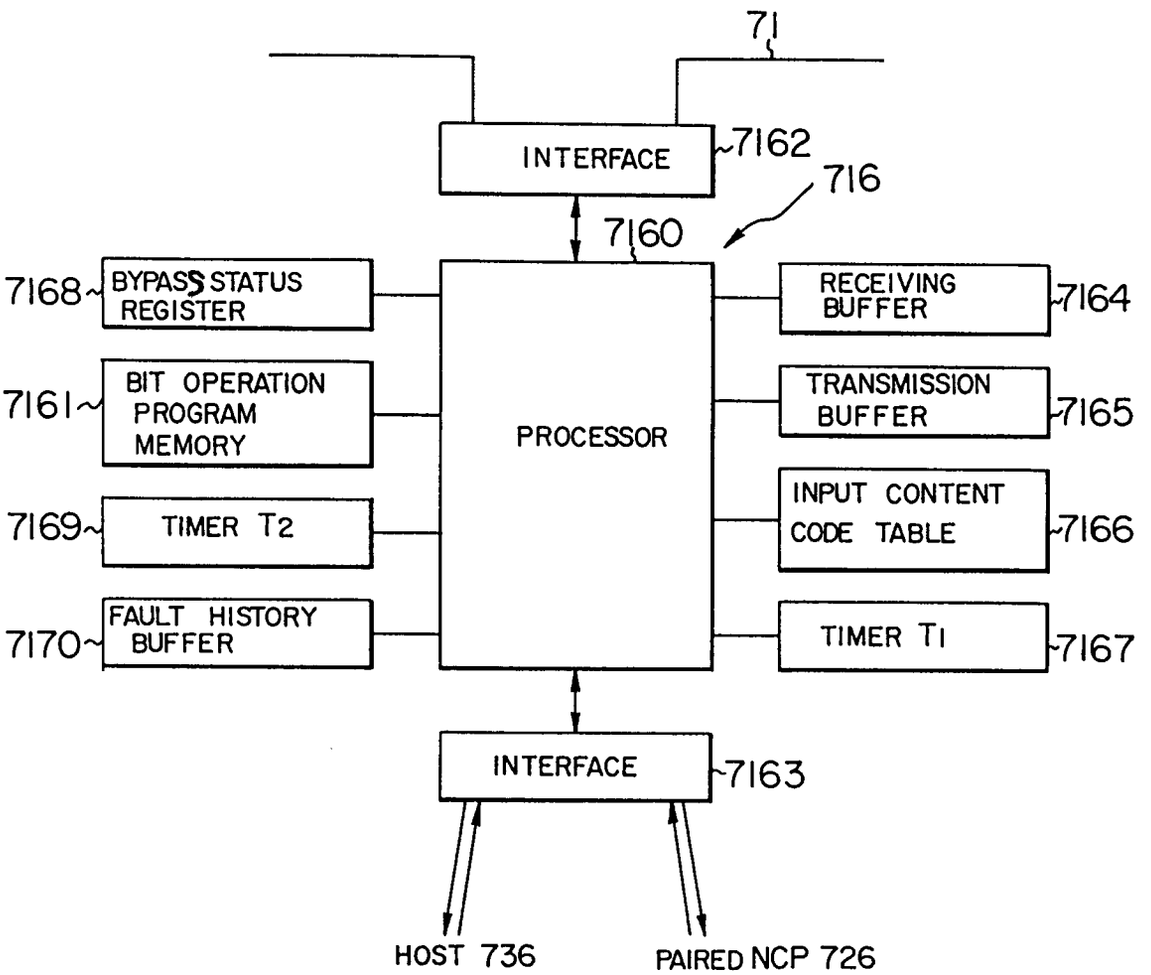

71
INTERFACE
7162
716
7160
7168
BYPASS STATUS REGISTER
7161
BIT OPERATION PROGRAM MEMORY
7169
TIMER T2
7170
FAULT HISTORY BUFFER
PROCESSOR
RECEIVING BUFFER
7164
TRANSMISSION BUFFER
7165
INPUT CONTENT CODE TABLE
7166
TIMER T1
7167
INTERFACE
7163
HOST 736
PAIRED NCP 726

FIG. 12

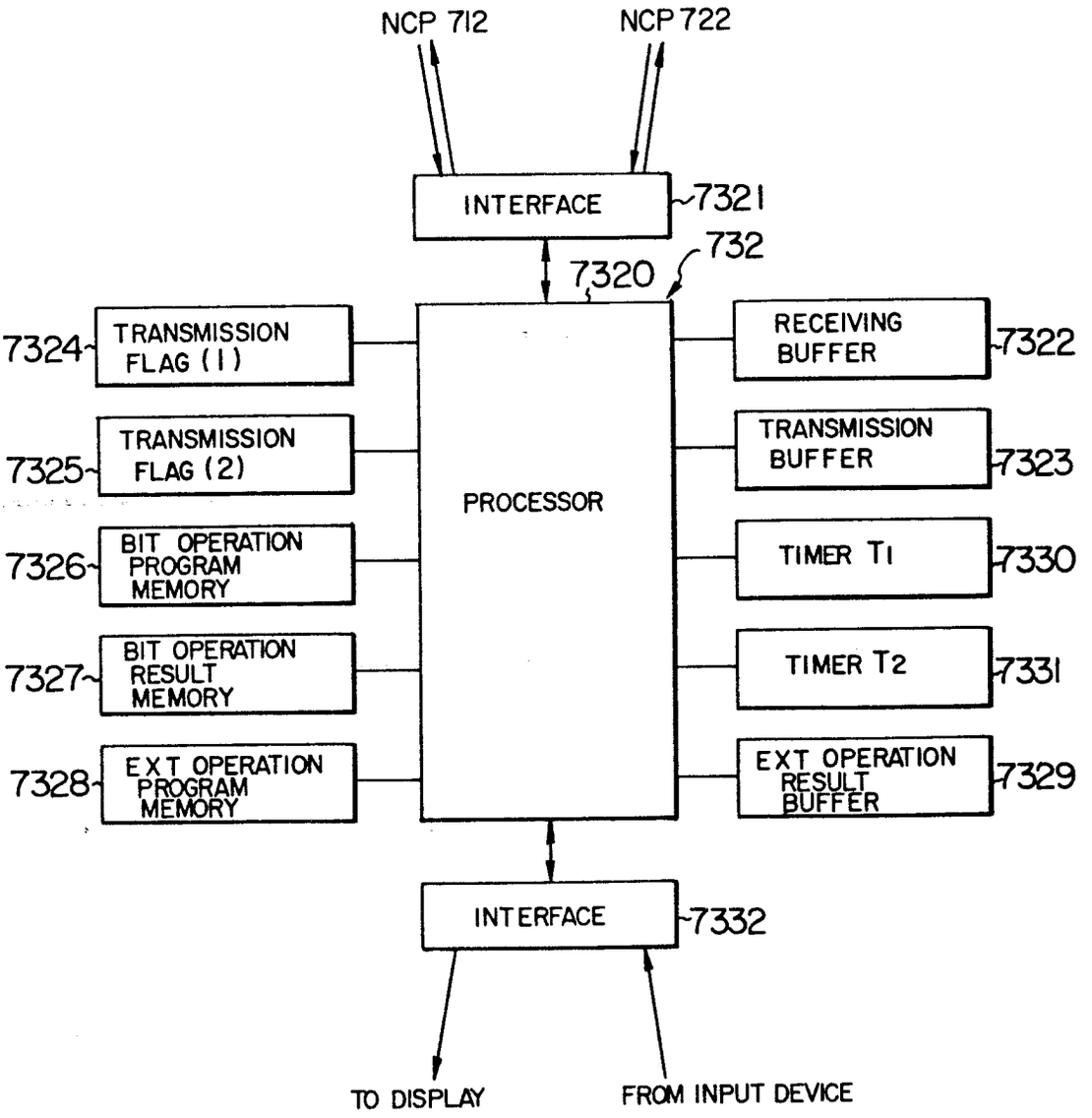

NCP 712
NCP 722
INTERFACE
7321
732
7320
7324
TRANSMISSION FLAG (1)
7325
TRANSMISSION FLAG (2)
7326
BIT OPERATION PROGRAM MEMORY
7327
BIT OPERATION RESULT MEMORY
7328
EXT OPERATION PROGRAM MEMORY
PROCESSOR
RECEIVING BUFFER
7322
TRANSMISSION BUFFER
7323
TIMER T1
7330
TIMER T2
7331
EXT OPERATION RESULT BUFFER
7329
INTERFACE
7332
TO DISPLAY
FROM INPUT DEVICE

FIG. 13A

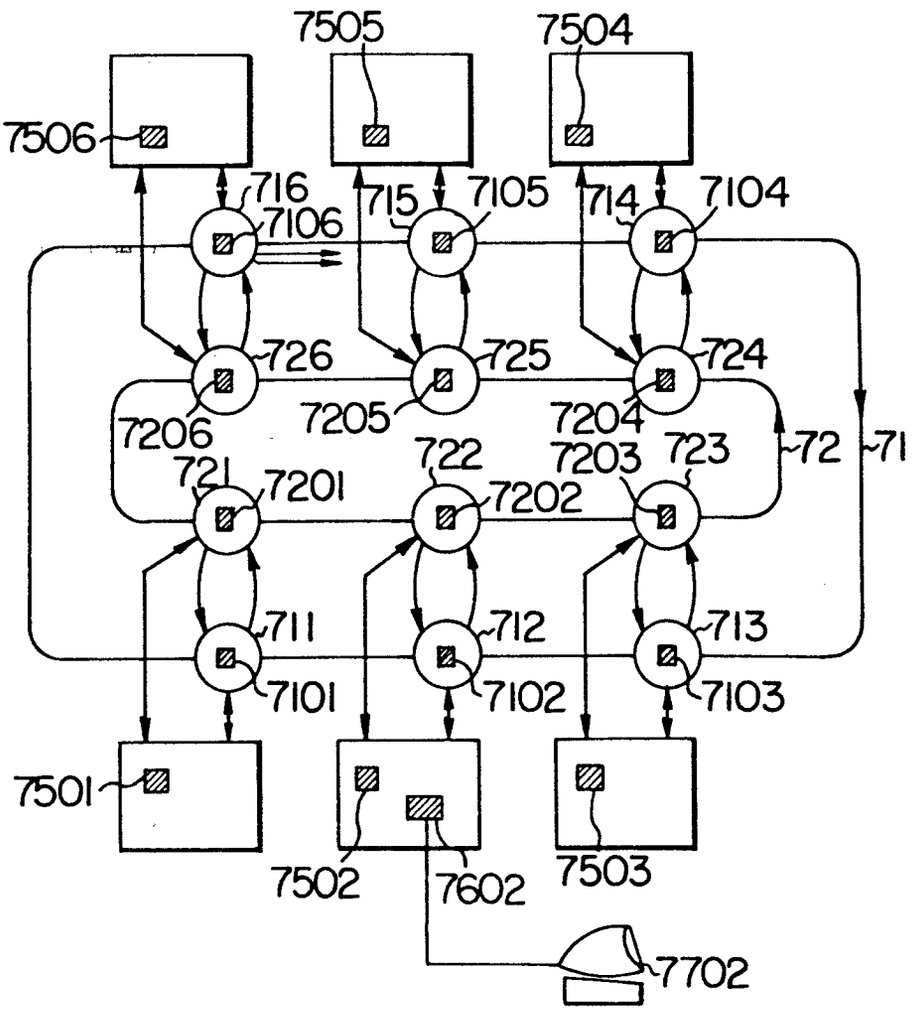

7505
7504
7506
716
7106
715
7105
714
7104
726
725
724
7206
7205
7204
72
71
721
7201
722
7202
7203
723
711
712
713
7101
7102
7103
7501
7502
7602
7503
7702

FIG. 13B

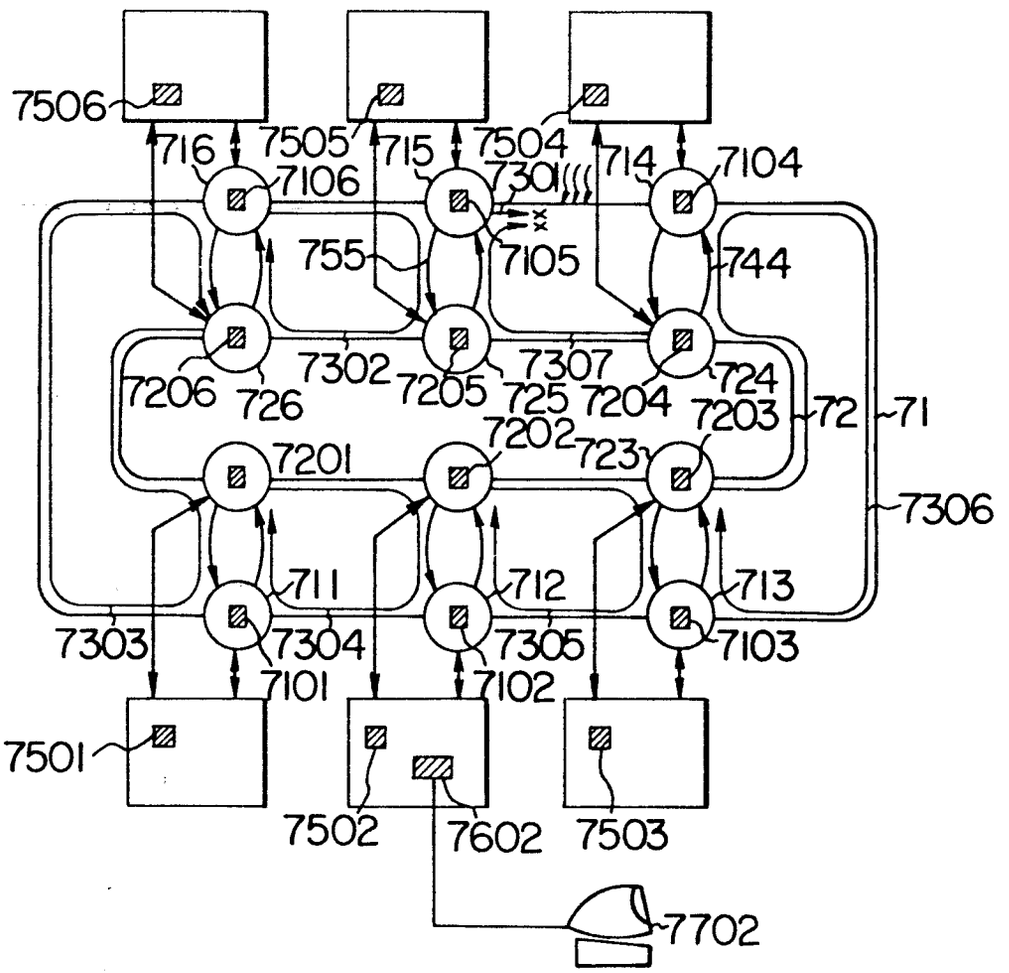

7506
7505
7504
716
715
714
7106
7301
7104
7105
755
744
7206
726
7302
7205
725
7307
7204
724
7203
72
71
7201
7202
723
7306
711
712
713
7303
7304
7305
7103
7101
7102
7501
7502
7602
7503
7702

FIG. 13C

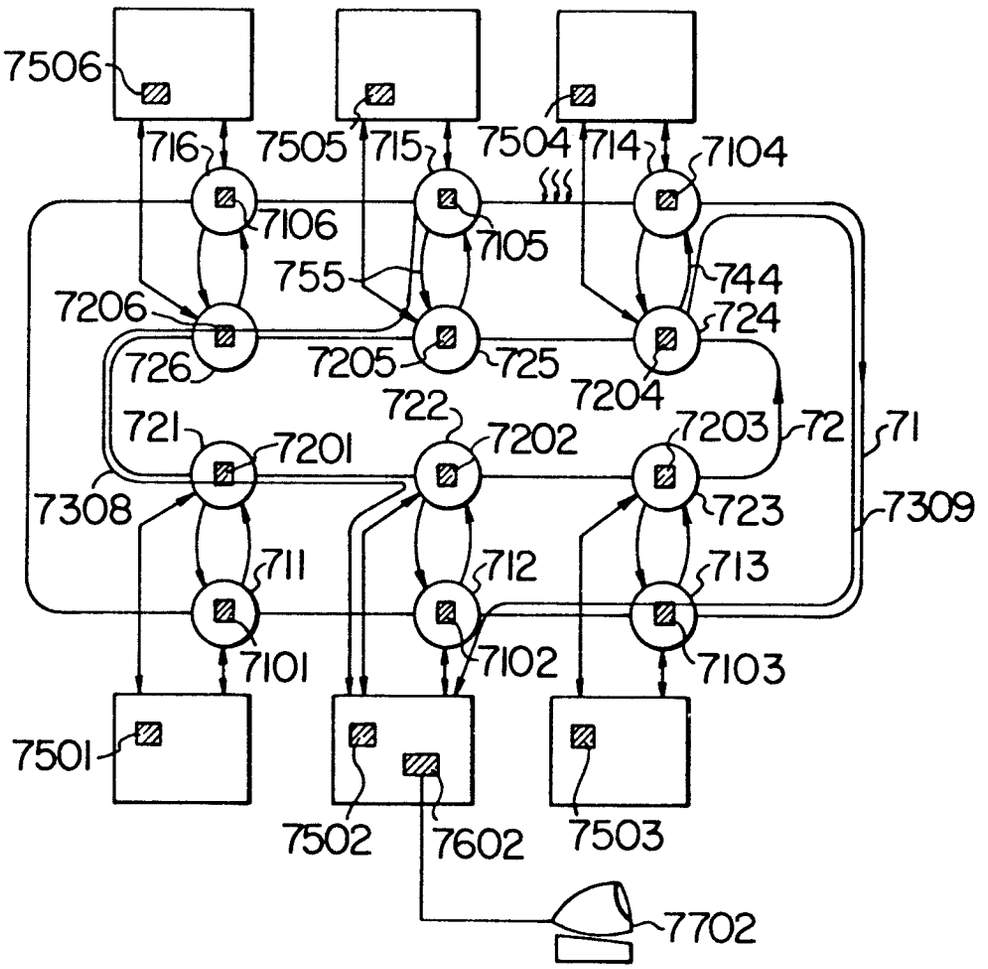

7506
716
7505
715
7504
714
7104
7106
7105
755
744
7206
724
726
7205
725
7204
722
721
7201
7202
7203
72
71
7308
723
7309
711
712
713
7101
7102
7103
7501
7502
7602
7503
7702

FIG. 13D

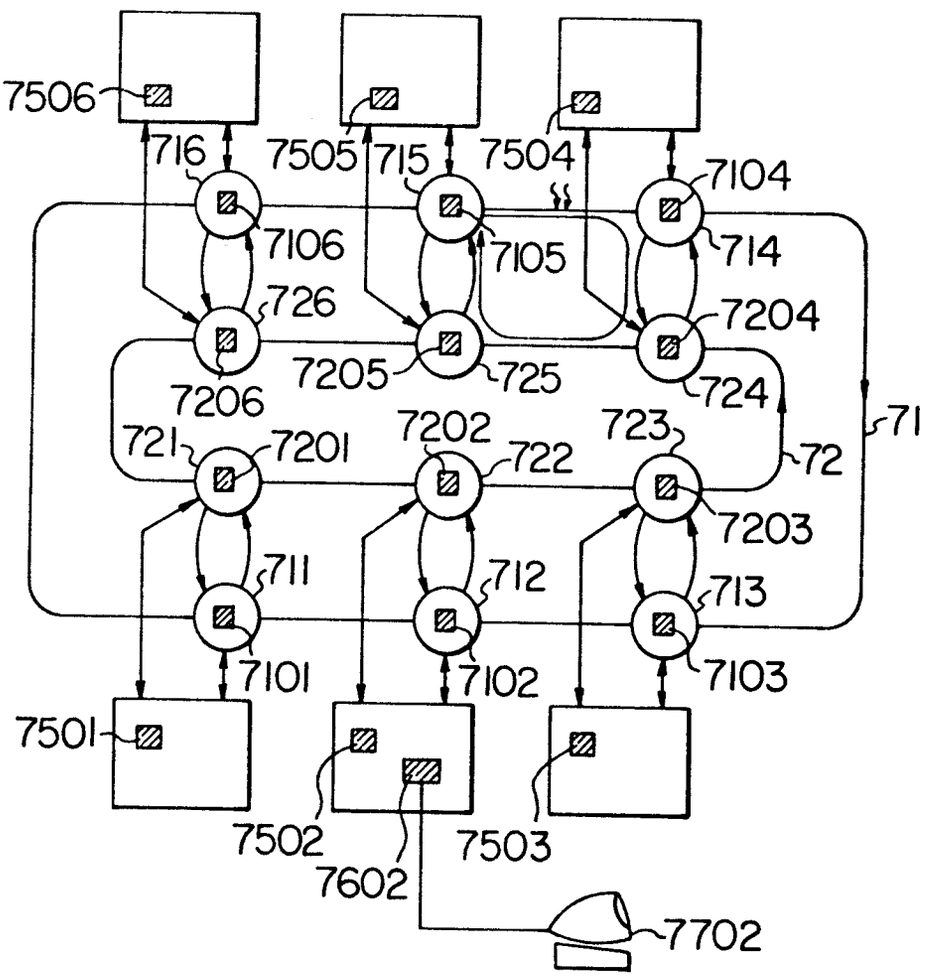

7506
716
7505
715
7504
7104
7106
7105
714
726
7204
7205
725
724
7206
71
721
7201
7202
722
723
72
7203
711
712
713
7101
7102
7103
7501
7502
7602
7503
7702

FIG. 14

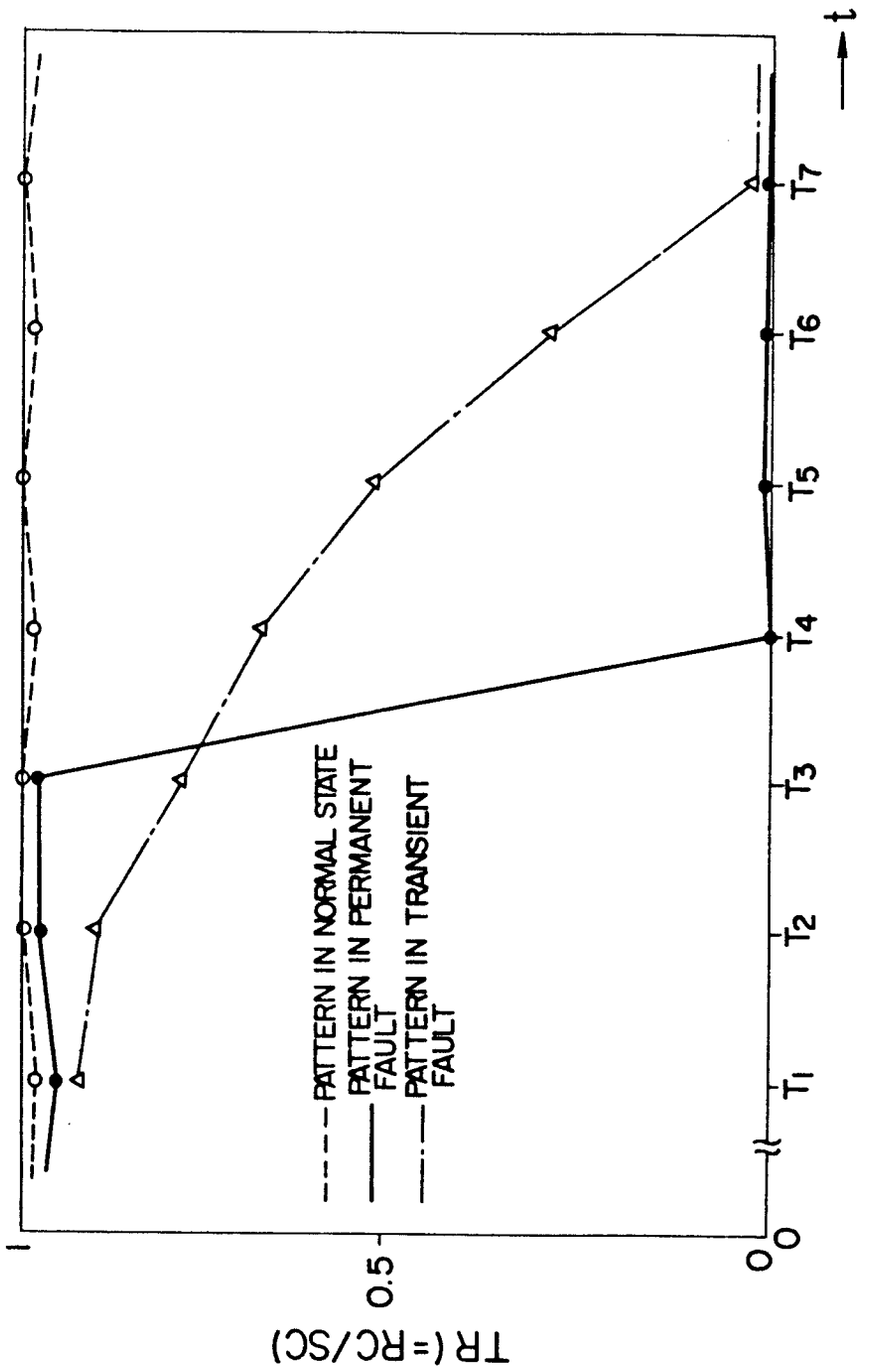

TR (=RC/SC)
1
0.5
0
0
T1
T2
T3
T4
T5
T6
T7
t
PATTERN IN NORMAL STATE
PATTERN IN PERMANENT FAULT
PATTERN IN TRANSIENT FAULT

FIG. 15

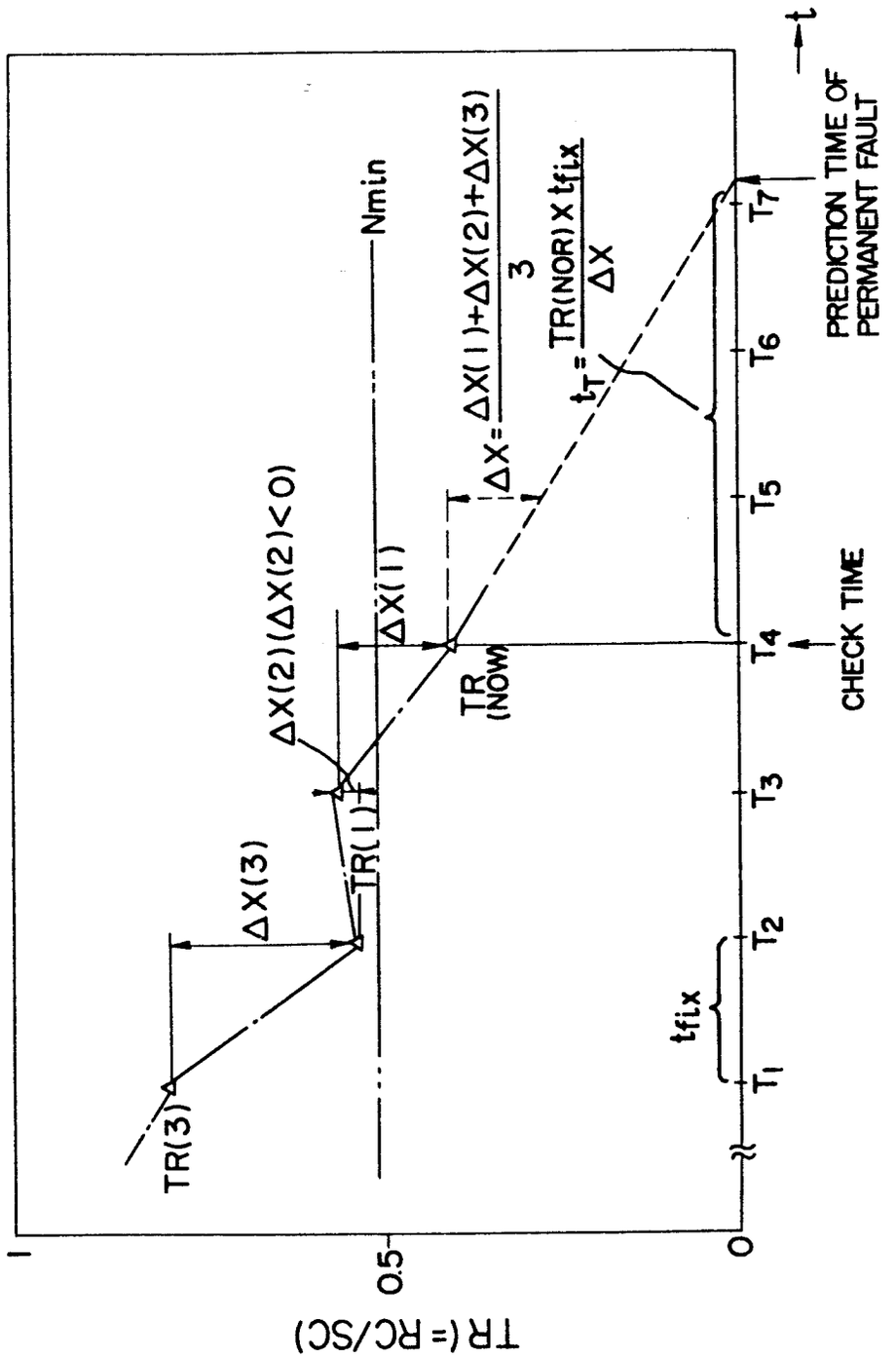
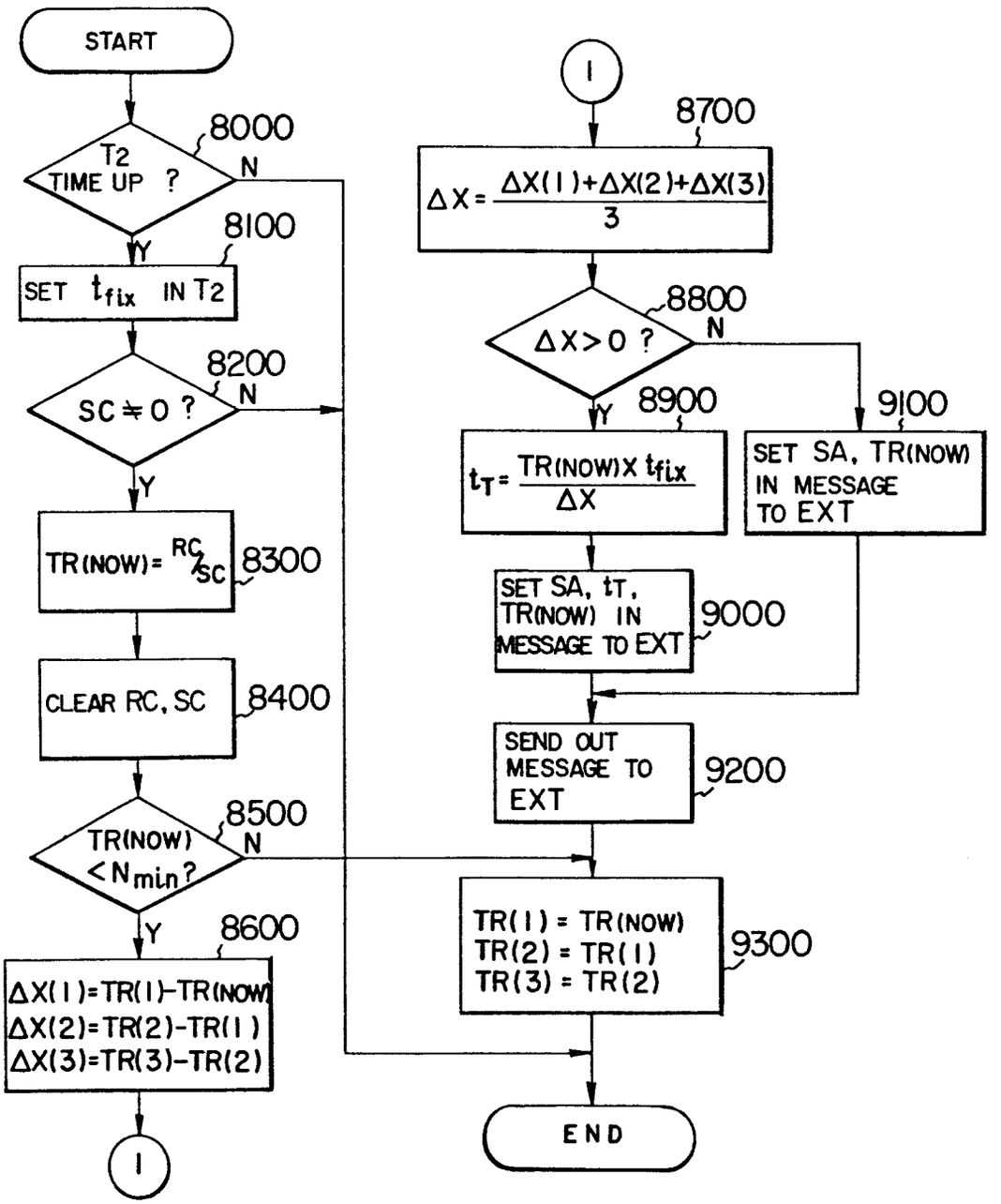

TR (= RC/SC)
1
0.5
0
t
T1
T2
T3
T4
T5
T6
T7
tfix
TR(3)
ΔX(3)
TR(1)
ΔX(2)(ΔX(2)<0)
ΔX(1)
Nmin
TR (NOW)
ΔX= ΔX(1)+ΔX(2)+ΔX(3) / 3
tT= TR(NOR) X tfix / ΔX
CHECK TIME
PREDICTION TIME OF PERMANENT FAULT

FIG. 16


START
8000
T2 TIME UP ?
N
Y
8100
SET t_{fix} IN T2
8200
SC ≒ 0 ?
N
Y
TR(NOW) = RC/SC
8300
CLEAR RC, SC
8400
8500
TR(NOW) < Nmin?
N
Y
8600
ΔX(1)=TR(1)-TR(NOW)
ΔX(2)=TR(2)-TR(1)
ΔX(3)=TR(3)-TR(2)
1
1
8700
ΔX = (ΔX(1)+ΔX(2)+ΔX(3))/3
8800
ΔX > 0 ?
N
Y
8900
t_T = TR(NOW) X t_{fix} / ΔX
9100
SET SA, TR(NOW) IN MESSAGE TO EXT
SET SA, tT, TR(NOW) IN MESSAGE TO EXT
9000
SEND OUT MESSAGE TO EXT
9200
TR(1) = TR(NOW)
TR(2) = TR(1)
TR(3) = TR(2)
9300
END