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(54) **Semiconductor memory device.**

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IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-13, no. 5, October 1978, pages 698-703, IEEE, New York, US; S.E. SCHUSTER: "Multiple word/bit line redundancy for semiconductor memories"

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Description

The present invention relates to a semiconductor memory device, in particular, it relates to a semiconductor memory device providing redundant cells.

Recently, the capacity of semiconductor memory devices has been and is being greatly increased, and this increase in the capacity of a semiconductor memory device leads to a high probability that some of the memory cells therein will be defective, thus rendering the entire memory defective. To alleviate this problem, there is known a method for providing redundant memory cells and of using these redundant memory cells to replace defective memory cells.

The provision of a large number of redundant cell groups is useful if a large number of defective memory cells are produced in a cell block. However, where defective memory cells are not produced, the provision of so many redundant cell groups is unnecessary, in that there is no use for them. Thus, usually, only one column or 2 to 3 columns of redundant cell groups are provided (per cell block). Further, in the conventional system, the redundant cell groups are linked exclusively to individual cell blocks.

When a redundant cell group is linked to an individual cell block, the following problems arise. That is, suppose that one column of redundant cells is provided for each cell block, and that two defective memory cells existing in different columns are produced in a first cell block but no defective cells are produced in a second cell block. In this case, although there are two redundant cell groups and two defective memory cells, the two redundant cell groups are linked to different cell blocks, and therefore, the redundant cell group in the second cell block cannot be used for the first cell block. Thus, only one redundant cell group can be utilised, to replace only one of the defective cells of the first cell block; the other defective cell cannot be replaced and the functioning of the memory device is deteriorated.

It is desirable to alleviate the above problem by providing a semiconductor memory device in which the redundant cell groups can be used freely by changing the linking of these cell groups to a particular cell block, and thus enabling a larger number of defective memory cells to be replaced by a smaller number of redundant cell groups.

PCT/US82/01826 discloses such a semiconductor memory device, in which spare columns of cells can be assigned to replace defective columns in any of eight bit segments. However, in this device, special column address switches are provided to activate each spare column in response to a column address of a defective column, and the outputs of the column address switches are multiplexed together with the output of normal columns of cells. As a result, there is a delay in accessing the device, and accesses take different times depending on whether a normal column or spare column is being accessed. US-A-4,346,459 discloses another such semiconductor memory device, which has special spare column select circuits which are switched during normal operation of the device, and hence has similar drawbacks.

According to the present invention there is provided a semiconductor memory device comprising: first and second cell blocks, each comprising a plurality of cell groups, each cell group comprising a plurality of memory cells; a redundant cell group comprising a plurality of memory cells; first and second data buses corresponding respectively to the first and second cell blocks; decoder circuitry for selecting one of the cell groups; and switching circuitry responsive to said decoder circuitry for connecting the redundant cell group to either of said first or second data buses corresponding to the first and second cell blocks; characterised in that the redundant cell group is arranged between the first and second cell blocks; each cell group is connected to the data bus corresponding to its block via a respective selection gate controlled by said decoder circuitry; and in that the switching circuitry comprises gates arranged, and controlled by said decoder circuitry, in parallel with said selection gates, and permanently-settable switch circuits for permanently connecting the redundant cell group to either of said first or second data buses.

Thus, by means of the present invention it is possible to provide flexibility in assigning redundant cell groups to defective cell groups, without adversely affecting the overall performance of the device.

Reference is made, by way of example, to the accompanying drawings in which:-

Figure 1 is a block diagram showing one example of a prior art semiconductor device;

Figure 2 is a block diagram showing a partially detailed portion of the device shown in Figure 1;

Figure 3 is a block diagram showing an embodiment of the present invention;

Figures 4A, 4B, and 4C are circuit diagrams showing partially detailed portions of the device shown in Fig. 3;

Figure 5 is another embodiment corresponding to Fig. 4B;

Figure 6 is a flowchart explaining the operation of the device shown in Figs. 4A, 4B, and 4C; and

Figure 7 is a block diagram showing the present invention applied to a memory device having a multi-bit connection.

Figure 1 shows one example of a conventional

semiconductor memory device providing redundant cells. In Fig. 1, 10 and 12 represent cell blocks and 14 and 16 redundant cell groups. As is already known, the cell blocks 10 and 12 arrange the memory cells at cross points of many word lines and bit lines (or row lines and column lines), and Y_o to Y_n are signals for selecting the bit lines. The word lines (not shown in the drawing), extend in a horizontal direction, and redundant cells are provided for one bit line (1 column) and are selected by a selection signal Y_a. Numerals 18 and 20 are data buses and 22 and 24 are I/O (input output) buffers. This memory is organized for 2 bit output, so that when memory cells are selected by any address, the corresponding memory cells in cell blocks 10 and 12 are read out, and one bit from each I/O buffer 22 and 24, i.e., a total of two bits, are output at the same time.

As the cell blocks and the redundant cell groups are selected by the same address, for simplicity, it is preferable that the word lines are commonly used. Figure 2 shows such a construction, in which WL shows a word line and BL shows a bit line, each are shown as only one line or as a pair of lines. MC is a memory cell, and in Fig. 2, a static random access memory (SRAM) is shown as an example, wherein the MC is formed by a flip-flop. RD is a row decoder, which receives word line selection addresses $A_o \sim A_n$ and selects a word line WL when these addresses are at a low (L) level. The word lines WL extend over the cell block 10, the redundant cell groups 14, 16, and the cell block 12, and each word line WL is selected at the same time by the word line address. The I/O buffers include a sense amplifier SA and an input (write) data buffer O/N, etc.

These memory devices are tested during manufacture, and when defective cells are found in the cell block, the defective address informations are written in a read-only memory (ROM) (not shown in the drawings). If a defective address is selected while the memory is in use, a column decoder which outputs $Y_o \sim Y_n$ is made noneffective (all outputs of the decoder are made at a low level), and a signal Y_a for selecting a redundant cell group is generated. The word lines are common to the cell blocks and redundant cell groups, so that the memory cells on the word lines for the redundant memory cell groups are selected instead of the defective memory cells.

The provision of a large number of redundant cell groups is useful if a large number of defective memory cells are produced in the cell block. However, where defective memory cells are not produced, the provision of so many redundant cell groups is unnecessary, in that there is no use for them. Thus, usually, only one column or 2 ~ 3 columns of the redundant cell groups are provided. Further, in the conventional system, the redundant cell groups are linked exclusively to an individual cell block. That is, as shown in Fig. 1, the redundant cell group 14 is linked to cell block 10 and the redundant cell group 16 is linked to cell block 12. This is determined by to which data bus the redundant cell group is connected.

When a redundant cell group is linked to a cell block in such a manner, the following problems arise. That is, suppose that one column of the redundant cells is provided for each cell block, and that two defective memory cells linked to different columns are produced in cell block 10 but no defective cells are produced in cell block 12. In this case, although there are two redundant cell groups and two defective memory cells, the two redundant cell groups are linked to different cell blocks, and therefore, the redundant cell group 16 cannot be used for cell block 10. Thus, only one redundant cell group 14 can be used to replace one defective cell , and therefore, the other defective memory cell cannot be replaced and the functioning of the memory device is impaired.

Figure 3 shows an embodiment of the present invention in which the same elements as in Fig. 1 are designated by the same symbols. As is clear from a comparison of Figs. 1 and 3, in the present invention, switches $S_1 \sim S_3$ are provided to connect the redundant cell groups 14 and 16 to either of the data buses 18 and 20. Immediately after the memory device is manufactured, the switches $S_1 \sim S_3$ are open. When no defective memory cell are found in the cell block 10, the redundant cell group 14 is not used, and when the defective memory cell exists in a column in the cell block 10, the switch S_2 is closed and the defective memory cell can be replaced by the redundant cell group 14. The same applies to the cell block 12. Up to this point, the device is similar to the conventional system. However, if two defective memory cells are produced in cell block 10, over two columns and no defective memory cell exists in cell block 12, such a case cannot be handled in the conventional system, but can be dealt with in the present invention, as shown below. That is, when the above feature occurs; the switches S_1 and S_2 are closed. Therefore, the redundant cell group 16 is linked to cell block 10, so that the defective memory cell belonging to one column of cell block 10 can be replaced by the redundant cell group 14, and the defective memory cell belonging to another column of the memory cell group 10 can be replaced by the redundant cell group 16. Therefore, the functioning of the memory device remains unimpaired.

When the defective memory cells occur in two columns in the cell block 12, and no defective memory cells occur in the cell block 10, switches S_1 and S_3 are closed. Thus, as mentioned above,

the redundant cells replace the defective memory cell, and functioning of the memory device remains unimpaired.

Since the switches S_1 ~ S_3 are initially open, and are closed only when necessary, the switches may be comprised of a poly-crystalline silicon fuse. When a switch is to be closed, the fuse is melted by supplying a current or by a laser beam. The switches S_1 ~ S_3 are initially open and are closed only when necessary, therefore the structure as shown in Figs. 4A and 4C may be used.

Figure 4A shows details of the switching circuit shown in Fig. 3. In Fig. 4A, gate transistors 41a, 42a, 43a; 41b, 42b, 43b; ... 41n, 42n, 43n are connected to Y decoders i, j, ... k, respectively, and gate transistors 44, 45 and 46 are connected between I/O inputs (data buses) (1) and (2). One terminal of each transistor 42a and 42b is connected to the transistor 47, one terminal of each transistor 43a and 43b is connected via transistors 48 and 49 to the transistor 42n, and the transistor 41n is connected to the transistor 50. The transistors 44 and 47 are controlled by an input from a fuse terminal F_a , the transistors 46 and 49 are controlled by an input from a fuse terminal F_b , and the transistors 45 and 50 are controlled by an input from a fuse terminal F_c.

Figure 4B shows the construction of the fuse (ROM) in each Y decoder wherein, in Fig. 4B, 51a and 52a represent a high resistance,53a and 54a represent fuses, and 50a represents a gate circuit which receives the outputs of the fuse shown in (b) and (c) of Fig. 4B. Figure 4C shows the construction of the fuses (Fa, Fb, Fc) which correspond to the sequences (groups) of the redundant cells. In Fig. 4C, 55 ~ 57 represent high resistances, and 58 ~ 60 represent fuses.

Next, referring to Figs. 4A, 4B, and 4C, the case in which column i in cell block (1) and column k in cell block (2) are replaced by the redundant cells will be explained. In this case, the fuse 53a corresponding to $\overline{F_{1i}}$ (53a) and the fuse 58 corresponding to F_a are melted, so that the sequence of redundant cells a replaces the column i in the cell block (1). Further, the fuse corresponding to $\overline{F_{2k}}$ and the fuse 59 corresponding to F_b are melted, so that the sequence of redundant cells b replaces the column k in the cell block (2).

Next, an explanation will be given for the case in which the columns i and j in the cell block (1) are replaced by the redundant cells. In this case, the fuse 53a corresponding to $\overline{F_{1i}}$ (53a) and the fuse 58 corresponding to F_a are melted so that the sequence of the redundant cells a replaces the column i in the cell block (1). Further, the fuse corresponding to $\overline{F_{1j}}$ and the fuse 60 corresponding to F_c are melted so that the sequence of the redundant cells b replaces the column j in the cell block (1).

In Figs. 4B and 4C, fuses are made of material such as poly-crystalline silicon, and the transistors are field effect transistors (FETs). As shown in Figs. 4B and 4C, the gate of the transistor is connected via the fuse F to ground, so that it is in an OFF state. When the fuse F is melted, the transistor is pulled up via the high resistances such as 51a, ..., 55, etc. to the electric source V_c , so that it becomes in an ON state. When the fuse F is not melted, the current flows from the electric source V_c via the high resistance and the fuse to ground. However, if the high resistance is used as the resistor R, this current can be decreased to a small value such as of the order of a pico ampere.

Figure 5 is another embodiment corresponding to Fig. 4B. In Fig. 4B, if one fuse such as 53a is melted, the signal F_i becomes "L" automatically, so that the transistor 41a is OFF. However, in the embodiment shown in Fig. 5, the structure is such that if at least one fuse corresponding to fuse 53a or 54a is melted, the fuse corresponding to 61a also melts, so that the signal F_i becomes "L" and the transistor 41a is OFF.

Figure 6 is a flowchart showing the operation of the device shown in Figs. 4A ~ 4C. In block 71, if a failure is detected, block 71 is transferred to block 72. In block 72, if one column in block 1 is detected, the fuse corresponding to the failed column i and the fuse F_a are melted in block 73, so that the entire device is tested (block 74). In block 72, if more than one failed column occurs in block 1, block 72 is transferred to block 75 and the failed columns are examined. When the failed columns are columns i and j in block (1), the fuses corresponding to $\overline{F_{1i}}$, $\overline{F_{1j}}$ (F_i , F_j), and F_a, F_b are melted in block 76, the failed columns are replaced by the redundant cells, and the entire device is tested (block 77) .

The memory device may have a one bit organization by which one memory cell is selected by one address,or a plurality bit organization by which a plurality of cells are selected at the same time by one address. Figures 1 and 3 show a memory having a two bit construction, and a multibit organization such as 8 bits may exist in a 64 KRAM. In this case, as shown in Fig. 7, the number of cell blocks and I/O buffers provided corresponds to the number of bits. In the Figure , 10A, 12A, ..., 12D are cell blocks and 22A, 24A, ..., 24D are I/O buffers. In this case, for example four circuits as shown in Fig. 2 may be provided, so that a 64 KRAM having an 8 K x 8 bits organization can be obtained. 14A, 16A, ... 16D are redundant cell groups corresponding to each cell block. In this example, the redundant cell groups 14A and 16A can be connected to the cell blocks 10A or 12A, however, they cannot be connected to another cell

block, for example, 12D. For the purpose of improving this point and increasing the connection flexibility of the redundant cell groups to any block, wire connections may be provided along the data buses 18 and 20 for switching the redundant cell groups to other cell blocks also. However, the connection layout then becomes rather complex.

As explained above, in the present invention, the redundant cell groups are not exclusively linked to a cell block but can be connected to any other cell block. Therefore, the present invention can deal with a frequent occurrence of defective memory cells in a cell block without increasing the number of redundant cell groups needed, and thus, the present invention is very effective for carrying out the stated purpose.

Claims

1. A semiconductor memory device comprising:

first and second cell blocks (10,12), each comprising a plurality of cell groups, each cell group comprising a plurality of memory cells;

a redundant cell group (14) comprising a plurality of memory cells;

first and second data buses (18,20) corresponding respectively to the first and second cell blocks (10,12);

decoder circuitry for selecting one of the cell groups;

and switching circuitry (51,52,S_1,S_2,S_3) responsive to said decoder circuitry for connecting the redundant cell group to either of said first or second data buses (18,20) corresponding to the first and second cell blocks (10,12); characterised in that:-

the redundant cell group (14) is arranged between the first and second cell blocks;

each cell group is connected to the data bus (18,20) corresponding to its block via a respective selection gate controlled by said decoder circuitry; and in that

the switching circuitry comprises gates (51,52) arranged, and controlled by said decoder circuitry, in parallel with said selection gates, and permanently-settable switch circuits (S_1,S_2,S_3) for permanently connecting the redundant cell group to either of said first or second data buses.

2. A device as claimed in claim 1, comprising at least one additional cell block, the switching circuitry being operable to link the redundant cell group to any of the cell blocks.

3. A device as claimed in claim 2, comprising at least one additional redundant cell group (16), the switching circuitry being operable to link the or each additional redundant cell group to any of the cell blocks (10,12).

4. A device as claimed in claim 1, having at least one additional cell block and at least one additional redundant cell group (16), the redundant cell groups (14,16) being associated with respective sets, for example pairs, of cell blocks, and the switching circuitry being operable to link a redundant cell group to any member of its associated set of cell blocks.

5. A device as claimed in claim 1, 2, 3 or 4, wherein said permanently-settable switch circuits comprise a first switch (S_1) which is connected between third and fourth data buses corresponding to a first group (14) of redundant cells and a second group (16) of redundant cells respectively, a second switch (S_2) which is connected between said first (18) and third data buses and a third switch which is connected between second (20) and fourth data buses; wherein, when the first group (14) of redundant cells is linked to the first cell block (10), said first switch (S_1) is permanently open and said second switch (S_2) is permanently closed; and when the first group (14) of redundant cells and the second group (16) of redundant cells are linked to said first cell block (10), said first switch (S_1) and said second switch (S_2) are permanently closed and said third switch (S_3) is permanently open.

6. A semiconductor memory device according to claim 5, wherein each of said first, second and third switches (S_1,S_2,S_3) is formed by a field effect transistor (44,45,46), and each is provided with a ROM element (55,58;56,59;57,60).

7. A semiconductor memory device according to claim 6, wherein each of said ROM elements includes a series circuit of a high resistance (55,56,57) and a fuse (58,59,60) formed by poly-crystalline silicon connected between a power source terminal and a ground terminal, such that, when said fuse is melted, a voltage (Vc) at said power source terminal is applied to a control gate of said field effect transistor (44,45,46) so that said field effect transistor is placed in a permanent ON state.

Revendications

1. Dispositif de mémoire à semiconducteur comprenant :

des premier et second blocs de cellules (10, 12), chacun comprenant une pluralité de groupes de cellules, chaque groupe de cellules

comprenant une pluralité de cellules de mémoire ;

un groupe de cellules redondantes (14) comprenant une pluralité de cellules de mémoire ;

des premier et second bus de données (18, 20) correspondant respectivement aux premier et second blocs de cellules (10, 12) ;

un circuit décodeur permettant de sélectionner un des groupes de cellules ; et

un circuit de commutation (51, 52, S_1, S_2, S_3,) sensible audit circuit décodeur pour relier le groupe de cellules redondantes à l'un ou l'autre desdits premier et second bus de données (18, 20) qui correspond aux premier et second blocs de cellules (10, 12) ;

caractérisé en ce que :

le groupe de cellules redondantes (14) est disposé entre les premier et second blocs de cellules ;

chaque groupe de cellules est connecté au bus de données (18, 20) qui correspond à son bloc via une porte de sélection commandée par ledit circuit décodeur ; et en ce que

le circuit de commutation comprend des portes (51, 52) qui sont disposées en parallèle auxdites portes de sélection et qui sont commandées par ledit circuit décodeur ainsi que des circuits d'interrupteur qui peuvent être positionnés de manière permanente (S_1, S_2, S_3) pour connecter de manière permanente le groupe de cellules redondantes à l'un ou l'autre desdits premier et second bus de données.

2. Dispositif selon la revendication 1, comprenant au moins un bloc de cellules supplémentaire, le circuit de commutation pouvant fonctionner pour relier le groupe de cellules redondantes à n'importe lequel des blocs de cellules.

3. Dispositif selon la revendication 2, comprenant au moins un groupe de cellules redondantes supplémentaire (16), le circuit de commutation pouvant fonctionner pour relier le ou chaque groupe de cellules redondantes supplémentaire à n'importe lequel des blocs de cellules (10, 12).

4. Dispositif selon la revendication 1, ayant au moins un bloc de cellules supplémentaire et au moins un groupe de cellules redondantes supplémentaire (16), les groupes de cellules redondantes (14, 16) étant associés à des jeux respectifs, par exemple des paires, de blocs de cellules, et le circuit de commutation pouvant fonctionner pour relier un groupe de cellules redondantes à n'importe quel élément de son jeu associé de blocs de cellules.

5. Dispositif selon la revendication 1, 2, 3 ou 4, dans lequel lesdits circuits d'interrupteur qui peuvent être positionnés de manière permanente comprennent un premier interrupteur (S_1) qui est connecté entre des troisième et quatrième bus de données correspondant respectivement à un premier groupe (14) de cellules redondantes et à un second groupe (16) de cellules redondantes, un second interrupteur (S_2) qui est connecté entre lesdits premier (18) et troisième bus de données et un troisième interrupteur qui est connecté entre les second (20) et quatrième bus de données ; dans lequel, lorsque le premier groupe (14) de cellules redondantes est relié au premier bloc de cellules (10), ledit premier interrupteur (S_1) est ouvert de manière permanente et ledit second interrupteur (S_2) est fermé de manière permanente ; et lorsque le premier groupe (14) de cellules redondantes et le second groupe (16) de cellules redondantes sont reliés audit premier bloc de cellules (10), ledit premier interrupteur (S_1) et ledit second interrupteur (S_2) sont fermés de manière permanente et ledit troisième interrupteur (S_3) est ouvert de manière permanente.

6. Dispositif de mémoire à semiconducteur selon la revendication 5, dans lequel chacun desdits premier, second et troisième interrupteurs (S_1, S_2, S_3) est formé par un transistor à effet de champ (44, 45, 46) et chacun est muni d'un élément de ROM (mémoire morte) (55, 58 ; 56, 59 ; 57, 60).

7. Dispositif de mémoire à semiconducteur selon la revendication 6, dans lequel chacun desdits éléments de ROM comporte un circuit série qui est constitué par une résistance élevée (55, 56, 57) et par un fusible (58, 59, 60) réalisé en silicium polycristallin, ce circuit étant connecté entre une borne de source d'alimentation et une borne de mise à la masse de telle sorte que lorsque ledit fusible est fondu, une tension (V_c) présente au niveau de ladite borne de source d'alimentation est appliquée à une grille de commande dudit transistor à effet champ (44, 45, 46) afin que ledit transistor à effet de champ soit placé dans un état passant permanent.

Patentansprüche

1. Halbleiterspeichervorrichtung mit:

ersten und zweiten Zellenblöcken (10, 12), die jeweils eine Vielzahl von Zellengruppen umfassen, von denen jede Zellengruppe eine Vielzahl von Speicherzellen umfaßt;

einer redundanten Zellengruppe (14), die eine Vielzahl von Speicherzellen umfaßt;

ersten und zweiten Datenbussen (18, 20), die den ersten bzw. zweiten Zellenblöcken (10, 12) entsprechen;

einer Decoderschaltung zum Auswählen einer der Zellengruppen;

und Schaltungskreisen (51, 52, S_1, S_2, S_3), die auf die genannte Decoderschaltung ansprechen, um die redundante Zellengruppe mit einem der genannten ersten oder

zweiten Datenbusse (18, 20) zu verbinden, die den ersten und zweiten Zellenblöcken (10, 12) entsprechen; dadurch gekennzeichnet, daß:-

die redundante Zellengruppe (14) zwischen den ersten und zweiten Zellenblöcken angeordnet ist;

jede Zellengruppe mit dem Datenbus (18, 20), der ihrem Block entspricht, über ein entsprechendes Auswahlgatter verbunden ist, das durch die genannte Decoderschaltung gesteuert wird; und daß

die Schaltungskreise Gatter (51, 52), die parallel zu den genannten Auswahlgattern angeordnet und durch die genannte Decoderschaltung gesteuert werden, und permanent setzbare Schaltkreise (S_1, S_2, S_3), zum permanenten Verbinden der redundanten Zellengruppen mit einem der genannten ersten oder zweiten Datenbusse, umfassen.

2. Vorrichtung nach Anspruch 1, mit wenigstens einem zusätzlichen Zellenblock, wobei die Schaltungskreise betreibbar sind, uni die redundante Zellengruppe mit irgendeinem der Zellenblöcke zu verbinden.

3. Vorrichtung nach Anspruch 2, mit wenigstens einer zusätzlichen redundanten Zellengruppe (16), wobei die Schaltungskreise betreibbar sind, um die oder jede zusätzliche redundante Zellengruppe mit irgendeinem der Zellenblökke (10, 12) zu verbinden.

4. Vorrichtung nach Anspruch 1, mit wenigstens einem zusätzlichen Zellenblock und wenigstens einer zusätzlichen redundanten Zellengruppe (16), wobei die redundanten Zellengruppen (14, 16) entsprechenden Sätzen, z.B. Paaren, von Zellenblöcken zugeordnet sind, und die Schaltungskreise betreibbar sind, um eine redundante Zellengruppe mit irgendeinem Teil des ihr zugeordneten Satzes von Zellenblöcken zu verbinden.

5. Vorrichtung nach Anspruch 1, 2, 3 oder 4, bei der die permanent setzbaren Schaltkreise einen ersten Schalter (S_1) umfassen, der zwischen dritten und vierten Datenbussen verbunden ist, die einer ersten Gruppe (14) von redundanten Zellen bzw. einer zweiten Gruppe (16) von redundanten Zellen entsprechen, einen zweiten Schalter (S_2), der zwischen den genannten ersten (18) und dritten Datenbussen verbunden ist, und einen dritten Schalter, der zwischen zweiten (20) und vierten Datenbussen verbunden ist; bei der dann, wenn die erste Gruppe (14) von redundanten Zellen mit dem ersten Zellenblock (10) verbunden wird, der genannte erste Schalter (S_1) permanent offen und der genannte zweite Schalter (S_2) permanent geschlossen ist; und dann, wenn die erste Gruppe (14) von redundanten Zellen und die zweite Gruppe (16) von redundanten Zellen mit dem genannten ersten Zellenblock (10) verbunden werden, der genannte erste Schalter (S_1) und der genannte zweite Schalter (S_2) permanent geschlossen sind und der genannte dritte Schalter (S_3) permanent offen ist.

6. Halbleiterspeichervorrichtung nach Anspruch 5, bei der jeder der ersten, zweiten und dritten Schalter (S_1, S_2, S_3) durch einen Feldeffekttransistor (44, 45, 46) gebildet ist, und jeder ist mit einem ROM-Element (55, 58; 56, 59; 57, 60) versehen.

7. Halbleiterspeichervorrichtung nach Anspruch 6, bei der jedes der genannten ROM-Elemente eine Reihenschaltung von einem hohen Widerstand (55, 56, 57) und ein Schmelzelement (58, 59, 60), das aus polykristallinem Silizium gebildet ist, enthält, verbunden zwischen einem Energiequellenanschluß und einem Erdanschluß, so daß dann, wenn das Schmelzelement geschmolzen wird, eine Spannung (Vc) bei dem genannten Energiequellenanschluß auf ein Steuergate des genannten Feldeffekttransistors (44, 45, 46) aufgebracht wird, so daß der genannte Feldeffekttransistor in einen permanenten EIN-Zustand gebracht wird.

Fig. 1

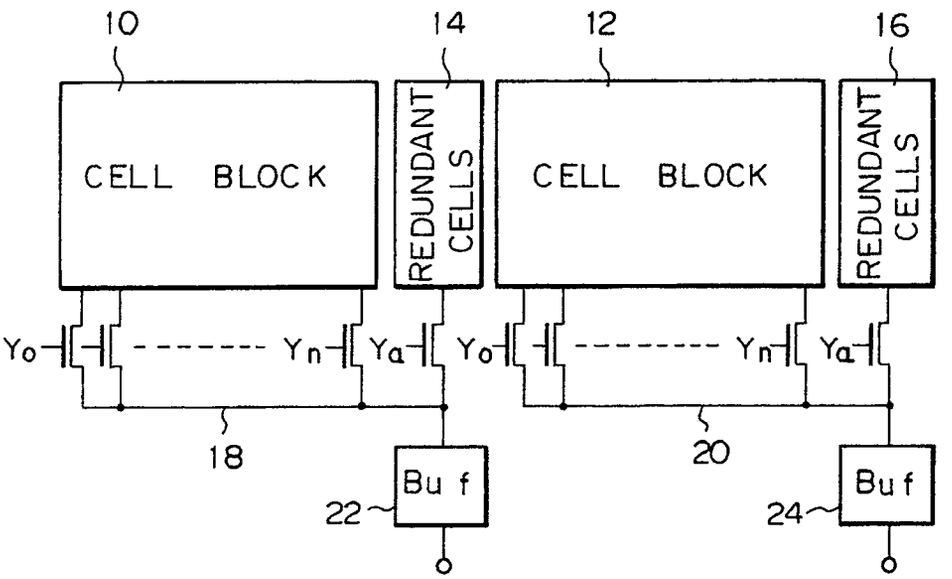

10
14
12
16
CELL BLOCK
REDUNDANT CELLS
CELL BLOCK
REDUNDANT CELLS
Yo
Yn
Ya
Yo
Yn
Ya
18
20
Buf
Buf
22
24

Fig. 2

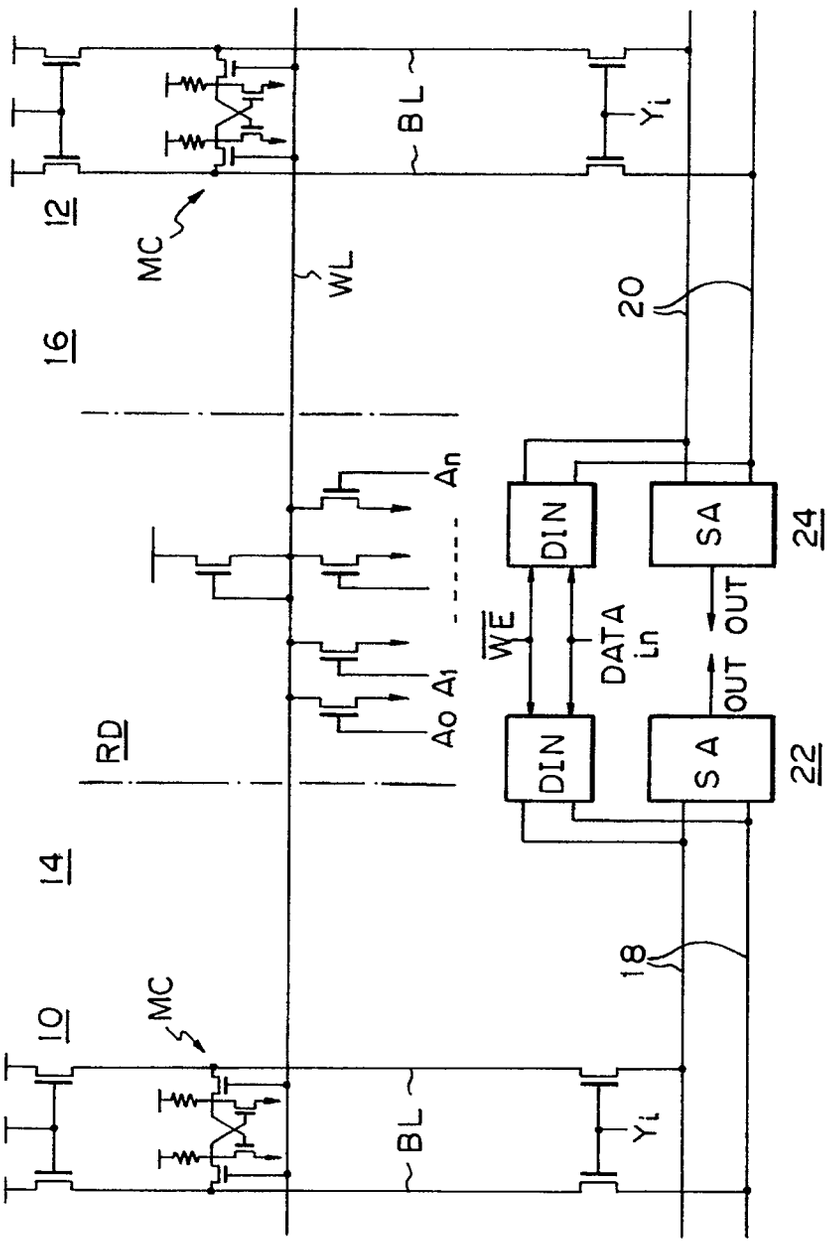

12
MC
WL
BL
Yi
16
20
An
Ai
Ao
RD
14
DIN
SA
24
WE
DATA in
OUT
OUT
DIN
SA
22
18
10
MC
BL
Yi

Fig. 3

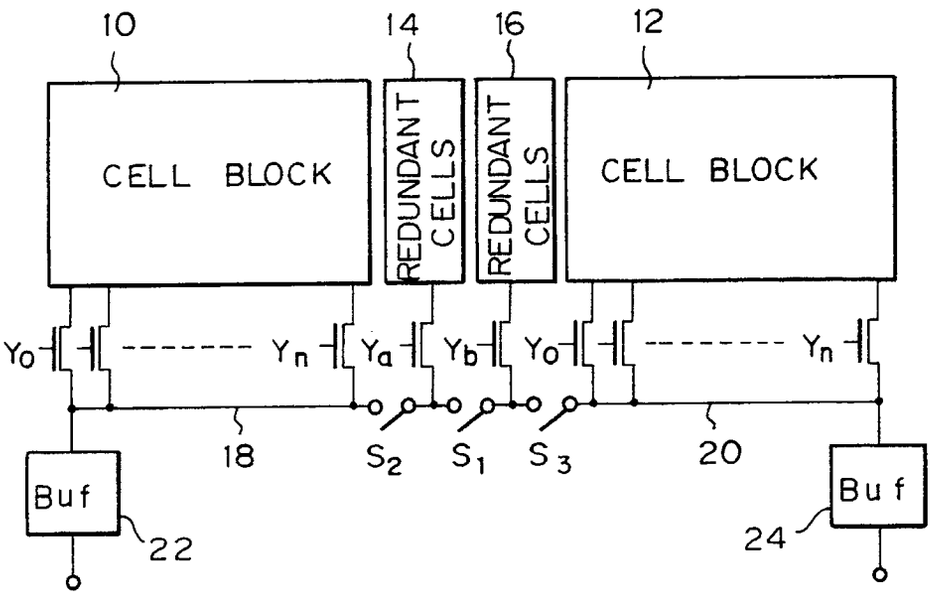

10
14
16
12
CELL BLOCK
REDUNDANT CELLS
REDUNDANT CELLS
CELL BLOCK
Y0
Yn
Ya
Yb
Y0
Yn
18
S2
S1
S3
20
Buf
22
Buf
24

Fig. 4A

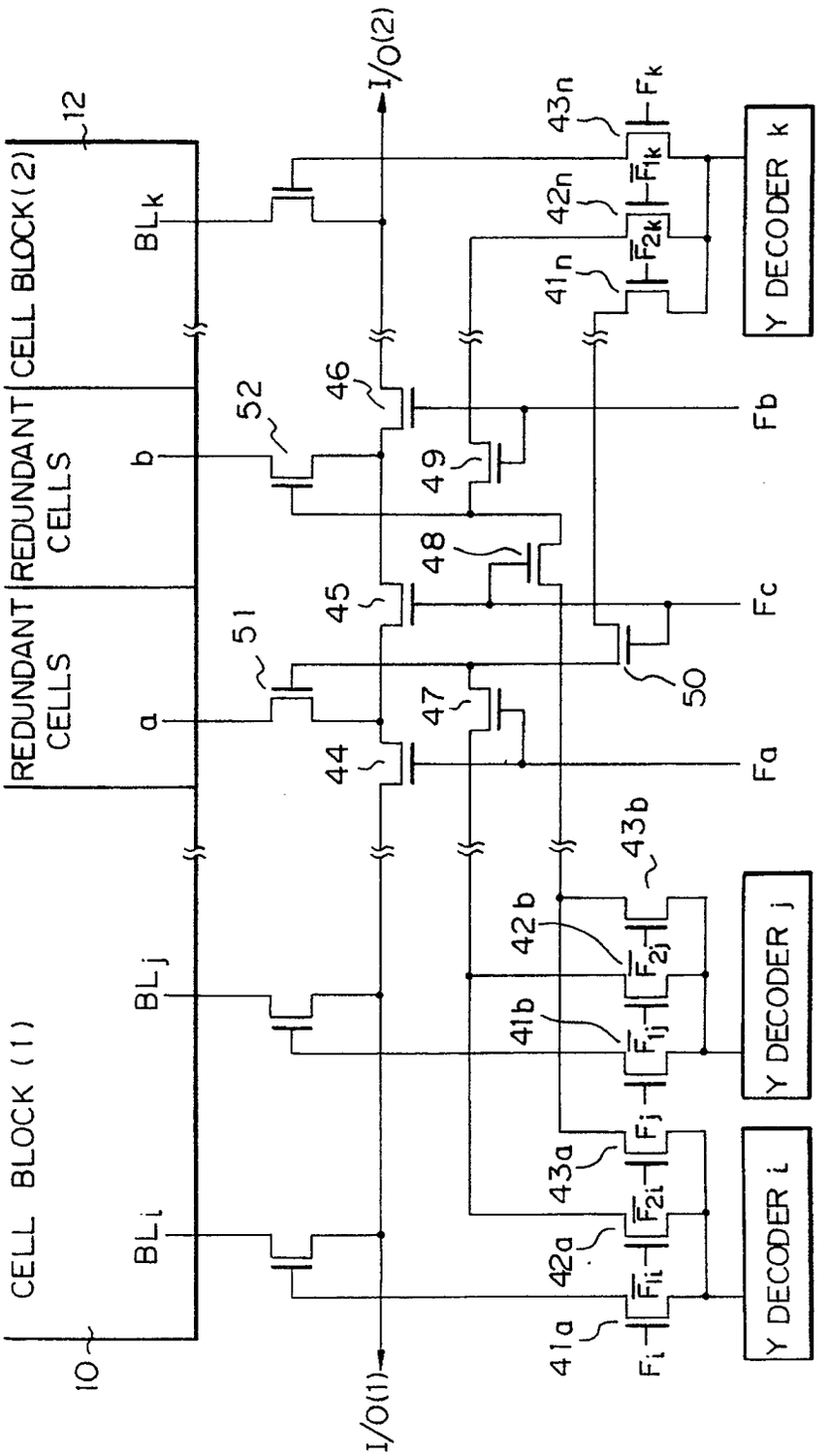

CELL BLOCK (1)
CELL BLOCK (2)
REDUNDANT CELLS
REDUNDANT CELLS
I/O(1)
I/O(2)
Y DECODER i
Y DECODER j
Y DECODER k
Fa
Fb
Fc
10
12
a
b
BLi
BLj
BLk
41a
41b
41n
42a
42b
42n
43a
43b
43n
44
45
46
47
48
49
50
51
52

Fig. 4B

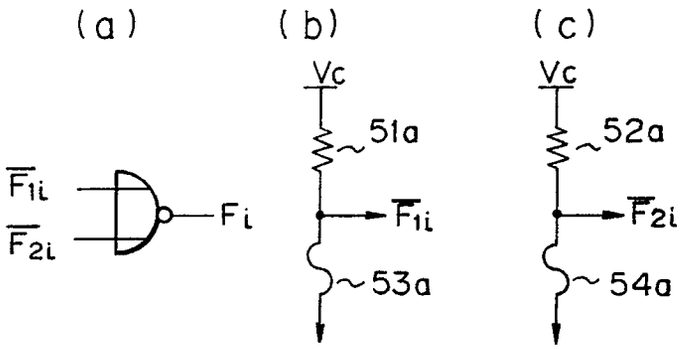


Fig. 4C

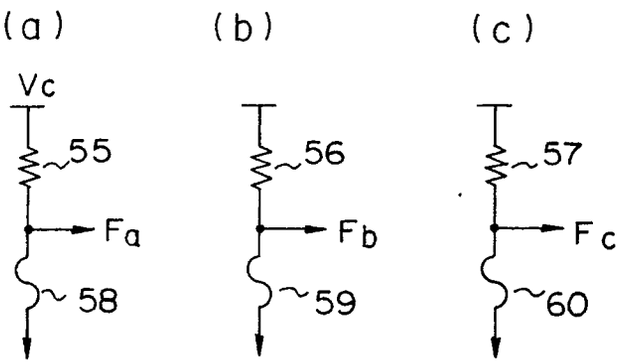


Fig. 5

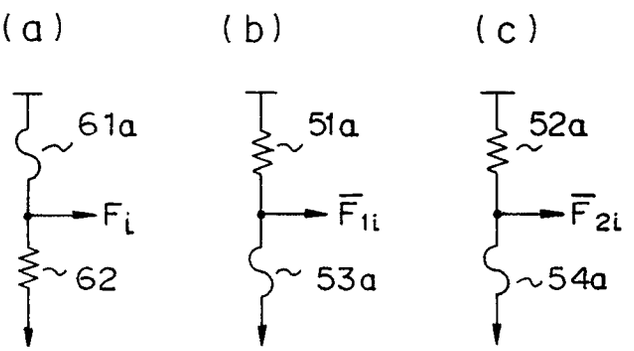


Fig. 6

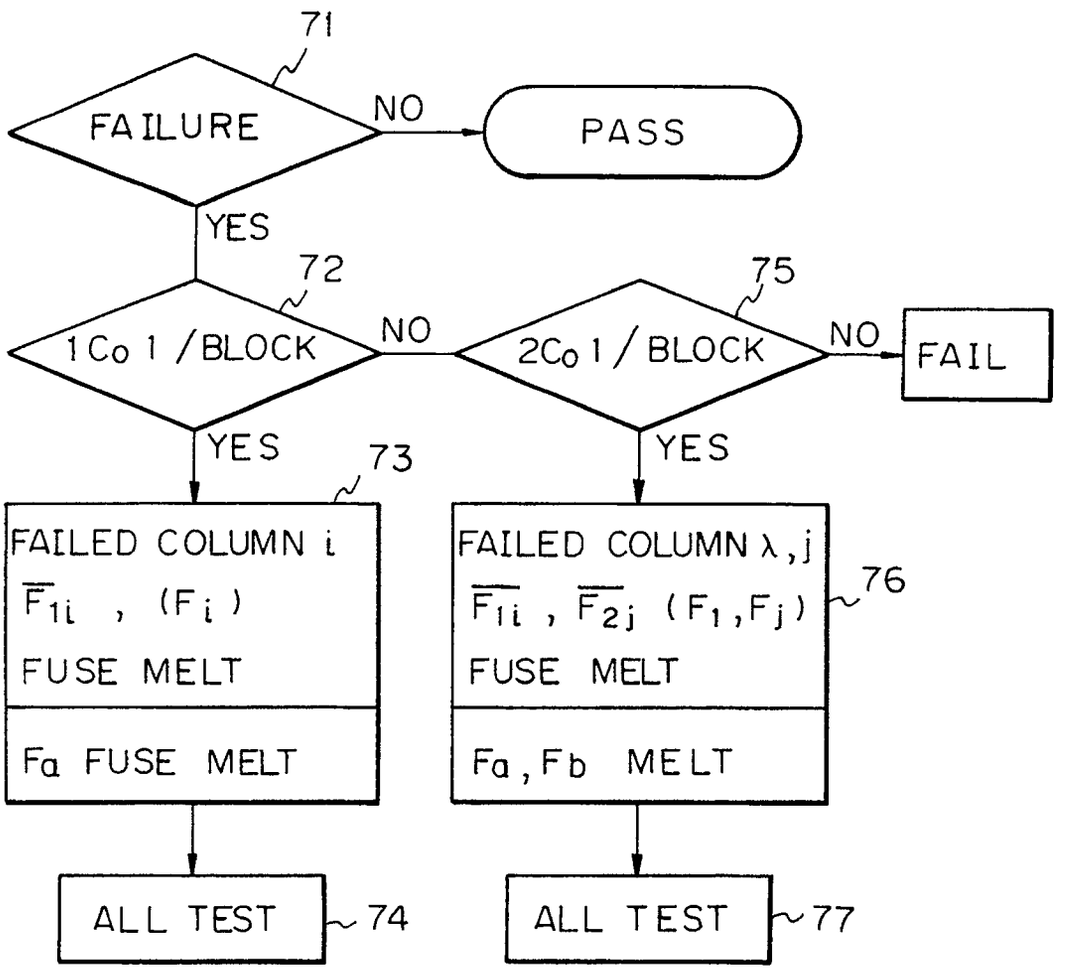
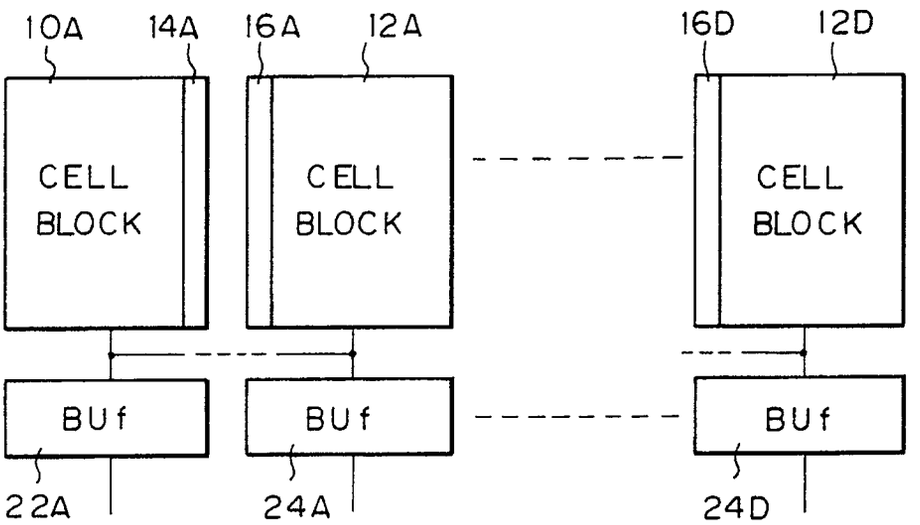

71
FAILURE
NO
PASS
YES
72
1Co 1 /BLOCK
NO
75
2Co 1 / BLOCK
NO
FAIL
YES
YES
73
FAILED COLUMN i
$\overline{F_{1i}}$, (F_i)
FUSE MELT
Fa FUSE MELT
FAILED COLUMN λ,j
$\overline{F_{1i}}$, $\overline{F_{2j}}$ (F_1,F_j)
FUSE MELT
Fa, Fb MELT
76
ALL TEST
74
ALL TEST
77

Fig. 7


10A
14A
16A
12A
16D
12D
CELL BLOCK
CELL BLOCK
CELL BLOCK
BUf
BUf
BUf
22A
24A
24D