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(54) **VECTOR ATTRIBUTE GENERATING METHOD AND APPARATUS.**

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Description

The present invention relates, generally, to computer data graphics systems and, more particularly, to a method and apparatus for generating patterned vector attribute data in conjunction with the creation of a vector in the refresh memory for the graphic system visual display device.

Background of the Invention

In the typical graphics display system, a cathode ray tube monitor, or similar visual display device, provides the user with a visual image that is generated from data stored in a refresh memory. Typically, the refresh memory contains data which defines the attributes of each pixel of the cathode ray display. Thus, there is a one-to-one correspondence between the data in the refresh memory and the visual information displayed by the cathode ray tube display. In a computer graphics display system, the user generates a visual image on the cathode ray tube by writing attribute data into the refresh memory. At the beginning of a new picture, the refresh memory is typically erased and loaded entirely with a background intensity level. When a new picture is created, a foreground intensity replaces the background intensity, along the image being created.

In the past, the structure for implementing such an operation involved the use of a first register loaded with the background level, and a second register loaded with the foreground level. These registers would then supply these levels to a two-to-one multiplexer. The output of the two-to-one multiplexer would be supplied to the refresh memory data input line. In the two-to-one multiplexer, the outputs thereof would be selected between the foreground and the background by an appropriate control signal. A vector generator generated the addressing to the refresh memory for the point in the refresh memory at which the image was being created. In a modification of this structure disclosed in WO—A—82/01614, the refresh memory was split up into an attribute memory, and an information memory. Such an arrangement required that there be participation by a controller, such as the control processing unit or system microprocessor in the designation of the vector attributes on a pixel by pixel basis and, as such, represents an inefficient use of processing time.

Summary of the Invention

These problems of prior art vector attribute generating systems are overcome by the present invention, as claimed in claims 1 and 12, for use in a graphics display system, wherein a refresh memory supplies image data to a visual display device for display, and wherein the contents of the refresh memory are written therein according to addresses supplied by a vector address generator and to attributes supplied by the present invention in accordance with an attribute format instruction. The present invention includes a memory means for storing data corresponding to a plurality of different attributes at selected addresses. The plurality of attributes can include different levels of intensity, color and the like. Also included are means for addressing the attribute storage means in response to the attribute format instruction and in conjunction with the addresses supplied from the vector address generator. With such a structure, the addressing means execute the attribute format instructions to generate a set of addresses which cause the memory means to provide the appropriate attribute data to the refresh memory in concert with the addressing to the refresh supplied thereto by the vector address generator means. This greatly reduces the amount of time that the microprocessor must spend in the generation of the screen image.

In a preferred embodiment of the present invention, the addressing means includes scaler counter means, address counter means and length counter means. The attribute format instructions include a scaler parameter, a length parameter, and a starting address. The scaler counter means receives a control signal from the vector generator which is generated in conjunction with the addressing of the refresh memory. An increment count pulse is output after the number of pulses specified by the scaler parameter have been received from the vector address generator control signal. In response to the count pulse from the scaler counter means, the address counter increments the starting address by one count. The length counter means is also responsive to the count pulse, counting the number of count pulses provided by the scaler counter means and, thereafter, outputting a load pulse to the address counter means after a number of counts, specified by the length parameter, have been received from the scaler counter means. When the address counter means receives the load signal from the length counter means, it reloads the original starting address and begins incrementing that starting address anew.

It is therefore an object of the present invention to provide a method and apparatus for generating vector information for storage in a refresh memory.

It is another object of the present invention to provide a method and apparatus for generating vector attributes for storage in a refresh memory which minimizes participation by the central processing unit therein.

It is a further object of the present invention to provide a method and apparatus for generating vector attributes for storage in a refresh memory wherein a microprocessor provides attribute instructions to an address generating means, and a vector address generator supplies control signals to the address generating means, and further wherein the address generating means, in response to the attribute data, address a attribute storage means to cause the attribute storage means to provide selected attribute data to the

refresh memory in concert with the addressing supplied by the vector means to the refresh memory.

These objectives, features and advantages of the present invention will be more readily understood upon consideration of the following detailed description and accompanying drawings.

Brief Description of the Drawings

Fig. 1 is a functional block diagram of the present invention.

Fig. 2 illustrates the generation of attributes in accordance with the present invention for a dashed-line image.

Fig. 3 illustrates the generation of vector attributes in accordance with the present invention for a vector in which the intensity increases every two pixels for a predetermined number of pixels, and is then reset to begin anew.

Detailed Description of the Invention

Referring to Fig. 1, it can be seen that a display device 10, such as a cathode ray tube, receives display data from a refresh memory 12. Display device 10 supplies appropriate addressing signals on display control line 14 to cause the contents of refresh memory 12 to be read out over display data line 16 on a periodic basis.

During the vertical retrace cycle, or a similar cycle which has been designated for display modification, the contents of refresh memory 12 are modified. This modification is typically conducted on a pixel-by-pixel basis. The location of each pixel to be modified is provided by addresses on line 18. These addresses are provided by vector address generator 20. Vector address generator 20 also provides a write enable signal to the refresh memory 12.

The actual data which describes the attribute for the particular pixel being modified is supplied to refresh memory 12 on line 22. The attribute data, in turn, is supplied on line 22 from attribute random access memory (RAM) 24.

Attribute RAM 24 is addressed by addressing circuitry 26. The contents of attribute RAM 24 are supplied by central processing unit 28 via data line 30 and control line 32. Central processing unit (CPU) 28 also supplies attribute format instructions to addressing circuitry 26 on data line 30, along with control signals on lines 34.

As can be seen from Fig. 1, CPU 28 also communicates with vector address generator 20. Finally, vector address generator 20 supplies control signals to addressing circuitry 26 via line 37.

With respect to vector address generator 20, the function of this device is to provide addressing on a pixel-by-pixel basis of the location of the image in the refresh memory, in response to signals received from the central processing unit 28, or some interface unit (not shown). In turn, the signals from the interface unit or the central processing unit 28, are derived from input signals from the user. These signals take the form of location, direction and length information. Vector address generator 20 converts these signals into specific pixel addresses. When these pixel addresses are supplied to refresh memory 12, along with attribute information on line 22, an image is created within refresh memory 12. Vector address generation is well known in the graphics display area. Methods and structures for implementing such a function are described in numerous texts.

Addressing circuitry 26 includes a presettable address counter 36, which is supplied with a starting address by address register 38. The presettable address counter 36 increments the starting address according to a clock supplied on line 40 from presettable scaler counter 42. Scaler counter 42, in turn, is supplied with the control signal on line 37 from vector address generator 20. Scaler counter 42 counts the number of pulses present on line 37 and outputs a clock pulse on line 40 after a predetermined number of pulses have appeared on line 37. This predetermined number is specified by the contents of scaler register 44.

Also responsive to the clock signal on line 40 from scaler counter 42 is presettable length counter 46. Presettable length counter 46 receives length data from length register 48 and issues a load pulse to address counter 36 after a predetermined number of clock pulses, as specified by the length data, have been detected on line 40.

As can be seen from Fig. 1, length register 48, starting address register 38, and scaler register 44 receive data and control signals from central processing unit 28 on lines 30 and 34, respectively. This data can be viewed as an instruction from central processing unit 28, which instruction is executed by addressing circuitry 26 without the need for further participation by central processing unit 28 during the execution of the instruction.

Attribute RAM 24 can be viewed as a look-up table, the contents of which can be modified by central processing unit 28 via lines 30 and 32. Attribute RAM 24 preferably contains selected addresses for all of the vector attribute information required for the images sought to be generated. This attribute information would include data such as background intensity, color, and the like, data on the various degrees of intensity which are to be used in the display, data on the various colors which are to be used in the display, and other similar information. As mentioned above, this information is stored at selected addresses so that the instructions supplied by the central processing unit 28 to the addressing circuitry 26, will cause the addressing circuitry 26 to address the attribute RAM 24 to select the appropriate attributes required for the vector being written into refresh memory 12 and for the image being generated.

For a given attribute format instruction from central processing unit 28, the resulting attribute data supplied to refresh memory 12 from attribute RAM 24 can be viewed as an attribute format which is being written into refresh memory 12 at the locations specified by the addressing from vector address generator 20.

The structure of the present invention as illus-

trated in Fig. 1 provides a high degree of flexibility in the generation of different attribute formats. The scaling data supplied to the scaler counter 42 determines for how many pixels the attribute currently being addressed in the attribute RAM 24 will continue to be supplied to refresh memory 12. Thus, if the scaling data represents a large number, the attribute being currently addressed will be supplied for a large number of pixels. Conversely, if the scaling data represents a small number, then the attribute data will change frequently.

The starting addresses supplied to address counter 36 from starting address register 38 specify at what point in the range of possible attributes the attribute actually being generated will be located. Similarly, where an attribute is being varied between a background level and some other level, the starting address will then be typically specified so that the background level is stored in the attribute RAM 24 at a location adjacent to the location of the other attribute level.

The length data determines the number of address counter iterations which will be permitted to occur before the address counter is reset to the starting address. Thus, length counter 46 provides a cyclical control or a segment control of the attribute format being generated.

As can be seen from Fig. 1, individual load lines are supplied to length register 48, starting address register 38 and scaler register 44. This permits the central processing unit 24 to modify the contents of a particular register without affecting the contents of the other registers. Thus, the central processing unit 28 can change the starting address in starting address 38 while the address circuitry 26 is processing data from the previous instruction. Thus, when length counter causes address counter 36 to be loaded with the starting address from starting address register 38, a new starting address can be supplied to address counter 36. The nature of the attribute, therefore, can be changed by modifying the starting address for the attribute format being generated.

The generation of these attribute formats will be more readily understood upon consideration of the examples provided in Figs. 2 and 3.

Fig. 2 illustrates the generation of a dashed-line attribute format in which the image varies between five pixels of background level and five pixels of intensity M, for example. The background level intensity attribute is located at address N in attribute RAM 24, while the intensity level M is located at address N+1 in attribute RAM 24, for example. For such a format, the central processing unit 28 supplies a starting address of N, a scaler count of 5, and a length count of 2.

The first line of Fig. 2 illustrates the signal on vector generator control signal line 37, while the second line of the figure illustrates the addresses being supplied to refresh memory 12. Line 3 illustrates the output of scaler counter 42, while line 4 illustrates the output of address counter 36. Line 5 illustrates the output of length counter 46. Finally, line 6 illustrates the attribute which is output from attribute RAM 24.

As can be seen from Fig. 2, for the first five pulses on vector generator control signal line 37, the address being supplied to parameter RAM 24 is N. This results in a attribute RAM 24 output of intensity level M. This intensity level is then stored at refresh memory locations A through A+4. At the fifth pulse on vector generator control line 37, scaler counter 42 provides a clock pulse. In response thereto, the address from address counter 36 is incremented by one. In turn, parameter RAM 24 provides the background intensity attribute.

After the second set of five pulses has occurred, scaler counter 42 provides a second clock pulse. In response thereto, length counter 46 provides an output pulse which causes address counter 36 to reload the starting address from starting address register 38. Thus, the output of address counter 36 at this point is N. This pattern continues so long as pulses are provided on vector control line 37, or until central processing unit 28 provides the next instruction to the addressing circuitry 26.

Referring to Fig. 3, an attribute format wherein the intensity level is permitted to increase every two pixels for a total of 128 pixels is illustrated. As with Fig. 2, the first line of Fig. 3 depicts the signals on vector generator control line 37. The second line illustrates the scaler counter 42 output. The third and fourth lines illustrate the length counter output and the address counter output, respectively. Finally, the fifth line illustrates the graphical equivalent of the attribute information being supplied from attribute RAM 24. In order to generate the above-described format, the scaler counter 42 is loaded with the number 2, the length counter is loaded with length 64, and the starting address counter is loaded with address M. As can be seen from Fig. 3, scaler counter 42 provides a pulse for every two pulses on the vector generator control line 37. With each pulse from scaler counter 42, address counter increments its output by 1, starting with starting address M. After the scaler counter 42 has output 64 pulses, corresponding to 128 pixels being addressed by vector generator 20, length counter 46 outputs a load pulse to address counter 36, thereby causing the original starting address M to be loaded into address counter 36. As can be seen from the fifth line of Fig. 3, a stair step-like attribute is created by this format.

The functional blocks shown in Fig. 1 can be implemented by commercially available devices. For example, parameter RAM 24 can be a 256 × 4 RAM comprising four 256 × 1 random access memories which are addressed in parallel. Commercially available parts such as industry number 10422, manufactured by Motorola, Inc. of Phoenix, Arizona are suitable for use in such an application. Similarly, the counter functional blocks 46, 36 and 42 can be industry part number 10136, manufactured by Motorola, Inc. of

Phoenix, Arizona. Finally, registers 48, 38 and 44 can be commercial part number 74LS374, manufactured by Signetics Corporation of Sunnyvale, CA.

In accordance with the method of the present invention, a storage means which stores a plurality of different attribute data at selected locations provides attribute data to a refresh memory associated with a visual display device, in conjunction with addresses supplied thereto by a vector address generator. Addressing for the storage means is supplied from an address generator. In order to generate vector attributes for storage in a refresh memory, the method of the present invention comprises the steps of storing a plurality of different attributes at selected addresses in the storage means, providing an attribute format instruction to the addressing means, addressing the storage means in accordance with the attribute format instruction, wherein the addressing step includes the steps of starting the addressing at a specified starting address, incrementing the address whenever a predetermined number of pixel addresses has been supplied to the refresh memory by the vector address generator, wherein the predetermined number is supplied in the attribute format instruction, and restarting the addressing from the starting address when a predetermined number of increment counts has been supplied wherein the predetermined number is provided in the attribute format instruction.

The terms and expressions which have been employed here are used as terms of description and not of limitations, and there is no intention, the use of such terms and expressions of excluding equivalents of the features shown and described, or portions thereof, it being recognized that various modifications are possible within the scope of the invention claimed.

Claims

1. An apparatus for writing patterned vectors having a specified attribute format into a refresh memory (12) in a graphics display system which includes a visual display (10), a vector address generator (20), and means (28) for supplying attribute format instructions, wherein the visual display (10) provides a visual image comprising a matrix of pixels, wherein the attributes of each pixel corresponding to each location in the visual image are specified by attribute data stored at a corresponding location in the refresh memory (12), and further wherein the vector address generator (20) accesses the refresh memory (12) at the locations into which the patterned vector is to be written, the apparatus including

means (24) coupled to the refresh memory for storing a plurality of different attribute data and for providing attribute data to the refresh memory (12);

means (26) coupled to the vector address generator (20) and to the storing means (24) and responsive to the attribute format instructions for addressing the storing means (24) in conjunction with the accessing of the refresh memory (12) by the vector address generator (20), wherein the addressing means (26) supply addresses to the storing means (24) which are selected in accordance with the attribute format instructions, so that selected attribute data are provided by the storing means (24) to the refresh memory (12) and are written into the locations being accessed by the vector address generator (20).

2. The apparatus of claim 1 wherein the storing means (24) is a random access memory.

3. The apparatus of claim 1 wherein the attribute format instructions include a starting address, a length parameter, and a scaling factor, and further wherein the addressing means (26) comprise

address modifying means (36) responsive to the starting address (38) for modifying the starting address in a predetermined manner in conjunction with an increment clock signal and for supplying the modified starting address to the storing means (24); and

clock means (42) coupled to the vector address generator (20) and responsive to the scaling factor (44) for generating the increment clock signal, wherein the clock means (42) generate the increment clock signal whenever the vector address generator (20) has accessed the refresh memory (12) a specified number of times, said specified number being defined by the scaling factor (44), so that the attribute data being supplied to the refresh memory (12) by the storing means (24) changes after said specified number of times.

4. The apparatus of claim 3 further including means (46) coupled to the address modifying means (36) and responsive to the length parameter (48) and to the increment clock signal (42) for initializing the address modifying means (36) to the starting address (38), whenever a predetermined number of increment clock signals have occurred, wherein said predetermined number is specified by the length parameter.

5. The apparatus of claim 3 wherein the address modifying means (36) generate a sequence of addresses which are incremented from the starting address (38) with each increment clock signal received from the clock means (42).

6. The apparatus of claim 4 wherein the increment clock signal is a pulse and further wherein the address modifying means (36) comprise a first presettable counter which is preset with the starting address (38) and which counts from the starting address (38) upon receipt of the increment clock signal.

7. The apparatus of claim 6 wherein the address modifying means (36) further include starting address register means (38) responsive to the starting address for supplying the starting address to the first presettable counter (36).

8. The apparatus of claim 4 wherein the clock means comprise a second presettable counter (42) which is preset with the scaling factor (44) and which decrements its count whenever the

vector address generator (20) accesses the refresh memory (12), wherein the second presettable counter (42) outputs the increment clock signal whenever its count reaches zero.

9. The apparatus of claim 8 further including scaling register means (44) responsive to the scaling factor for supplying the scaling factor to the second presettable counter (42).

10. The apparatus of claim 4 wherein the increment clock signal is a pulse and further wherein the initializing means comprise a third presettable counter (46) which is preset to the length parameter and which decrements its count with each increment clock signal received, wherein the third presettable counter (46) initializes the address modifying means (36) when its count reaches zero.

11. The apparatus of claim 10 further including length register means (48) responsive to the length parameter for supplying the length parameter to the third presettable counter (46).

12. A method for writing patterned vectors having a specified attribute format into a refresh memory (12) in a graphics display system which includes a visual display (10), a vector address generator (20), and means (28) for supplying attribute format instructions, wherein the visual display (10) provides a visual image comprising a matrix of pixels, wherein the attributes of each pixel corresponding to each location in the visual image are specified by attribute data stored at a corresponding location in the refresh memory (12), and further wherein the vector address generator (20) accesses the refresh memory (12) at locations into which the patterned vector is to be written, the method including the steps of

a. storing a plurality of different attribute data at selected addresses in a storing means (24);

b. addressing the storing means (24) according to the attribute format instructions and in conjunction with the accessing of the refresh memory (12) by the vector address generator (20) so that selected attribute data are output from the storing means (24); and

c. providing the selected attribute data to the refresh memory (12) in conjunction with the accessing of the refresh memory (12) by the vector address generator (20).

13. The method as recited in claim 12 wherein the attribute format instructions include a starting address (38), a scaling parameter (44), and a length parameter (48), and further wherein step "b" includes the steps of

i) counting (42) the number of times the vector address generator (2) accesses the refresh memory (12);

ii) outputting an increment clock signal whenever the count in step "i)" corresponds to the scaling parameter;

iii) incrementing the starting address by one location for every occurrence of the increment clock signal in step "ii)";

iv) counting (46) the number of increment clock signals output in step "ii)";

v) repeating steps "i)" through "iv)" until the count in step "iv)" corresponds to the length parameter (48); and

vi) initializing step "iii)" to begin from the starting address (38).

Patentansprüche

1. Vorrichtung zum Einschreiben von Mustervektoren mit einem vorgegebenen Attributformat in einen Auffrischspeicher (12) eines graphischen Bildschirmsystems mit einem Bildschirmgerät (10), einem Vektor-Adressengenerator (20) und einer Einrichtung (28) zur Lieferung von Attributformatbefehlen, wobei das Bildschirmgerät (10) ein Bild aus einer Matrix von Bildpunkten liefert und die Attribute jedes einer Stelle im Bild entsprechenden Bildpunktes durch Attributdaten angegeben werden, die an einer entsprechenden Stelle im Auffrischspeicher (12) gespeichert sind, und wobei der Vektor-Adressengenerator (20) auf den Auffrischspeicher (12) an denjenigen Stellen zugreift, in die die Mustervektoren einzuschreiben sind,

mit einer mit dem Auffrischspeicher verbundenen Einrichtung (24) zur Speicherung einer Vielzahl unterschiedlicher Attributdaten und zur Lieferung von Attributdaten an den Auffrischspeicher (12),

einer mit dem Vektor-Adressengenerator (20) und der Speichereinrichtung (24) verbundenen Einrichtung (26), die unter Ansprechen auf die Attributformatbefehle die Speichereinrichtung (24) in Verbindung mit dem Zugreifen des Auffrischspeichers (12) durch den Vektoradressengenerator (20) adressiert, wobei die Adressiereinrichtung (26) Adressen an die Speichereinrichtung (24) liefert, die entsprechend den Attributformatbefehlen gewählt sind, so daß gewählte Attributdaten durch die Speichereinrichtung (24) an den Auffrischspeicher (12) geliefert und in Speicherstellen geschrieben werden, die durch den Vektor-Adressengenerator (20) zugegriffen werden.

2. Vorrichtung nach Anspruch 1, bei der die Speichereinrichtung (24) ein Speicher mit wahlfreiem Zugriff ist.

3. Vorrichtung nach Anspruch 1, bei der die Attributformatbefehle eine Startadresse, einen Längenparameter und einen Skalierfaktor umfassen, wobei die Adressiereinrichtung (26) aufweist:

eine Adressenänderungseinrichtung (36), die unter Ansprechen auf die Startadresse (38) diese in vorbestimmter Weise in Verbindung mit einem Weiterschalt-Taktsignal abändert und an die Speichereinrichtung (24) liefert, und

eine Takteinrichtung (42), die mit dem Vektor-Adressengenerator (20) verbunden ist und unter Ansprechen auf den Skalierfaktor (44) das Weiterschalt-Taktsignal immer dann erzeugt, wenn der Vektor-Adressengenerator (20) eine vorgegebene Anzahl von Zugriffsvorgängen auf den Auffrischspeicher (12) durchgeführt hat, wobei die vorgegebene Anzahl durch den Skalierfaktor (44) definiert ist, so daß die durch die Speichereinrichtung

(24) an den Auffrischspeicher (12) gelieferten Attributdaten sich nach der angegebenen Anzahl von Zugriffsvorgängen ändern.

4. Vorrichtung nach Anspruch 3, mit ferner einer Einrichtung (46), die mit der Adressenabänderungseinrichtung (36) verbunden ist und unter Ansprechen auf den Längenparameter (48) und das Weiterschalt-Taktsignal (42) die Adressenabänderungseinrichtung (36) auf die Startadresse (38) immer dann einstellt, wenn eine vorbestimmte Anzahl von Weiterschalt-Taktsignalen aufgetreten ist, wobei die vorbestimmte Anzahl durch den Längenparameter angegeben wird.

5. Vorrichtung nach Anspruch 3, bei der die Adressenabänderungseinrichtung (36) eine Folge von Adressen erzeugt, die ausgehend von der Startadresse (38) mit jedem von der Takteinrichtung (42) empfangenen Weiterschalt-Taktsignal weitergeschaltet wird.

6. Vorrichtung nach Anspruch 4, bei der das Weiterschalt-Taktsignal eine Impulsfolge ist und die Adressenabänderungseinrichtung (36) einen ersten voreinstellbaren Zähler umfaßt, der mit der Startadresse (38) voreingestellt wird und bei Empfang des Weiterschalt-Taktsignals von der Startadresse (38) ausgehend weiterzählt.

7. Vorrichtung nach Anspruch 6, bei der die Adressenabänderungseinrichtung (36) ferner ein Startadressenregister (38) umfaßt, das unter Ansprechen auf die Startadresse diese an den ersten voreinstellbaren Zähler (36) liefert.

8. Vorrichtung nach Anspruch 4, bei der die Takteinrichtung einen zweiten voreinstellbaren Zähler (42) umfaßt, der mit dem Skalierfaktor (44) voreingestellt wird und seinen Zählwert immer dann zurückzählt, wenn der Vektoradressengenerator (20) auf den Auffrischspeicher (12) zugreift, wobei der zweite voreinstellbare Zähler (42) das Weiterschalt-Taktsignal immer dann ausgibt, wenn sein Zählwert Null erreicht.

9. Vorrichtung nach Anspruch 8 mit ferner einem Skalierregister (44), das unter Ansprechen auf den Skalierfaktor diesen an den zweiten voreinstellbaren Zähler (42) liefert.

10. Vorrichtung nach Anspruch 4, bei der das Weiterschalt-Taktsignal eine Impulsfolge ist und die Einstelleinrichtung einen dritten voreinstellbaren Zähler (46) umfaßt, der auf den Längenparameter voreingestellt wird und seinen Zählwert mit jedem empfangenen Weiterschalt-Taktsignal zurückzählt, wodurch der dritte einstellbare Zähler (46) die Adressenabänderungseinrichtung (36) einstellt, wenn sein Zählwert Null erreicht.

11. Vorrichtung nach Anspruch 10 mit ferner einem Längenregister (48), das unter Ansprechen auf den Längenparameter diesen an den dritten voreinstellbaren Zähler (46) liefert.

12. Verfahren zum Einschreiben von Mustervektoren mit einem vorgegebenen Attributformat in einen Auffrischspeicher (12) eines graphischen Bildschirmsystems mit einem Bildschirmgerät (10), einem Vektor-Adressengenerator (20) und einer Einrichtung (28) zur Lieferung von Attributformatbefehlen, wobei das Bildschirmgerät (10) ein Bild aus einer Matrix von Bildpunkten liefert und die Attribute jedes Bildpunktes entsprechend einer Stelle im Bild durch Attributdaten angegeben werden, die an einer entsprechenden Stelle im Auffrischspeicher (12) gespeichert sind, und wobei der Vektor-Adressengenerator (20) auf den Auffrischspeicher (12) an Stellen zugreift, in die der Mustervektor einzuschreiben ist, mit den Verfahrensschritten:

a. Speichern einer Vielzahl unterschiedlicher Attributdaten an gewählten Adressen in einer Speichereinrichtung (24),

b. Adressieren der Speichereinrichtung (24) entsprechend den Attributformatbefehlen und in Verbindung mit dem Zugreifen durch den Vektor-Adressengenerator (20) auf den Auffrischspeicher (12), so daß gewählte Attributdaten von der Speichereinrichtung (24) ausgegeben werden, und

c. Liefern der gewählten Attributdaten an den Auffrischspeicher (12) in Verbindung mit dem Zugreifen durch den Vektor-Adressengenerator (20) auf den Auffrischspeicher (12).

13. Verfahren nach Anspruch 12, bei dem die Attributformatbefehle eine Startadresse (38), einen Skalierparameter (44) und einen Längenparameter (48) umfassen und wobei der Schritt "b" die folgenden Schritte umfaßt:

i) Zählen (42), wie oft der Vektor-Adressengenerator (20) auf den Auffrischspeicher (12) zugreift,

ii) Ausgeben eines Weiterschalt-Taktsignals immer dann, wenn der Zählwert des Schrittes i) dem Skalierparameter entspricht,

iii) Weiterschalten der Startadresse um eine Speicherstelle bei jedem Auftreten des Weiterschalt-Taktsignals gemäß Schritt ii),

iv) Zählen (46) der Anzahl von Weiterschalt-Taktsignalen, die beim Schritt ii) ausgegeben werden,

v) Wiederholen der Schritte i) bis iv), bis der Zählwert beim Schritt iv) dem Längenparameter (48) entspricht, und

vi) Einleiten des Schrittes iii) derart, daß er mit der Startadresse (48) beginnt.

Revendications

1. Appareil pour écrire des vecteurs configurés ayant un format d'attribut spécifié dans une mémoire (12) de régénération dans un système d'affichage graphique qui comprend un dispositif (10) d'affichage visuel, un générateur (20) d'adresses de vecteurs et des moyens (28) destinés à fournir des instructions de format d'attribut, dans lequel le dispositif d'affichage visuel (10) produit une image visuelle comprenant une matrice de pixels, dans laquelle les attributs de chaque pixel correspondant à chaque position dans l'image visuelle sont spécifiés par des données d'attributs stockées dans une position correspondante dans la mémoire (12) de régénération, et dans lequel en outre le générateur (20) d'adresses de vecteurs accède à la mémoire (12) de régénération aux emplacements dans lesquels le vecteur configuré doit être écrit, l'appareil comprenant

des moyens (24) couplés à la mémoire de

régénération pour stocker plusieurs données d'attributs différentes et pour fournir des données d'attributs à la mémoire (12) de régénération;

des moyens (26) couplés au générateur (20) d'adresses de vecteurs et aux moyens (24) de stockage et qui, en réponse aux instructions de format d'attribut, sont destinés à l'adressage des moyens (24) de stockage en même temps que le générateur (20) d'adresses de vecteurs accède à la mémoire (12) de régénération, les moyens (26) d'adressage fournissant des adresses aux moyens (24) de stockage qui sont choisies en fonction des instructions de format d'attribut, de manière que des données choisies d'attribut soient fournies par les moyens (24) de stockage à la mémoire (12) de régénération et soient écrites dans les positions accédées par le générateur (20) d'adresses de vecteurs.

2. Appareil selon la revendication 1, dans lequel les moyens (24) de stockage comprennent une mémoire vive.

3. Appareil selon la revendication 1, dans lequel les instructions de format d'attribut comprennent une adresse de départ, un paramètre de longueur et un facteur d'échelle, et en outre dans lequel les moyens (26) d'adressage comprennent

un moyen (36) de modification d'adresse qui, en réponse à l'adresse (38) de départ, modifie l'adresse de départ d'une manière prédéterminée conjointement avec un signal d'horloge d'incrémentation et fournit l'adresse de départ modifiée aux moyens (24) de stockage; et

un moyen d'horloge (42) couplé au générateur d'adresses de vecteurs et qui, en réponse au facteur d'échelle (44), génère le signal d'horloge d'incrémentation, le moyen d'horloge (42) générant le signal d'horloge d'incrémentation lorsque le générateur (20) d'adresses de vecteurs a accédé un nombre spécifié de fois à la mémoire (12) de régénération, le nombre spécifié étant défini par le facteur d'échelle (44) afin que les données d'attributs fournies à la mémoire (12) de régénération par les moyens (24) de stockage changent après ledit nombre spécifié de fois.

4. Appareil selon la revendication 3, comprenant en outre des moyens (46) couplés au moyen (36) de modification d'adresse et qui, en réponse au paramètre (48) de longueur et au signal d'horloge d'incrémentation (42), initialisent le moyen (36) de modification d'adresse à l'adresse de départ (38), lorsqu'un nombre prédéterminé de signaux d'horloge d'incrémentation est apparu, ledit nombre prédéterminé étant spécifié par le paramètre de longueur.

5. Appareil selon la revendication 3, dans lequel le moyen (36) de modification d'adresse génère une séquence d'adresses qui sont incrémentées depuis l'adresse (38) de départ à chaque signal d'horloge d'incrémentation reçu du moyen d'horloge (42).

6. Appareil selon la revendication 4, dans lequel le signal d'horloge d'incrémentation est une impulsion et dans lequel en outre le moyen (36) de modification d'adresse comprend un premier compteur à présélection qui est présélectionné avec l'adresse (38) de départ et qui compte à partir de l'adresse (38) de départ à la suite de la réception du signal d'horloge d'incrémentation.

7. Appareil selon la revendication 6, dans lequel le moyen (36) de modification d'adresse comprend en outre un moyen (38) à registre d'adresse de départ qui, en réponse à l'adresse de départ, fournit l'adresse de départ au premier compteur (36) à présélection.

8. Appareil selon la revendication 4, dans lequel le moyen d'horloge comprend un deuxième compteur (42) à présélection qui est présélectionné avec le facteur d'échelle (44) et qui décrémente son compte lorsque le générateur (20) d'adresses de vecteurs accède à la mémoire (12) de régénération, le second compteur (42) à présélection délivrant en sortie le signal d'horloge d'incrémentation lorsque son compte atteint zéro.

9. Appareil selon la revendication 8, comprenant en outre un moyen (44) à registre de changement d'échelle qui, en réponse au facteur d'échelle, fournit le facteur d'échelle au deuxième compteur (42) à présélection.

10. Appareil selon la revendication 4, dans lequel le signal d'horloge d'incrémentation est une impulsion et dans lequel en outre les moyens d'initialisation comprennent un troisième compteur (46) à présélection qui est présélectionné au paramètre de longueur et qui décrémente son compte à chaque signal d'horloge d'incrémentation reçu, le troisième compteur (46) à présélection initialisant le moyen (36) de modification d'adresse lorsque son compte atteint zéro.

11. Appareil selon la revendication 10, comprenant en outre un moyen (48) à registre de longueur qui, en réponse au paramètre de longueur, fournit le paramètre de longueur au troisième compteur (46) à présélection.

12. Procédé pour écrire des vecteurs configurés, ayant un format d'attribut spécifié, dans une mémoire de régénération (12) dans un système d'affichage graphique qui comprend un dispositif d'affichage visuel (10), un générateur (20) d'adresses de vecteurs et des moyens (28) destinés à fournir des instructions de formats d'attributs, le dispositif d'affichage visuel (10) produisant une image visuelle qui comprend une matrice de pixels, dans laquelle les attributs de chaque pixel, correspondant à chaque position dans l'image visuelle, sont spécifiés par des données d'attributs stockées dans une position correspondante dans la mémoire (12) de régénération, et dans lequel en outre le générateur (20) d'adresses de vecteurs accède à la mémoire (12) de régénération en des positions dans lesquelles le vecteur configuré doit être écrit, le procédé comprenant les étapes qui consistent

a. à stocker plusieurs données d'attributs différentes en des adresses choisies dans des moyens de stockage (24);

b. à adresser les moyens de stockage (24) conformément aux instructions de formats d'attributs et conjointement avec l'accès du générateur d'adresses de vecteurs à la mémoire (12) de régénération afin que les données d'attributs

choisies soient délivrées en sortie des moyens (24) de stockage; et

c. à appliquer les données d'attributs choisies à la mémoire (12) de régénération conjointement avec l'accès à la mémoire (12) de régénération par le générateur (20) d'adresses de vecteurs.

13. Procédé selon la revendication 12, dans lequel les instructions de formats d'attributs comprennent une adresse de départ (38), un paramètre d'échelle (44) et un paramètre de longueur (48), et dans lequel en outre l'étape "b" comprend les étapes qui consistent

i) à compter (42) le nombre de fois que le générateur (20) d'adresses de vecteurs accède à la mémoire (12) de régénération;

ii) à délivrer en sortie un signal d'horloge d'incrémentation lorsque le compte dans l'étape "i)" correspond au paramètre d'échelle;

iii) à incrémenter l'adresse de départ d'une position à chaque apparition du signal d'horloge d'incrémentation dans l'étape "ii)";

iv) à compter (46) le nombre de signaux d'horloge d'incrémentation en sortie à l'étape "ii)";

v) à répéter les étapes "i)" à "iv)" jusqu'à ce que le compte dans l'étape "iv)" corresponde au paramètre de longueur (48); et

vi) à initialiser l'étape "iii)" pour commencer à partir de l'adresse de départ (38).

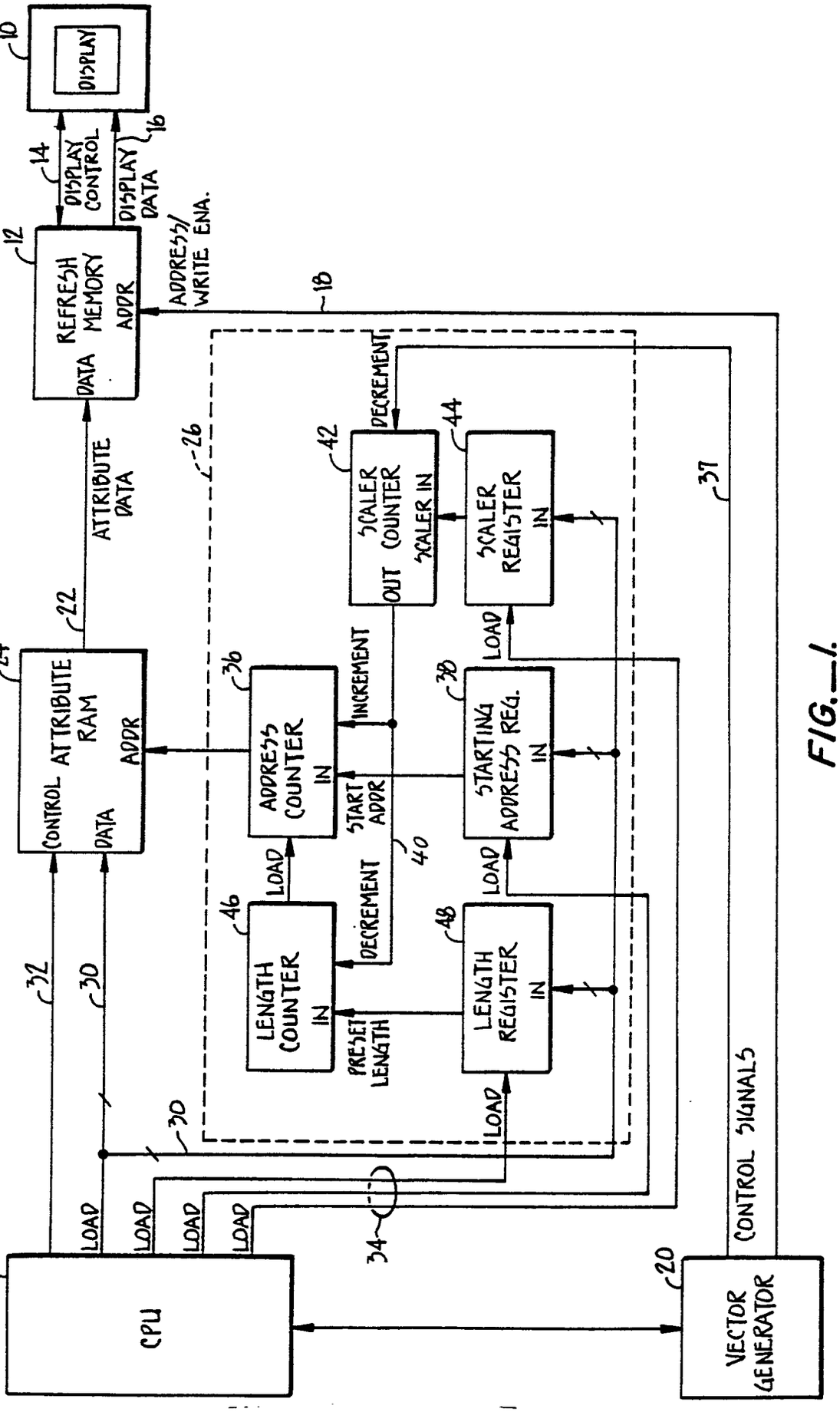

10
DISPLAY
14
DISPLAY CONTROL
16
DISPLAY DATA
12
REFRESH MEMORY
DATA
ADDR
ADDRESS/ WRITE ENA.
18
ATTRIBUTE DATA
22
24
ATTRIBUTE RAM
CONTROL
DATA
ADDR
26
42
SCALER COUNTER
SCALER IN
OUT
DECREMENT
44
SCALER REGISTER
IN
LOAD
37
36
ADDRESS COUNTER
IN
INCREMENT
START ADDR
38
STARTING ADDRESS REG.
IN
LOAD
40
46
LENGTH COUNTER
IN
LOAD
DECREMENT
PRESET LENGTH
48
LENGTH REGISTER
IN
LOAD
32
30
30
LOAD
LOAD
LOAD
LOAD
34
28
CPU
20
VECTOR GENERATOR
CONTROL SIGNALS

FIG. 1.

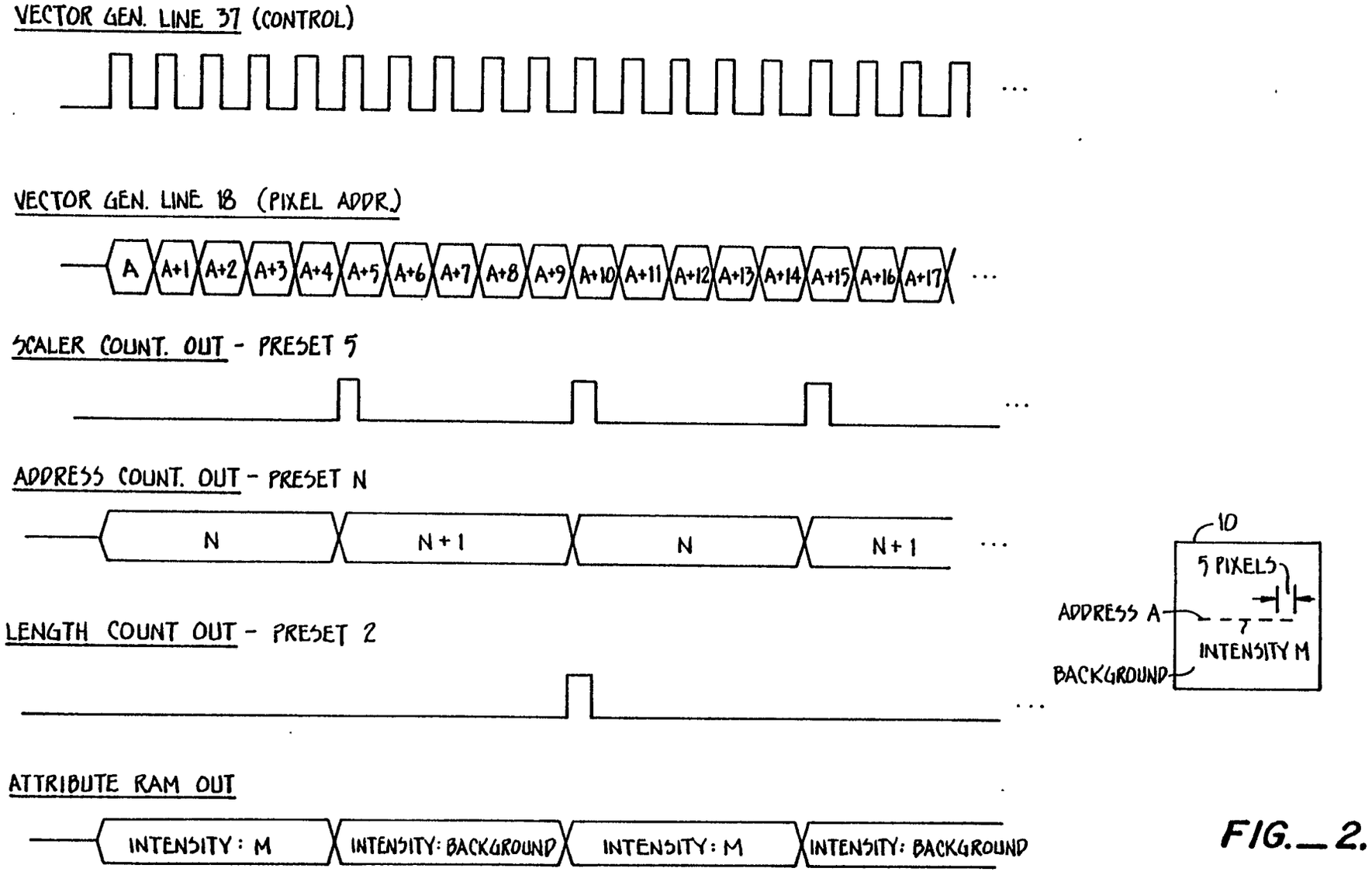

VECTOR GEN. LINE 37 (CONTROL)
VECTOR GEN. LINE 18 (PIXEL ADDR.)
A
A+1
A+2
A+3
A+4
A+5
A+6
A+7
A+8
A+9
A+10
A+11
A+12
A+13
A+14
A+15
A+16
A+17
SCALER COUNT. OUT - PRESET 5
ADDRESS COUNT. OUT - PRESET N
N
N+1
N
N+1
LENGTH COUNT OUT - PRESET 2
ATTRIBUTE RAM OUT
INTENSITY: M
INTENSITY: BACKGROUND
INTENSITY: M
INTENSITY: BACKGROUND
10
5 PIXELS
ADDRESS A
INTENSITY M
BACKGROUND

FIG. 2.

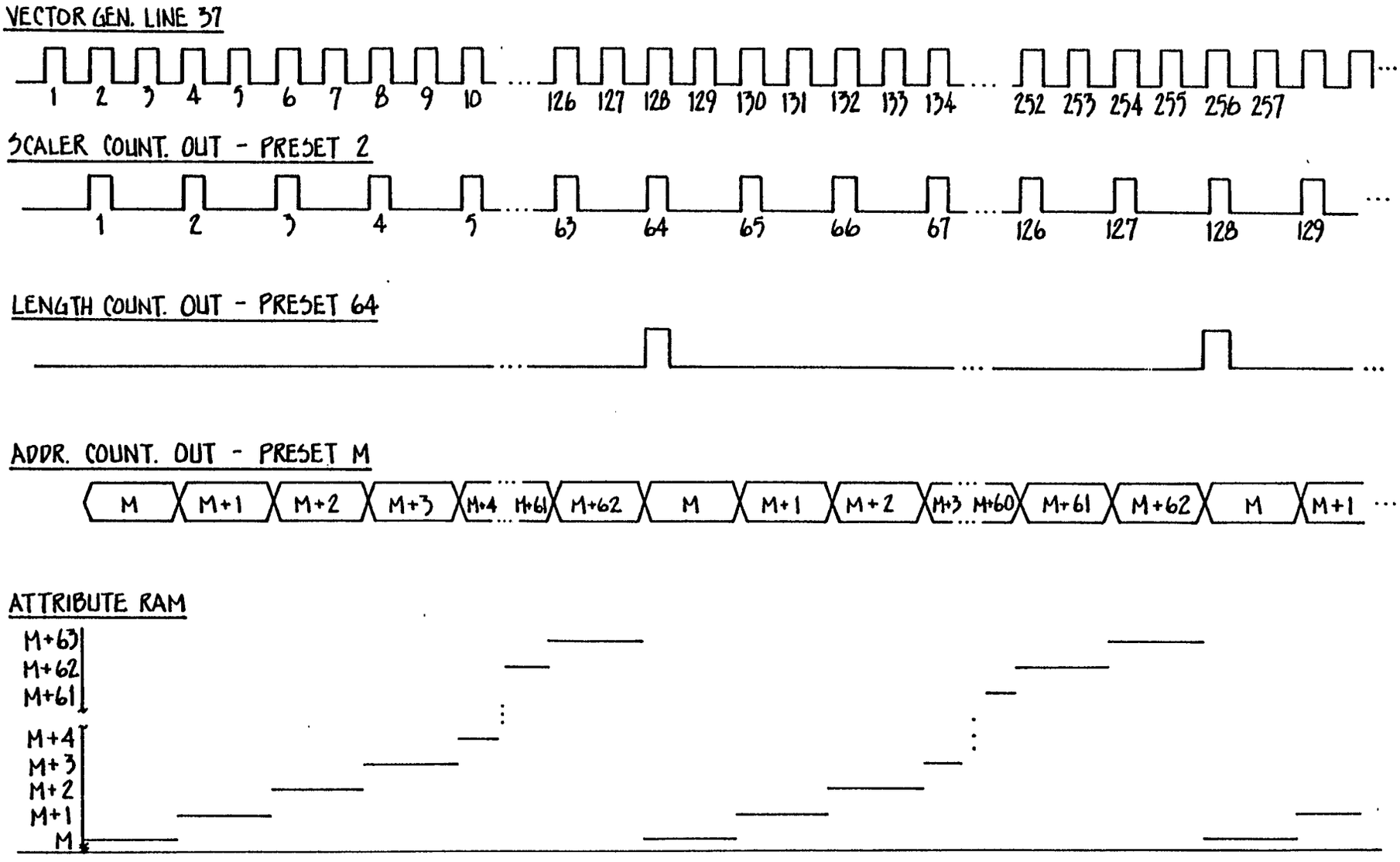


FIG. 3.

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