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(54) **Combination infrared microwave intrusion detector.**

(57) The independent outputs of the microwave system (26) and the passive infrared detector (28) are processed separately in electronic circuits so that there will be no final alarm output signal unless both systems are activated by the radiation of a moving target. A time-AND gate is used to combine the signals and generate an alarm. The upper portion (12) of the housing includes a circular well wall and ribs which radiate from the well wall and the lower portion of the housing includes a circular well wall and a coaxial circular wall. The bottom edge of the printed circuit board (PCB) of the detector butts against the upper edge of the ribs and a portion of the PCB bears against the circular well wall while the upper edge of the PCB butts against the upper edge of the circular wall and a portion of the PCB bears against the well wall formed in the upper housing. The PCB also engages a swivel ring (18) which is rotatable with the housing and which includes notches engageable with a projection extending from the inner surface of the lower housing.

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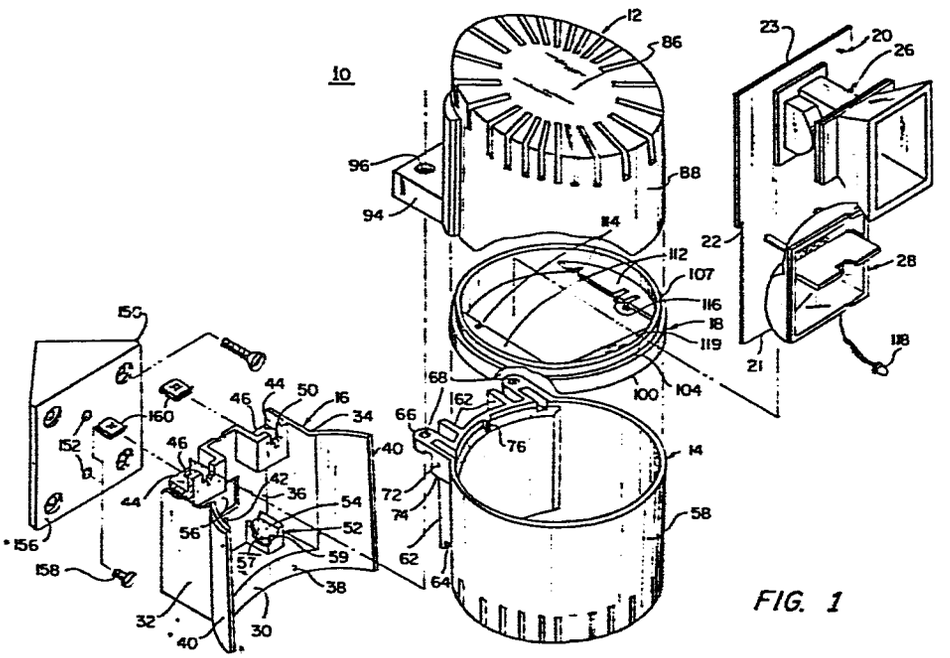
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FIG. 1

COMBINATION INFRARED MICROWAVE INTRUSION DETECTOR

This invention relates generally to intrusion detectors and more specifically to a detector system utilizing sensors of two different types in combination.

The purpose of combining the two detectors is to provide overlapping detection patterns which will, in combination, suppress false alarms due to various spurious signals produced by environmental elements or by active components in the detector subsystems.

The art is comparatively new and the inventors are not familiar with other devices which utilize two different types of detectors for the purposes above mentioned.

The invention disclosed herein comprises electrical outputs of two independent detection systems which are processed separately in electronic circuits so that there will be no final alarm output signal unless both are simultaneously activated by the radiation of a moving target. A time-AND gate is used to combine these signals and generate an alarm.

A multi-faceted optical system is used in the PIR sensor to focus radiation from discrete fields of view within the protection pattern on to the window of a twin element pyroelectric detector. Both sensing elements are connected in series opposition to provide a differential output of either polarity and immunity from common mode signals such as those generated by variation in ambient temperature, background radiation and acoustic noise.

The pyroelectric detector output is amplified and processed so that no PIR alarm signal will occur unless a moving intruder target passes

into and out of any one field of view. To further reduce the possibility of false alarms, this PIR circuit requires two sequential signals of opposite polarity to exceed a preset threshold within a defined period of time.

The RF sensor uses a solid state X-band microwave diplexer in a zero IF system for detecting Doppler-shift energy reflected from a moving intruder target within the specified protection pattern.

Temperature compensated Gunn effect technology is employed to generate stable fixed-frequency microwave power in the diplexer waveguide which feeds a common high-gain horn antenna and this radiates an electromagnetic field in the form of a beam. The waveguide also contains a Schottky barrier diode in an associated mixer cavity which combines reflected energy from a moving target with a sample of the generated power to produce a difference signal or Doppler shift in frequency.

To further reduce the possibility of false alarms due to extraneous sources, the diplexer detector output is amplified and processed so that no RF alarm signal will occur at the time-AND gate output unless an intruder target moves continuously within the beam for a defined period of time.

The two independent detection systems are positioned in a housing having cup-shaped upper and lower portions which include the inner surfaces of the cap elements. The cap of the lower portion has a circular well wall with a series of spaced radiating ribs extending therefrom. The cap of the upper portion includes a circular well wall having a circular wall in spaced coaxial relation therewith. The printed circuit board on which the electrical elements and the independent detectors are mounted

has its lower edge bearing against the upper surface of the ribs with a horizontal surface adjacent the lower edge bearing against a side of the well wall. The upper edge of the printed circuit board bears against the upper surface of the circular wall and has a horizontal surface adjacent the upper edge bearing against the side of its well wall.

The lower housing also includes a projection which engages a ring rotatable within the lower housing and including notches which are engaged by the projection to determine the position of the printed circuit board in relation to the housing.

The method of engaging the upper and lower housings with each other, with a swivel ring, from which the ring extends and a bracket has many unique features including the use of U nuts attached to a shelf formed in compartment of the bracket, T shaped elements which extend from a lid portion of the upper housing engageable with a part of the lower housing and ribs formed on the lower housing which engage an element formed in the bracket.

Further details are explained below with the help of the examples illustrated in the attached drawings in which:

FIG. 1 is an exploded perspective view from the front of an embodiment of the intrusion detector system according to the present invention;

FIG. 1A is an enlarged rear view of the compartment of the bracket of the intrusion detector system according to the present invention;

FIG. 2 is a top plan view of the housing of the intrusion detector system shown in FIG. 1;

FIG. 3 is a side elevational view of the intrusion detector system shown in FIG. 1;

FIG. 4 is a top plan view of the intrusion

detector system shown in FIG. 1;

FIG. 5 is a rear elevational view of the intrusion detector system shown in FIG. 1;

FIG. 6 is a sectional view of the intrusion detector system taken on line 6-6 of FIG. 5;

FIG. 7 is a sectional view of the intrusion detector system taken on line 7-7 of FIG. 5;

FIG. 8 is a rear elevational view of the combination of the upper housing, lower housing, swivel ring and the bracket of the detector system shown in FIG. 1;

FIG. 9 is a sectional view of the intrusion detector system taken on line 7-7 of FIG. 8;

FIG. 10 is a top plan view of the upper housing of the detector system shown in FIG. 1;

FIG. 11 is a front elevational view of the housing enclosure of the PIR detector of the intrusion detector system shown in FIG. 1;

FIG. 12 is a cross-sectional view of the housing enclosure of the PIR detector of the intrusion detector system shown in FIG. 1;

FIG. 13 is a front elevational view of the signal processing board and a mirror member of the PIR detector of the intrusion detector system shown in FIG. 1;

FIG. 14 is a cross-sectional view of the mirror member shown in FIG. 13;

FIG. 15 is a perspective bottom view of the PCB and mirror member of the PIR detector of the intrusion detector system shown in FIG. 1 taken from the back of the mirror member;

FIG. 16 is a cross-sectional view of the partial assembly of the housing assembly, PCB and mirror member illustrating the reflective characteristics of impinging infrared radiation to

the PIR when assembled;

FIGS. 17 and 18 are diagrams illustrating the detection pattern of the intrusion detector system shown in FIG. 1;

FIG. 19(A-E) are wave form diagrams illustrating various input and output signals of the intrusion detector system shown in FIG. 1;

FIG. 20 is an exploded view of the PCB having the PIR assembly and the microwave assembly mounted thereon of the intrusion detector system shown in FIG. 1;

FIGS. 21 and 22 together show the electronic circuit of the signal processing board of most of the PIR system of the intrusion detector system shown in FIG. 1; and

FIGS. 23 and 24 together show the electronic circuit of the microwave assembly and of part of the PIR system of the intrusion detector system shown in FIG. 1.

Referring to FIG. 1, there is illustrated an exploded perspective view of an intrusion detector system apparatus of the present invention referred to by the general reference character 10. The system 10 includes a package comprising an upper housing 12, a lower housing 14, a wall bracket 16, a swivel ring 18 and a printed circuit board 20.

The printed circuit board 20 is a thin rectangular board having a lower portion of smaller width than the upper portion forming a protrusion 22 on each side of the board 20 and having a lower edge 21 and an upper edge 23. A self-detect microwave assembly 26 and PIR assembly 28 are mounted on the board 20 with the microwave assembly 26 mounted on the larger portion and the passive infrared (PIR) assembly 28 mounted on the lower portion. Both the

assemblies 26, 28 are mounted on the same side of the printed circuit board 20 and face in the same direction so that the detection patterns of each cover the same area.

The bracket 16 comprises a box-like configuration having a bottom wall 30, a first side wall 32, a second side wall 34 and a back wall 36. The first and second side walls 32,34 and the back wall 36 extend from edges of the bottom wall 30 and the back wall 36 connects the first and second side walls 32,34 which are in spaced parallel relation with each other. The forward edge 38 of the bottom wall 30 is arced on a horizontal plane. An extension portion 40 extends from each of the forward edges of the first and second side walls 32,34 forming a continuation of the arc of the forward edge 38 of the bottom wall 30 and being integral therewith. The back wall 36 includes a pair of key hole slots 42 which are positioned on the vertical midline and are spaced from each other. On each side of the upper portion of the back wall 36 a rectangular box-like compartment 44 is positioned. A side wall of each of the compartments 44 is provided by the respective side wall 32 or 34 of the bracket 16 as shown in FIG. 1. An engagement shelf 46 extends from the forward wall of the compartment 44 in spaced parallel relation with the upper surface of the bottom wall 30 and in right angle relation to the first and second side walls 32, 34. Each of the engagement shelves 46 includes a narrow U-shaped engagement slot 48 which opens away from the forward wall of the compartment 44. The forward wall of each of the compartments 44 includes a T-shaped slot 50 which opens upwardly away from the bottom wall 30. A pair of support portions 52 extend upwardly from the upper surface of the

bottom wall 30 and each of them includes a lead into a vertical support slot 54. The support slot 54 includes a floor portion 57 having a cubic rib engagement portion 59 extending vertically therefrom as shown in FIG. . A rectangular opening 56 is provided in the back wall 36 between the two key hole slots 42 providing access to the cable which goes to the printed circuit board 20. The wall bracket 16 is formed of a plastic material, for example, polypropylene.

The lower housing 14 is generally tubular in configuration including a circumferential wall 58 which extends upwardly from a base 60. The base 60 is positioned at an angle to the vertical axis of the lower housing 14. The wall 58 is formed of material which will provide some rigidity and at the same time is adapted to allow passage of infrared radiation. The lower housing 14 is open at the top and includes at the rear section of the wall 58 a series of retaining elements. The retaining elements include a pair of vertically extending ribs 62 which extend from the rim of the lower housing 14 to a predetermined point vertically down from the rim. The ribs 62 are in spaced parallel relation to each other and each of them at their lower end includes a retainer slot 64 spaced from the wall 58. Outboard of each of the ribs 62 an integral ear or projection 66 is provided. Each of the ears 66 comprises a generally rectangular projection extending away from the cavity formed by the wall 58 having a terminal end with a through aperture 68 formed adjacent thereto. A rectangular notch is formed on each side of the ear 66 spaced from the aperture 68 to provide a T-shaped engagement portion 70. A rectangular box-like element 72 is formed inboard of the T-shaped

engagement portion 70 which provides a seating surface 74. A semi-circular key or projection 76 extends from the inner surface of the wall 58 into the area defined by the wall 58. The configuration of the bottom of the lower housing 14 is essentially a circular well defined by a well wall 78 with the free terminal ends 80 of a series of rib elements 82 butting against the well wall 78. Each of the rib elements 82 include an upper surface 84. The upper surfaces 84 of the rib elements 82 lie on the same horizontal plane. The lower housing 14 may be formed of a plastic material such as high density polyethylene or polypropylene.

The upper housing 12 comprises a cap portion 86 from which a circumferential wall 88 extends. The wall 88 is formed of a plastic material, for example, polypropylene, which will pass microwave radiation. A centrally positioned, second well wall 78a extends from the inner surface of the cap portion 86. A 300+ degree circular rib 90 extends from the inner surface of the cap portion 86 in coaxial relation with the vertical axis of the second well 78a and includes an upper surface 91 which lies on a horizontal plane below the upper surface of the second well wall 78a as shown in FIG. 9. A series of cosmetic grooves 92 are formed on the outer surface of the cap portion 86 and are continued for a short distance down the adjacent circumferential wall 88. The formation of these cosmetic grooves 92 create bulges on the inner surface of the cap portion 86 which are without function. A lid portion 94 extends from the external surface of the upper housing 12 at the rear thereof (i.e. that part closest to the mounting wall) and being generally in right angle relation to the

vertical axis of the upper housing 12. With the exception of the side integral with the upper housing 12, the lid portion 94 is generally rectangular in configuration. A through hole 96 is formed in each of the two outer corners of the lid portion 94 for a purpose to be explained hereinafter. A T-shaped projection 98 extends from the lower surface of the lid portion 94 between the through hole 96 and the circumferential wall 88.

The swivel ring 18 comprises a base ring 100 having a first surface 102 and a second surface 104 in spaced parallel relation to the first surface 102. An adjustment ring 106 of smaller diameter than the base ring 100 extends from its first surface 102 in coaxial relation with the base ring 100 and a guide ring 107 of smaller diameter than the adjustment ring 106 extends from the second surface 104, away from the adjustment ring 106 and in coaxial relation with the base ring 100. A series of 9 arcuate notches 108 are formed on the periphery of the adjustment ring 106 and occupy less than 180 degrees of the circumference while being spaced from each other. The purpose of the arcuate notches 108 will be set forth hereinafter. A bearing portion 112 is formed on each side of the inner circumference of the base ring 100. Each of the bearing portions 112 is defined by a chord of the base ring 100, is in opposed relation to each other and includes a PCB engagement slot 114. The PCB engagement slots 114 are in spaced opposed relation to each other. On one of the bearing portions 112 a pair of clamping fingers 116 are formed which hold the leads of an LED 118. On surface 119, which is coplanar with the bearing portions 112 a third clamping finger 116 is provided which assist the other clamping fingers 116

in retaining the leads of the LED 118. A pair of snap-in fingers 121 extend from the surface 119 and are spaced from the clamping finger 116. If the horizontal midline of the pair of snap-in fingers 121 is extended on the diameter of the circular aperture defined by the base ring 100, it will bisect the distance between the two slots 114. The LED 118 is retained in position so that the illumination provided by the LED 118 is always directed away from the vertical axis of the lower housing 14 in substantially right angle relationship to the vertical plane of the PCB 20. The base, guide and adjustment rings 100, 106, 107 are formed of a transparent or translucent material such as a polycarbonate.

The PIR assembly 28 includes an enclosure component 120 mounted so that it faces the inner surface of the wall 58 of the housing 14 permitting infrared radiation to enter the enclosure component 120 from an ambient source.

A signal processing board 122 which carries the electric circuit components of the PIR assembly 28 is positioned in the enclosure component 120 so as not to interfere with radiation directed toward the rear of the enclosure component 120. The signal processing board 122 has a series of first reflective surfaces 124 extending at an acute angle downwardly from the rear edge and the lower surface thereof providing a first concave mirror 126. The first concave mirror 126 is adapted to face the wall 58 of the lower housing 14. A pyroelectric sensor 128 for detecting infrared radiation is connected to the signal processing board 122 by a mount 130 attached to the signal processing board 122. A rectangular notch 132 is formed in the signal processing board

122 opening at a forward edge thereof. The sensor 128 is mounted partially within the area defined by the notch 132 and includes a filter element formed of a material which is transparent to infrared radiation but opaque to visible light. A set of three male, rod-like connectors 134 are supported by a terminal board 136 which extends upwardly, in a direction opposite to the first mirror 126, from the upper surface of the signal processing board 122 adjacent the rear edge thereof. The male connectors 134 are adapted to interconnect with a power source to power the signal processing board 122 and to interconnect with an output device for indicating detection of an object by the sensor 128. As assembled, the signal processing board 122, is inserted into the enclosure component 120 with each of the short terminal edges of the signal processing board 122 slide fitted within a pair of horizontally extending rib elements 138 which extend from the inner surface of the enclosure component 120. The terminal board 136 has a through hole, formed on each side of and spaced from the male connectors 134, which are aligned with a hole formed through the back end of the enclosure component 120 permitting the signal processing board 122 to be attached by screws to the enclosure component 120. A set of three through holes 140 are formed through the back of the enclosure component 120 and are spaced from and horizontally aligned with each other. Each of the holes 140 is adapted to permit passage of one of the male connectors 134 therethrough whereby their terminal ends extend beyond the enclosure component 120 where they may be connected to other elements (not shown).

FIG. 11 discloses a front elevational view of the inside of the enclosure component 120 whose

interior surface is completely covered with reflective material. This interior surface includes a lower concave reflective surface 142, which extends to a line slightly above the through holes 140, an intermediate concave reflective surface formed of five intermediate reflective segments 144 and an upper concave reflective surface formed of three concave reflective segments 146. The angular relationship between the upper reflective segments 146 and the intermediate reflective segments 144 is shown in FIG. 12.

FIG. 13 is a front elevational view of the assembly of the signal processing board 122, the first mirror 126, the pyroelectric sensor 128 and the terminal board 136. The first mirror 126, as shown, is formed of seven (7) reflective surfaces 124 and is positioned in spaced, forward relationship to the lower concave reflective surface 142 when the assembly is attached within the enclosure component 120.

Note that, as shown in FIG. 16, when the signal processing board 122 is engaged within the enclosure component 120, the lower concave reflective surface 142 is covered by the rear of the first mirror 126. Impinging radiation is thereby reflected from the upper reflective segments 146, the intermediate reflective segments 144 and the first reflective surfaces 124.

FIG. 15 is a perspective view of the rear of the assembly of the signal processing board 122, the first mirror 126, the pyroelectric sensor 128 and the terminal board 136, illustrating the relationship of the sensing surfaces of the pyroelectric sensor 128. The pyroelectric sensor 128 includes a pair of detectors 148 which are positioned so that half of

each detector 148 is located on one side of the signal processing board 122 and the other half is located on the other side of the signal processing board 122. The position of the detectors 148 permits infrared radiation reflected from the upper reflective segments 146, the intermediate reflective segments 144 and the first reflective surfaces 124 to impinge on the detectors 148 in some instances through the rectangular notch 132.

FIG. 17 is a top plan view of a room disclosing the intrusion detector system apparatus 10 mounted centrally on a wall of the room having lines drawn to indicate the surveillance pattern and showing the first reflective surfaces 124, the intermediate reflective segments 144 and the upper reflective segments 146 diagrammatically. The first reflective surfaces 124 will focus radiation on to the detectors 148 from a field defined by the solid lines and the numeral 124. The upper reflective segments 146 will focus radiation on to the detectors 148 from a field defined by the solid lines and the numeral 146. The intermediate reflective segments 144 will focus radiation on to the detectors 148 from a field defined by the solid lines and the numeral 144.

FIG. 18 is a cross-sectional view of the room shown in FIG. 17. The fields from which radiation is focused on to the detectors 148 are again shown by solid lines and the numeral of the reflective surface associated with the field. As illustrated in FIGS. 17 and 18 only discrete fields are under surveillance.

The intrusion detector system 10, of the present invention is mounted on the wall of a room, for example, or in the corner of a room and is assembled in place. Assuming that the intrusion

detector system 10 is to be mounted in a corner, a triangular mounting bracket 150 is positioned in a corner at a predetermined height and screwed in place. Two tapped holes 152 are provided on the vertical midline of the front face 156 of the mounting bracket 150. The tapped holes 152 are vertically spaced from each other. A screw 158 is engaged with each tapped hole 152 and has its head spaced from the front face 156 of the mounting bracket 150. A snap on U nut 160 is attached to each of the engagement shelves 46 with the threaded portion of the U nut 160 positioned below and aligned with the engagement slot 48. The upper portion of the U nut 160 is in superposed, abutting relationship with the engagement shelf 46. An electric cable 162 extends from a power source (not shown). The wall bracket 16 is connected to the mounting bracket 150 by engaging each of the screws with its respective keyhole slot 42. This positions the backwall 36 of the wall bracket 16 in abutting relation to the front face 156 of the mounting bracket 150. The electric cable 162 is passed through the opening 56 in the back wall 36.

The lower housing 14 is assembled with the attached wall bracket 16 positioning each of the retaining slots 64 over and into engagement with its respective rib engagement portion 59. Simultaneously, each of the ears 66 is positioned over the shelf 46 and its respective mounting U nut 160 with the aperture 68 in coaxial relation with the holes in the U nut 160 and the engagement slot 48 of the shelf 46. One of the T-shaped engagement portions 70 is positioned in each of the T-shaped slots 50 of the compartments 44.

The subassembly of the PCB 20, the

microwave assembly 26 and the PIR assembly 28 is placed in the swivel ring 18 by sliding the side edges of the PCB 20 in the opposed engagement slots 114 until the protrusions 22 of the PCB 20 abut the surfaces of the bearing portions 112 adjacent the engagement slots 114 thereby forming a ring-PCB assembly 115. In this position, the base ring 100 is in superposed relation to the adjustment ring 106 and the adjustment ring 106 is in close proximity to the PIR assembly 28. The ring-PCB assembly 115 is engaged with the mounted lower housing 14 by inserting the lower portion (i.e. narrower portion) into the lower housing cavity until the lower edge 21 of the PCB 20 butts against the upper surfaces 84 of the rib elements 82 of the lower housing 14 and a portion of the PCB 20 bears against and is tangent to well wall 78 as shown in FIG. 9. The adjustment ring 106 is within the cavity and the base ring 100 rests on the upper edge of the lower housing 14. The periphery of the base ring 100 lies on the same vertical plane as the external surface of the lower housing 14. The PIR assembly 28 is positioned in the lower housing cavity. Assuming a 90 degree position of the PIR assembly 28 and the microwave assembly 26 is desired, the key 76 of the lower housing 14 is engaged within the fifth notch 108 of the adjustment ring 106 and the first surface 102 rests on the upper edge of the lower housing 14. Should a different target area be desired and therefore a different degree position of the PIR assembly 28 and the microwave assembly 26, the installer would engage the key 76 with a different notch 108, as indicated in phantom line in FIG. 7. After connecting the electric cable 162 to the PCB 20, the installer may verify the detection pattern for the different target

area by observing the LED 118 as he walks into the target area from each direction. As he enters the outer boundaries, of the detection patterns of the PIR assembly 28 and microwave assembly 26, the LED 118 will be activated visually indicating the pattern boundaries for the different degree position resulting from the engagement of a notch 108 with the key 76. The printed circuit board 20 is biased 4 degrees from the 90 degree vertical when it is mounted in the lower housing 14.

The upper housing 12 is now assembled with the mounted lower housing 14 and ring-PCB assembly 115 by butting the upper edge 23 of the PCB 20 against the upper surface 91 of the circular rib 90 of the upper housing 12. A portion of the PCB 20 bears against and is tangent to the second well wall 78a. The free edge of the upper housing 12 butts against the second surface 104 of the base ring 100. The guide ring 107 is thereby positioned within the cavity of the upper housing 12 and each of the through holes 96 is axially aligned with the aperture 68 of the ear 66. In this position each of the T-shaped projections 98 bears against the upper surface of its underlying ear 66. A screw is passed through the alignment of a through hole 96, an aperture 68, the hole in the upper portion of the U nut 160, the engagement slot 48 of the shelf 46 and then threaded into engagement with the internally threaded portion of the U nut 160 completing the assembly of the intrusion detection system 10.

The circuit diagrams of FIGS. 21, 22 represent the signal processing circuit for the PIR assembly 28 as it is positioned on the first printed circuit board 122 and is referred to by the numeral 164. The first stage of the circuit 164 is the

detector circuit network 166 which includes the pyroelectric sensor 128 which in the embodiment disclosed has dual detectors 148 which are connected in series and a field effect transistor 168. The first RF by-pass capacitor 170 is part of the detector circuit network 166 and is connected to the transistor 168. The emitter follower transistor 172 provides a semi-regulated source voltage from supply rail 174 to the detector circuit network 166. The first RF by-pass capacitor 170 shunts any high frequency noise around the pyroelectric sensor 128. The second capacitor 176 shunts high frequency from the output of the pyroelectric sensor 128 back to ground. The first voltage rail 178 and the second or common voltage rails 180 form the input of the detector circuit network 166 providing a potential across the pyroelectric sensor 128. The output signal from the detector circuit network 166 appears on the line 182. The resistor 184 and capacitor 186 provide a load for the sensor 128. The output signal from the detector circuit network 166 passes along line 182 into the amplifier chain comprising operational amplifiers 188,190 and 192 which serve as a band pass amplifiers in the range .3 to 10 hertz. The selection of the values of the components around the operational amplifiers 188,190,192 is such that the gain would fall off below .3 hertz and above 10 hertz. The purpose of the amplifier chain is to take the output signal from the detector circuit network 166, buffer it, increase it in amplitude and limit the amount of band pass. The output of the operational amplifier 188 is fed back to the inverting input of the operational amplifier 188 through a feed back loop comprising a capacitor 194 which is in parallel with a resistor 196 and in

series with a resistor 198. This feedback loop is connected to the second voltage rail 180 through a resistor 200 which is in series with a capacitor 202.

The output terminal of the operational amplifier 188 is connected through a capacitor 204 and a resistor 206, which is connected in series therewith, to an inverting input terminal 208 of the operational amplifier 190. The operational amplifier 190 has its output fed back to the input terminal 208 through a feedback loop comprising a capacitor 210 in parallel with a resistor 212. A non-inverting input terminal of the operational amplifier 190 is connected to the non-inverting input terminal of the operational amplifier 192. The output terminal 214 of the operational amplifier 190 is connected through a capacitor 216 and a resistor 218, which is connected in series therewith, to an input terminal 220 of the operational amplifier 192. If an additional gain is required over that supplied by the operational amplifiers 188,190, the gain supplied by the operational amplifier 192 can be varied by varying, in a manner well known in the art, the value of a resistor 222.

A non-inverting input terminal 224 of the operational amplifier 192 is connected to the common voltage rail 180 through a filtering capacitor 226.

The output of the amplifier chain is received by a level detection stage 228 having a first operational amplifier 230 and a second operational amplifier 232. The non-inverting input terminal of the first operational amplifier 230 and the inverting input terminal of the second operational amplifier 232 are joined in common to the output of the operational amplifier 192. As

illustrated, the second operational amplifier 232 functions in the inverting mode, while operating amplifier 230 functions as a non-inverting comparator.

A voltage divider network 234 includes five resistors and is designed to set up a number of reference voltages over which the system will work. The supply rail 174 may be set at five volts, for example; therefore, all the operational amplifiers are working with a power supply voltage of five volts. If the system is to operate as linear as possible, the quiescent operating point of the first and second operational amplifiers 230,232 should be midway between the power rail 174 and the common rail 180. The five resistors of the voltage divider network are numbered 236,238,240,242 and 244. Assuming that the two resistors 236,238 have a combined resistance of 276 K and the three resistors 240,242,244 have a combined resistance of 276 K, for example, a reference terminal 246 is positioned midway between the mentioned two resistors 236,238 and the mentioned three resistors 240,242 and 244 and is connected to all of the reference inputs of the operational amplifiers in the operational amplifier chain. The output from a junction 248 of the voltage divider resistor pair 236,238 is connected to the negative input of the operational amplifier 230. The output from a junction 250 of the voltage divider resistor pair 240,242 is connected to the positive input of the operational amplifier 232. The values of the resistors are calculated to create a symmetrical system such that, for example, the value of the resistor 236 may be 220 K so that this value of resistance exists from the junction 248 to the plus or first voltage rail 178 and the value of the

resistors 242,244 together equal 220 K so that this value of resistance exists from the junction 250 to the minus or second voltage rail 180. This sets a value of 1/2 volt difference from the reference input 246 to both junctions 248 and 250. For example, the value of the voltage at the junction 250 will be 2 and the value of the voltage at the junction 248 will be 3 assuming a 2.5 voltage value at the reference input 246. This means that the one of the two operational amplifiers (i.e. comparators) 230,232 change state whenever the voltage of the operational amplifier that is looking at the pyroelectric sensor 128 puts out a voltage that is greater than .5 volts. The outputs of the comparators 230,232 are each connected to a resistor 252 and to a decoupling diode 254. The comparator 230 is connected to the resistor 252 and the decoupling diode 254 and the comparator 232 is connected to a resistor 256 and a decoupling diode 258. The decoupling diodes 254,258 serve to decouple the comparators 230,232 from the time constant networks 260,262 which are electrically downstream from them. To recapitulate, when the voltage swings .5 volts on either side of the midpoint 2.5 volts the associated comparator trips creating a positive going signal which is passed by its associated decoupling diode into its associated timing resistor and capacitor. The associated timing resistor and capacitor of the comparator 230 is a resistor 264 and the capacitor 266 and the associated timing resistor and capacitor of the comparator 232 is a resistor 268 and a capacitor 270. The R-C networks 264,266 and 268,270 define a signal sustaining or pulse stretching network wherein the positive pulse is stored on the capacitor and slowly bled off by the resistor. In effect, this circuitry

takes a pulse input and turns it into a slowly decaying exponential. Assuming that the voltage at the junction 248 was reached, it would indicate that a positive going pulse was accepted by the level detector stage. The logic of the system is arranged such that a positive going pulse must be followed by a negative going pulse, indicating passage of an intruder through a "window" in the PIR detector (single mirror segment) within a prescribed time period to avoid activating the system by electrical noise. The signal would now go below the voltage at the junction 250 and the pulse would be detected by the comparator 232 and would be coupled through its decoupling diode 258 and then be reacted upon by its associated timing resistor 268 and capacitor 270 creating the wave form shown at FIG. 5 D. Downstream of the first and second operational amplifiers, i.e. comparators 230,232, is a second set of comparators in this case the comparators 272,274. The output from the junction 276 downstream of the resistor 252 and the R-C network 264,266 and the decoupling diode 254 is connected to the positive input of the comparator 272. The output from the junction 278 downstream of the resistor 256 and the R-C network 268,270 and the decoupling diode 258 is connected to the positive input of the comparator 274. The comparators 272,274 may be referred to as part of the logic system. The comparators 272,274 are referenced to the voltage appearing at a junction 280 positioned between the resistor 242 and the resistor 244. The reference point or junction 280 was chosen because the exponentials decay all the way back to ground. If there is a signal across either one or both of the integrating R-C circuits 264,266 or 268,270 that is greater than, say, a volt then the associated

comparator will turn on and there will be essentially 3.8 volts across its output. If both the comparators 272,274 turn on, the output voltage would be high, if only one comparator 272 or 274 is tripped, the output voltage would be zero. To put it another way, if both comparators 272,274 trip, then the direct output of each comparator 272,274 is approximately 3.8 volts and their combined output at a junction 282, due to the fact that the resistors 284,286 are balanced, will also be 3.8 volts. If, on the other hand, only one of the comparator 272 or 274 trip, then the direct output of one comparator would be 3.8 volts and the other would be 0 volts and their combined output at junction 282 due to the fact that the resistors 284,286 are balanced will be half of that, i.e. 1.9 volts. The junction 282 is connected to the negative input of a comparator 288 whose positive input is connected to the three volt junction 248. If the input voltage from the comparators 272,274, and the resistor network 284,286 is 3.8 volts, the output of the comparator 288 will be less than .8 volts and if that output is 0 or 1.9 volts, then it will be approximately 3.8 volts. The comparators 272.274,288 thus form an AND gate. If a positive pulse is followed in time by a negative pulse or if a negative pulse is followed in time by a positive pulse, the conditions will be met that will cause the output of the comparator 288 to go low thereby sending out an alarm signal.

The circuit diagram of FIGS. 23 and 24 represents the signal processing circuit for the PCB assembly as it is positioned on the signal processing board 122 and is referred to by the numeral 290. The resistor 292 is connected to the top of a zener 294 and has as a source the 9.4 volt rail 296 producing a

regulated voltage of 5 volts which is the source for the PIR circuit 164. A capacitor 298 and the resistor 300 are connected across the input of the PIR processor to the logic block for RFI protection. This signal is coupled to the input of a comparator amplifier 302 which determines the difference between the two logic levels. A resistor 304 serves as a load resistor for the comparator amplifier 302. The voltage on the input 306 of the comparator amplifier 302 is compared to the voltage on a positive input 308 which is generated by a voltage divider 310 made up of the resistors 312,314,316 and 318. The reference voltage produced across resistor 318 appears at a junction 320. When the voltage on the input 306 of the comparator amplifier 302 exceeds 1.8 volts, it will change state. The output on the comparator amplifier 302 will be essentially zero. Assuming that the PIR circuit 164 is in the alarm condition, the voltage on the input 306 will go to zero and an output 322 of the comparator amplifier 302 will go high. The current of the output 322 will flow through resistor 324 charging a capacitor 326 toward 7.6 volts. A resistor 328 in parallel with the capacitor 326 serves to discharge that capacitor and also to form part of a voltage divider with the resistor 324. The alarm condition from the PIR circuit 164 terminates and the voltage on the input 306 of the comparator amplifier 302 goes high thereby causing its output 322 to go low. A diode 330 keeps the voltage developed at capacitor 326 from going back into the output 322. There is no path for charging an input 332 of a comparator amplifier 334 and the only path available is through the resistor 328 which starts to discharge the capacitor 326 over a time constant (approximately four seconds). The

voltage at the cathode of the diode 330 starts to fall from 7.6 volts until it reaches approximately 2.8 volts during which time the comparator amplifier 334 will alter states and stay toggled to the high condition (i.e. 7.8 volts). When the voltage at the input 332 reaches 2.8 volts, the comparator amplifier 334 will return to the low state. To summarize, the function of the comparator amplifiers 302,334 is to take the alarm condition from the PIR circuit 164 of the PIR assembly and stretch it over a time period. A resistor 336 and a diode 338 are used to indicate the alarm condition and form the end of the PIR logic chain.

We start the description of the PCB assembly 26 at the input power pin 340 and the common pin 342 and the first element that we see is the capacitor 344 which functions to eliminate spiking from the input thereby blocking such interferences from the regulator. The next element is a fuse 346 which acts as protection for a failed unit and which acts in conjunction with a diode 348 to prevent inadvertent application of backward polarity to the unit. If the input power pin 340 were held negative with respect to common, a current would flow through the fuse 346 through the diode 348 to common. There being no resistance in that circuit the fuse 346 would blow, while the diode 348 serves to limit reverse voltage application to its forward drop (approximately .6 volts DC) within limits for non-damaging operation. Power then passes primarily from the output of the diode 348 to a transistor 350 which is part of a series pass regulator including a transistor 352 and an operational amplifier 354. Transistor 352 acts as a variable resistance changing the amount of current that passes from its collector

to its emitter in response to the amplifier output. The goal is to maintain the voltage on the emitter of transistor 350 at 7.5 volts as the optimum bias potential of the Gunn diode. Transistor 350 is connected into the circuit as an emitter-follower, and as is well known the voltage on the emitter is the voltage applied to the base minus the base emitter voltage drop of the transistor 350. Therefore, the most efficient control of the emitter voltage is accomplished by control of the base voltage. It takes a lot smaller power dissipation at the base to control a larger power dissipation from collector to emitter. The transistor 350 thus acts as an amplifier (non-linear resistor). The voltage on the base of transistor 350 is supplied by the amplifier 354. A resistor 356 supplies current from the emitter of transistor 350 to the cathode of a zener diode 358 which controls the voltage at a pin 360 of the amplifier 354. A pin 362 of amplifier 354 is connected to a voltage divider made up of resistor 356, a potentiometer 364, a resistor 366 and a resistor 368. A voltage is thus generated at the wiper of the potentiometer 364 which has a value between the potential of a rail 370 and the common rail. The function of the zener diode 358 is to maintain a stable reference voltage at pin 360 irrespective of the voltage applied to the resistor 356. The voltage divider formed by the resistor 366, the potentiometer 364 and the resistor 368 provides a chain between the rail 370 and the common rail which reflects the current voltage of the rail 370. If, for example, the voltage on the rail 370 was 7.9 volts, this would cause the voltage on pin 362 to change in the direction of the error. Any rise in the voltage at the voltage divider formed by the

resistor 366, the potentiometer 364 and the resistor 368 will be immediately countered by a falling voltage at the pin 372 which, in turn, will cause the voltage on the base of the transistor 350 to fall causing the voltage of its emitter to fall bringing the voltage across the voltage divider resistor 366, the potentiometer 364 and the resistor 368 back to 7.5. The potentiometer is adjusted to obtain, in this case, the desired voltage of 7.5 volts. Resistors 374,376 are part of the design of the operational amplifier 354 and serve to compensate for leakage currents at the inputs to the amplifier 354. Resistors 378,380 form a voltage divider for producing voltage across the base of the transistor 350. The transistor 352 has its collector tied to the source, its emitter being an output terminal and its base being connected to a network. The difference between the element configuration of the transistor 350 and the transistor 352 is that the base of the transistor 352 is directly controlled by a zener diode 382. Resistor 384 and zener diode 382 make up a potential source which is applied directly to the base of transistor 352. Therefore, the transistor 352 follows the voltage applied to its base minus the base emitter drop. With the zener diode 382 having a value of 10 volts with a base emitter drop of .6 volts, the output of the transistor 352 should be 9.4 volts. The function of a capacitor 386 is to filter out any rapid change in the zener control voltage at the base of transistor 352. The transistor 352 provides a 9.4 volt regulated source at the rail 296 and for the base drive transistor 350.

The 7.5 voltage at the emitter of the transistor 350 acts as the source for a microwave

detector comprising a Gunn diode (not shown) and a Schottky diode (not shown) in an appropriately tuned cavity (not shown), all well known in the art. The Gunn diode is biased by the 7.5 supply and self oscillates creating an RF signal. A small portion of this signal is directed towards the Schottky diode which also is exposed to a portion of the signal reflected from targets in the range of the RF radiation. If the target is moving there is a shift in frequency between these two signals, known as the Doppler shift, which is converted by the rectifying action of the Schottky diode into a low frequency AC signal returned by a line 388 back to the main PCB circuitry there first encountering a capacitor 390. The capacitor 390 serves as a DC blocking capacitor to remove constant amplitude signals from fixed targets. A potentiometer 392 is used to set the overall amplitude of the AC signal which will be effectively applied to an operational amplifier 394. The portion of that signal relative to 7.5 volts is applied directly to the operational amplifier 394 through a resistor 396. A resistor 398 assures that even if the potentiometer 392 is turned to zero the amplitude of the AC signal will not become zero. A negative pin 400 of the operational amplifier 394 is attached to a network. A resistor 402 and the resistor 396 supply the gain of the network (i.e. the value of resistor 402 divided by the value of resistor 396). This figure provides the amplification factor of the operational amplifier 394. Resistors 404,406 function as compensating resistors. A capacitor 408 supplies a roll off for the operational amplifier 394. It is particularly important for two reasons: it provides RFI protection and causes a roll off of all signals out of the

frequency spectrum we are interested in. The output of the operational amplifier 394 is passed through a capacitor 410 which blocks any DC signal so that only an AC signal is delivered to a resistor 412. An operational amplifier 414 includes a pin 416 which acts as a reference for the operational amplifier 414. The reference voltage at pin 416 is generated by a voltage divider comprising resistors 418, 420 tied across the 7.5 rail 370 and the common rail and providing, for example, 6.52 volts as the reference. The AC signal is coupled into the operational amplifier 414 through the resistor 412. The feed back network of the operational amplifier 414 includes a resistor 422, which sets the gain and a capacitor 424 provides high frequency roll-off. The output at pin 426 of the operational amplifier 414 is actually the output of the microwave detector. The reference voltage of the voltage divider comprising resistors 418,422 establish an output level upon which the circuitry will impress the AC signal at pin 426 and provide minimum bias for operation of a diode 428. A DC potential generated across the top of a capacitor 430 resulting from a current flowing through a resistor 432 causes capacitor 430 to charge toward 7.5 volts. Assuming a microwave signal has been detected, this will cause the signal between the input at a pin 434 and pin 416 of the operational amplifier 414 to go high. The output at pin 426 of the operational amplifier 414 will then go low and the integrating capacitor 430 discharges rapidly through diode 428 into operational amplifier 414 causing the voltage on capacitor 430 to fall. This causes a corresponding fall at a pre-alarm point 436. Thus, a time constant is provided by the resistor 432 and the capacitor 430 so that reaction to non-alarm

outputs of the operational amplifier 414 are not instantaneous and therefore the voltage on the pre-alarm point 436 will not change immediately. The voltage on the capacitor 430 is applied through pre-alarm point 436 to two amplifiers one of which is a follower amplifier 438. The purpose of the amplifier 438 is to provide a buffered output 440 from the detector system that allows a check of the suitability of the microwave position. A voltage is generated on the output of the amplifier 438 which is exactly equal to the voltage applied at its input pin 442. The only purpose of amplifier 438 is to provide a signal which is buffered but is the same as that applied at pin 442. A comparator amplifier 444 is the main alarming comparator. A positive input is supplied by the voltage divider formed by resistors 446,448 through a blocking diode 450 which allows a signal to pass to a capacitor 452. This signal is shunted by a resistor 454 which charges to the voltage of the pre-alarm point 436. This is an example of automatic gain control. The normal background signal that the microwave picks up will always have some AC component in it due to normal phase shift and the background composite signal. This input provides a zero point or no intrusion reference. Since this reference may change slowly over time the input must be an active network that can adjust itself, thus allowing very slow change in reference signals by charging or discharging the capacitor 452 incrementally. The same signal is also coupled to a negative input 456 of the operational amplifier 444 by passing it through the blocking diode 450 which allows a filtered signal to pass to a capacitor 458 which is shunted by a resistor 460. Due to the lower value of the capacitor 458 in

relation to the capacitor 452, the negative input 456 will react to a signal change, for example, five times faster. Thus, if the signal is rapidly changing and if the change is large enough, a small voltage difference will occur between the negative input 456 and the positive input and that signal will be amplified by the operational amplifier 444. If the system detects motion, the voltage across the capacitor 430 will decrease, because the diode 428 is conducting and the charge is being drained off. Therefore, there will be less potential on the anodes of the diode 450 and a diode 462. This latter condition causes the voltage on the integrating networks, capacitor 452, resistor 454 and capacitor 458, resistor 460, to fall because the time constant of the capacitor 458 is so much smaller than that of the capacitor 452. The voltage on the capacitor 458 will fall more rapidly and thus, in the same period of time the capacitor 458 will attain a lower voltage than the capacitor 452 causing the net potential across the operational amplifier 444 to be negative. The operational amplifier 444 being in the inverting mode will produce a positive output voltage. A resistor 463 will conduct a current activating the yellow indicator 464 showing the microwave system has detected a motion. This competes the microwave portion of the alarm system.

As stated hereinbefore, the output of the PIR assembly 28 is available at the input of the resistor 336 and the microwave signal is available at the input of a resistor 466 and if both inputs indicate an alarm condition, the voltage at pin 468 of an operational amplifier 470 will be approximately 7.5 volts. If either the output of the PIR assembly 28 or the microwave signal at the input of the

resistor 466 is low and the other is high the voltage at pin 468 will be that generated by the voltage divider made up of the resistors 336,466, i.e. approximately 3.5 volts. The other input to the operational amplifier 470 at its pin 472 is tied back to the voltage divider 310 made up of resistors 312, 314,316 and 318.

If the voltage applied to pin 468 of the operational amplifier 470 exceeds 6.1 volts, the voltage on pin 472, the net input to the operational amplifier 470, will be positive and the amplifier will have a positive output at a pin 474, otherwise it does not. 3.5 volts on pin 468 will be treated exactly the same way as 0 volts. Thus, at the output pin 474 of the operational amplifier 470, the voltage will be 0 in the non-alarm condition and 7.6 volts in the alarm condition, for example. Assuming an alarm condition a capacitor 476 will be charged through a blocking diode 478 and will slowly discharge, after the alarm condition has ceased, through a resistor 480. This voltage appears at pin 482 of an operational amplifier 484. A positive input pin 486 is connected back to the voltage divider 310 comprising the resistors 312,314,316 and 318 which in this case holds the voltage at say 2.8 volts. Therefore, as long as the voltage at pin 482 of operational amplifier 484 is greater than 2.8 volts, the operational amplifier 484 output at a pin 488 will be negative, which is the alarm condition. The purpose of an operational amplifier is to invert the alarm signal that appears at pin 488 of the operational amplifier 484 and to utilize it for two purposes: 1) to display the alarm condition at an indicator 492 through a resistor 49, and 2) provide an inverted signal which is fed back to diode 496

connected to one terminal of a latch 498 allowing the unit to be locked up in the alarm state once it has alarmed. The other terminal of the latch 498 is connected to the negative input pin 482 of the operational amplifier 484. If the two terminals of the latch 498 are connected together, the alarm condition once achieved will be maintained. The latch 498 can also be used as a test point. The output of the operational amplifier 484 is coupled through a resistor 500, acting in conjunction with the resistor 501, to the base of a transistor 502 which serves as a relay driver to transmit the alarm condition. The transistor 502 is coupled to a network comprising a capacitor 504, a resistor 506, a coil 508 of a relay 510 and a diode 512. In a situation where the relay 510 is not pulled in, for example, just after an alarm, the capacitor 504 will have discharged through the resistor 506 to the point where there is little or no charge on the capacitor 504. Assume the alarm condition terminates and the latch 498 is not in use, current passes to the base of the transistor 502 causing a current to flow from a 12 volt rail 514 through the relay coil 508 and then initially through the capacitor 504 and the collector emitter junction of the transistor 502 to common, causing the relay 510 to pull in. As time goes on, the capacitor 504 is charged through the resistance of the relay coil 508 until no current passes through the fully charged capacitor 504 causing all the current to pass through resistor 506 and the collector emitter junction of the transistor 502 to ground. This effectively lowers the voltage applied to the relay coil 508, limiting power consumption by the relay 510. A resistor 506 provides a path for leakage voltage. The diode 512

protects the transistor 502 from the effects of back EMF when the relay 510 opens, during a detected alarm state. Use of unactivated contacts for the alarm state insures that common failure of components in the output state result in an alarm condition. The capacitors 536 act to protect the contacts of the relay 510.

The resistor 516 and the capacitor 518 form a further filtering network for the PIR circuitry as shown in FIG. 21.

As shown in FIG. 23, the capacitor 520 acts as an input filter while the capacitor 522 functions as an RF by-pass capacitor as does the capacitor 526. The capacitor 524 functions as a DC blocking capacitor.

In FIG. 24 the resistor 528 functions to limit current. The voltage divider made up of resistors 530,532 provides a reference point for the amplifier 444. The resistor 534 is a current limiting resistor for the latch 498.

CLAIMS

1. An infrared intrusion detector for detecting the presence of an intruder comprising: a housing having a front surface through which infrared radiation may pass; a plurality of reflective surfaces positioned within the apparatus housing; a detector circuit network including two sensing areas located in proximity to the reflective surfaces and adapted to generate a signal in response to movement of the intruder through a field defined by one of the reflective surfaces; amplifier means connected to the output of the detector circuit network for amplification of the signal; level detection means connected to the output of the amplifier means for producing an alarm signal when the amplified signal reaches a predetermined level.

2. An infrared intrusion detector for detecting the presence of an intruder comprising: an apparatus housing including a housing cover having a front surface through which infrared radiation may pass; a plurality of reflective surfaces positioned within the apparatus housing; a first detector circuit network including two sensing areas located in proximity to the reflective surfaces and adapted to generate a first and second signal in response to movement of the intruder through a beam defined by one of the reflective surfaces; amplifier means connected to the output of the first detector circuit network for amplification of the first and second signals; level detection means connected to the output of the amplifier means for producing first and second level detection signals when the amplified first and second signals reach a predetermined level; signal sustaining means connected to the output of the level detection means whereby the first level

detection signal is sustained for a sufficient period so that under an alarm condition the second level detection signal will be available during the time period that the first level detection signal is being sustained; and gate means connected to the signal sustaining means for providing an output indicating the presence of an intruder when the sustained first level detection signal is available at the same time as the second level detection signal is produced by the level detection means.

3. The infrared intrusion detector of Claim 2, wherein each of the reflective surfaces defines a discrete field.

4. The infrared intrusion detector of Claim 2, wherein the signal sustaining means comprises an RC network for sustaining the output of the level detection means.

5. The infrared intrusion detector of Claim 2, wherein the gate means comprises an AND gate providing an output from the apparatus housing when an alarm condition is detected.

6. The infrared intrusion detector of Claim 2, further comprising means for avoidance of random false triggering which comprises having the output of the first and second signal sustaining means connected to the first and second inputs respectively of an AND gate such that the AND gate produces an output only in the presence of both first and second level detection signals.

7. A signal processing circuit for an infrared intrusion detector adapted for detecting the presence of an intruder comprising: a detector circuit network including two sensing areas adapted to generate a first and second signal in response to movement of the intruder; voltage mode amplifier means connected

to the output of the detector circuit network for amplification of the first and second signals; level detection means connected to the output of the amplifier means for producing first and second level detection signals when the amplified first and second signals reach a predetermined level; signal sustaining means connected to the output of the level detection means whereby the first level detection signal is sustained for a sufficient period so that under an alarm condition the second level detection signal will be available during the time period that the first level detection signal is being sustained; and gate means connected to the signal sustaining means for providing an output when an alarm condition is detected by the detector circuit network.

8. The signal processing circuit for the infrared intrusion detector of Claim 7, wherein the detector circuit network includes means for filtering power supply transients connected between the voltage mode amplifier and a voltage source.

9. The signal processing circuit for the infrared intrusion detector of Claim 8, wherein the means for filtering power supply transients comprises an RC network connected between the voltage mode amplifier and the voltage source.

10. The signal processing circuit for the infrared intrusion detector of Claim 7, wherein the amplifier means has a band-pass corresponding to the walking speed of a human.

11. The signal processing circuit for the infrared intrusion detector of Claim 7, wherein the signal sustaining means comprises an RC network.

12. The signal processing circuit for the infrared intrusion detector of Claim 7, wherein the gate means comprises an AND gate connected to the

signal sustaining means for providing an alarm output.

13. The infrared intrusion detector of Claim 7, further comprising means for avoidance of random false triggering which comprises having the output of the first and second signal sustaining means connected to the first and second inputs respectively of an AND gate such that the AND gate produces an output only in the presence of both first and second level detection signals.

14. The infrared intrusion detector of Claim 7, further comprising means for avoidance of random false triggering which comprises having the output of the first and second signal sustaining means connected to the first and second inputs respectively of an AND gate such that the AND gate produces an output only in the presence of both first and second level detection signals.

15. The combination of an infrared intrusion detector and a microwave intrusion detector for detecting the presence of a moving body, the infrared intrusion detector having a field of view including the field of view of the microwave intrusion detector, the infrared intrusion detector comprising: an apparatus housing positioned within a housing having a surface through which infrared and microwave radiation may pass, a plurality of reflective surfaces positioned within the housing; a first detector circuit network including two sensing areas located in proximity to the reflective surfaces and adapted to generate a signal in response to movement of the body through a field defined by one of the reflective surfaces; amplifier means connected to the output of the first detector circuit network for amplification of the signal; first level detection means connected to the output of the amplifier means

for producing a first detection signal when the amplified signal reaches a predetermined level; the microwave intrusion detector having a second detector signal electrically connected to the first detection signal of the infrared intrusion detector producing an alarm state only after both the infrared intrusion detector and the microwave intrusion detector have been tripped; a first signal detection sustaining means connected to the output of the first level detection means whereby the first detection signal is sustained for a sufficient period so that under an alarm condition the second detection signal will be available during the time period that the first detection signal is being sustained; gate means connected to the first signal detection sustaining means for providing an alarm indicator output indicating the presence of an intruder when the sustained first detection signal is available at the same time as the second sustained detection signal.

16. The combination of an infrared intrusion detector and a microwave intrusion detector for detecting the presence of a moving body, the infrared intrusion detector having a field of view including the field of view of the microwave intrusion detector, the infrared intrusion detector comprising: an apparatus positioned within a housing having a surface through which infrared radiation may pass; a plurality of reflective surfaces positioned within the apparatus housing; a first detector circuit network including two sensing areas located in proximity to the reflective surfaces and adapted to generate a first and second signal in response to movement of the body through a field defined by one of the reflective surfaces; amplifier means connected to the output of the first detector circuit network

for amplification of the first and second signals; level detection means connected to the output of the amplifier means for producing first and second level detection signals when the amplified first and second signals reach a predetermined level; first signal sustaining means connected to the output of the level detection means whereby the first level detection signal is sustained for a sufficient period so that under an alarm condition the second level detection signal will be available during the time period that the first level detection signal is being sustained; gate means connected to the signal sustaining means for providing a first indicator output indicating the presence of an intruder when the sustained first level detection signal is available at the same time as the second level detection signal is produced by the level detection means; the microwave intrusion detector having a second indicator output connected to the first indicator output of the infrared intrusion detector producing an alarm state only after both the infrared intrusion detector and the microwave intrusion detector have been tripped.

17. A housing for an intrusion detector system, the housing comprising a cup shaped upper housing 12, a cupped shaped lower housing 14, attachment means 16, a swivel ring 18 and a printed circuit board 20, a detector means mounted on the board 20, the swivel ring 18 comprising a base ring 100 having a first surface 102 and a second surface 104 in spaced parallel relation to the first surface 102, an adjustment ring 106 extending from the first surface 102 in coaxial relation with the base ring 100 and engagement means extend from the second surface 104 base ring 100, a series of notches 108 are formed on the periphery of the adjustment ring 106 facing away

from the vertical axis of the swivel ring 18 and printed circuit board engagement means formed therein, the lower housing 14 having a wall defining a cavity, the wall of the lower housing 14 having a projection 76 extending therefrom into the cavity, an upper surface defining an opening into the cavity of the lower housing 14 and having an external surface, the upper housing 12 having a circumferential wall 88, the circumferential wall 88 defining a cavity, having an abutment surface defining an opening into the cavity of the upper housing 12 and having an external surface, the printed circuit board 20 engaged with the printed circuit board engagement means of the swivel ring 18, the assembly of the printed circuit board 20 and the swivel ring 18 is engaged with the lower housing 14 with the first surface 102 of the base ring 100 positioned on the upper surface of the lower housing 14 and the projection 76 of the lower housing 14 engaging a notch 108 of the adjustment ring 106, the abutment surface of the upper housing 12 bearing against second surface 104 of the swivel ring 18.

18. A housing for an intrusion detector system as set forth in Claim 20 wherein the wall 58 of the lower housing 14 extends upwardly from a base 60, the base 60 having an inner surface from which a circular well wall 78 extends and from which a series of rib elements 82 extend, the rib elements 82 spaced from each other, radiating from the well wall 78 and having an upper surface, the printed circuit board 20 having a lower edge 21, the lower edge 21 bearing against the upper surface of the rib elements 82 and the printed circuit board 20 bearing against the well wall 78.

19. A housing for an intrusion detector system

as setforth in Claim 20 wherein the wall 58 of the lower housing 14 is formed of material adapted to allow passage of detectable radiation and the engagement means of the swivel ring 18 is a guide ring 107, the guide ring 107 being of a diameter equal to that of the adjustment ring 106, extending from the second surface 104 away from the adjustment ring 106 and in coaxial relation with the base ring 100.

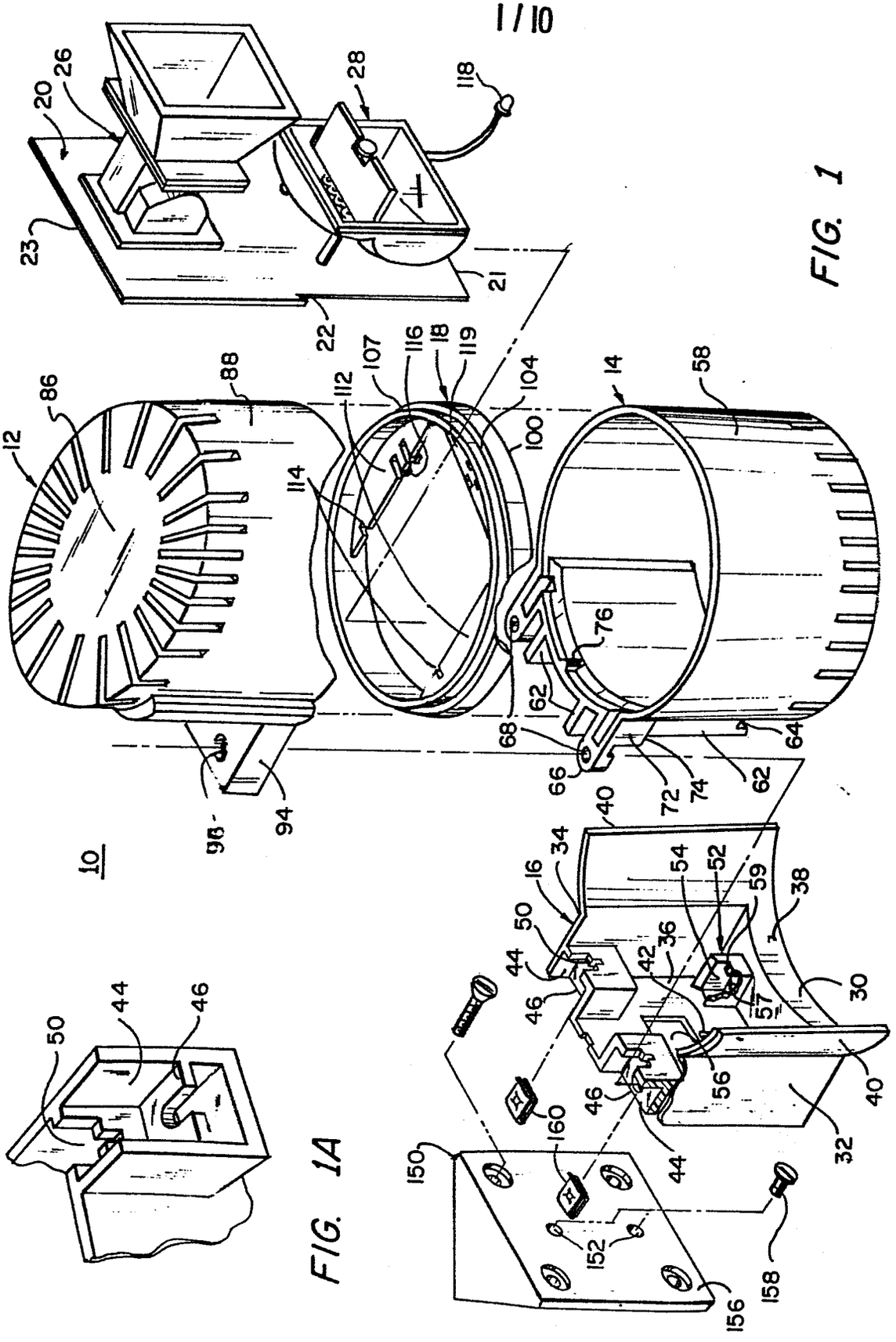
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FIG. 1

FIG. 1A

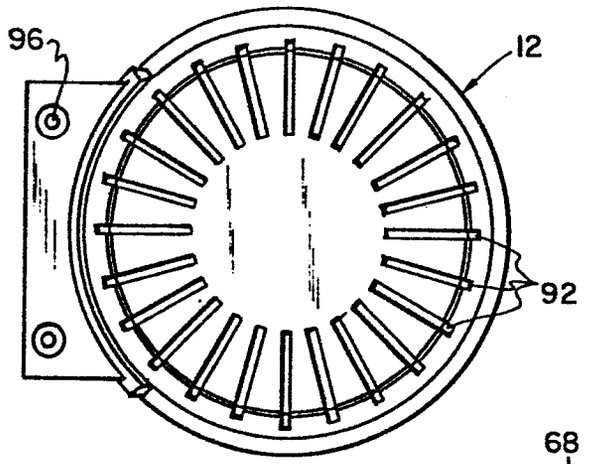

FIG. 2

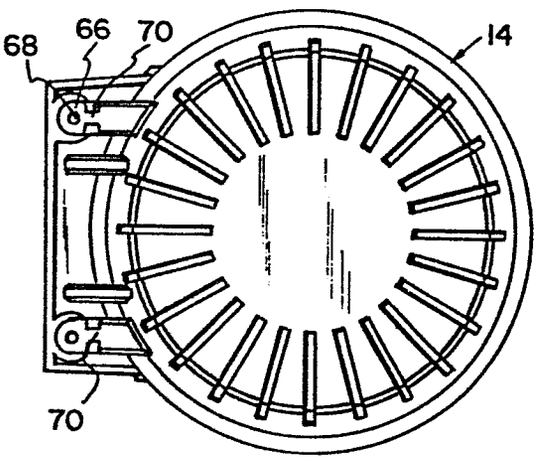

FIG. 3

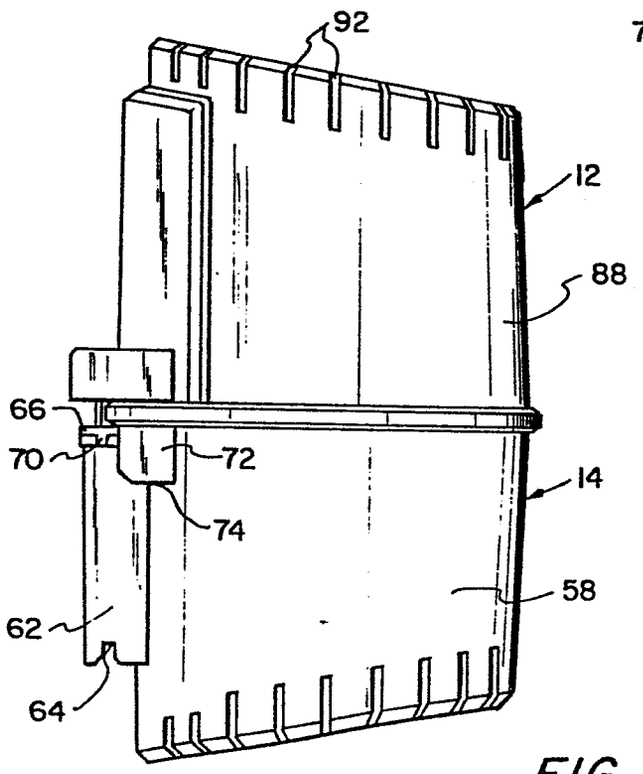

FIG. 4

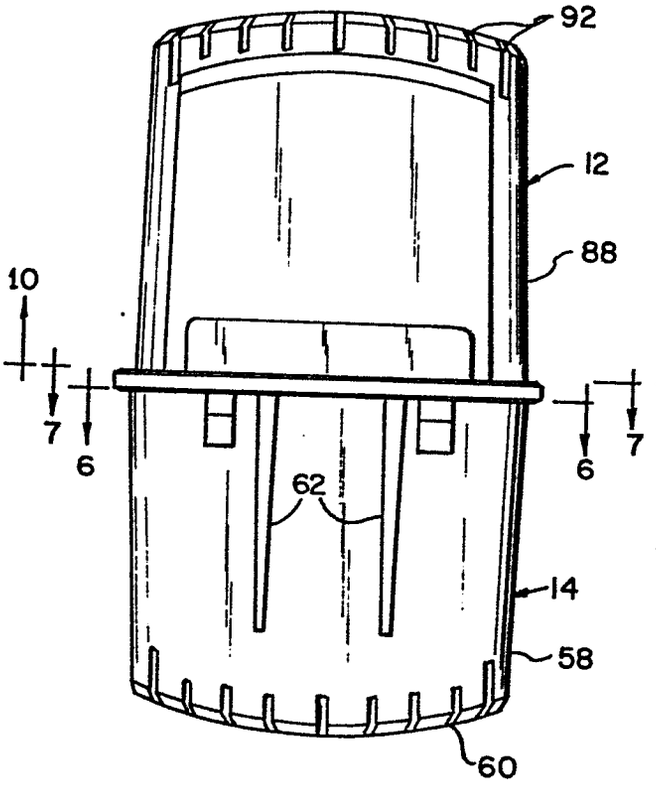

FIG. 5

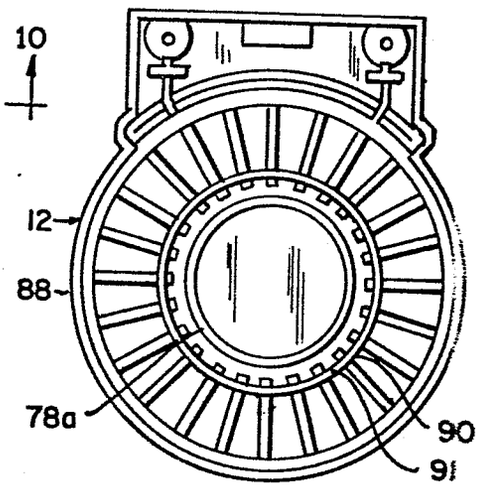

FIG. 10

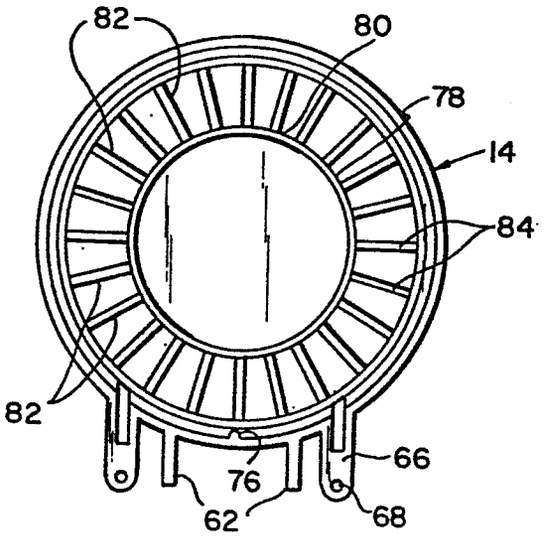

FIG. 6

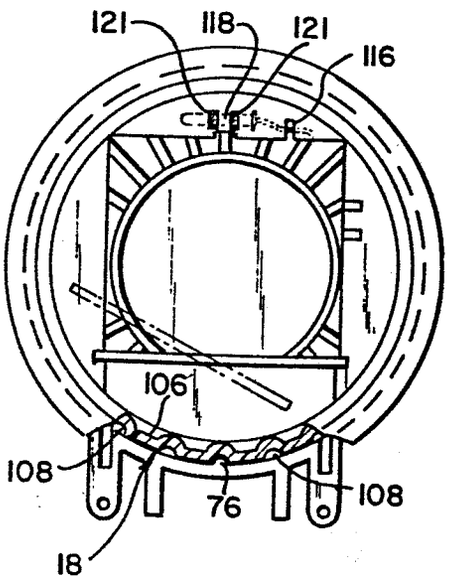

FIG. 7

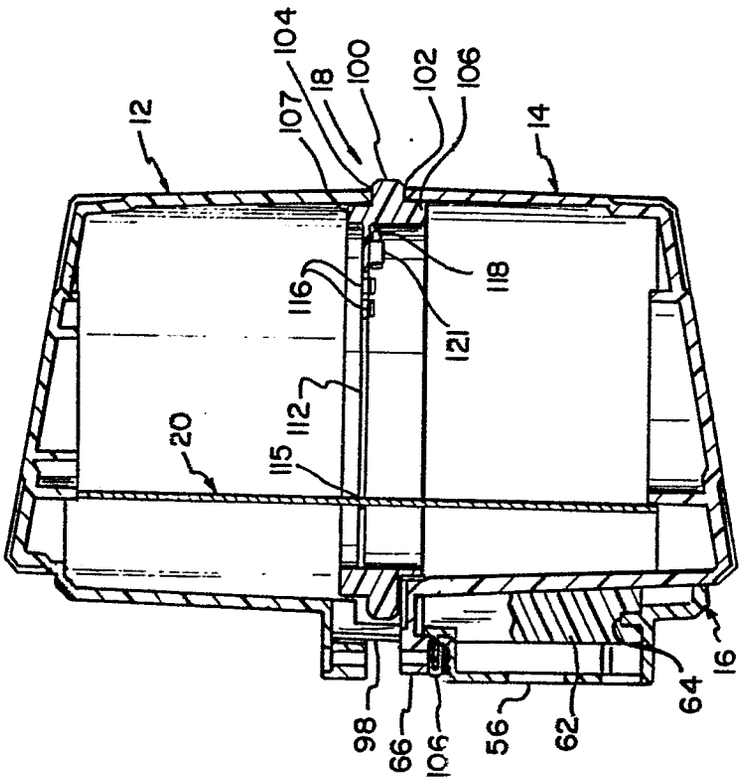
104
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FIG. 9

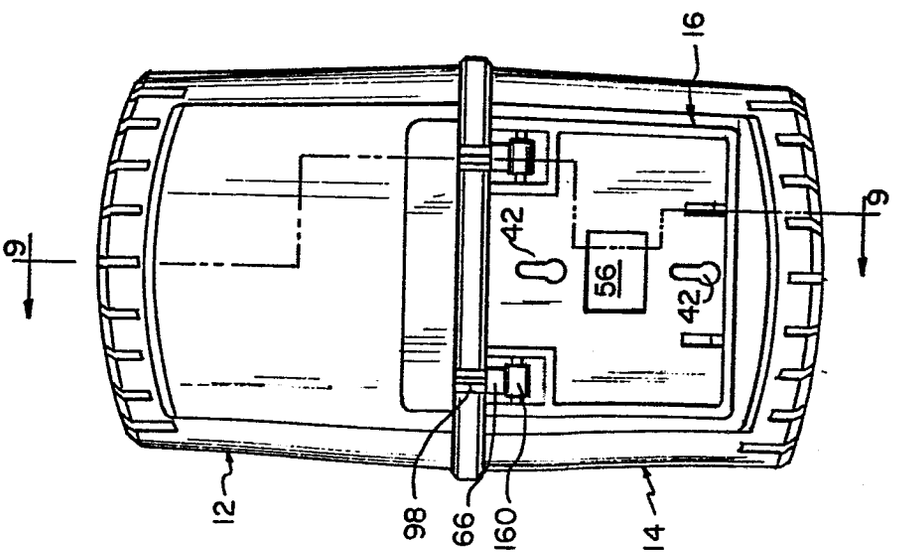
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FIG. 8

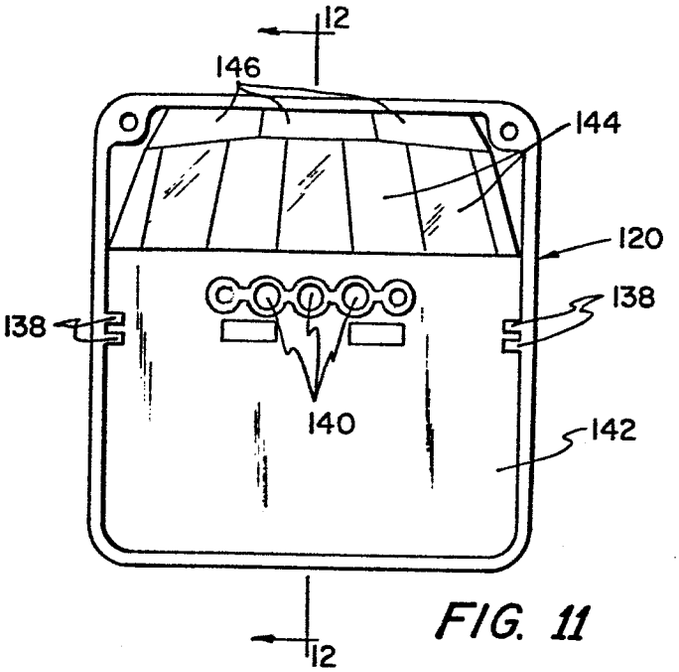

FIG. 11

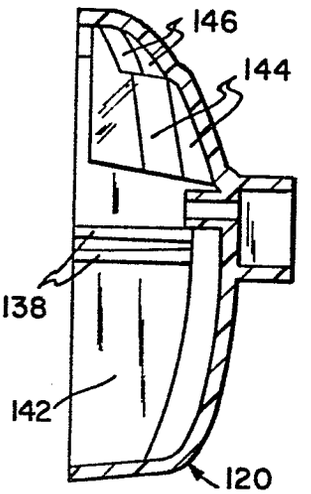

FIG. 12

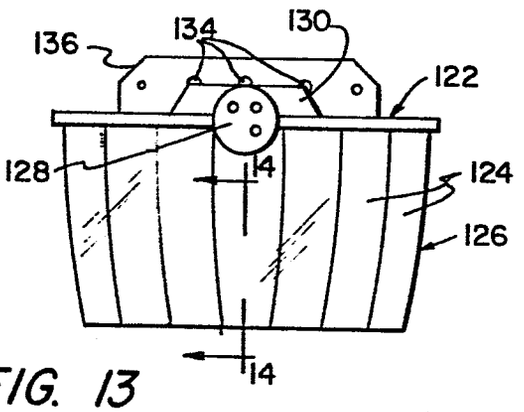

FIG. 13

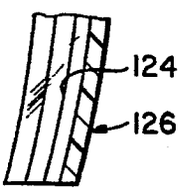

FIG. 14

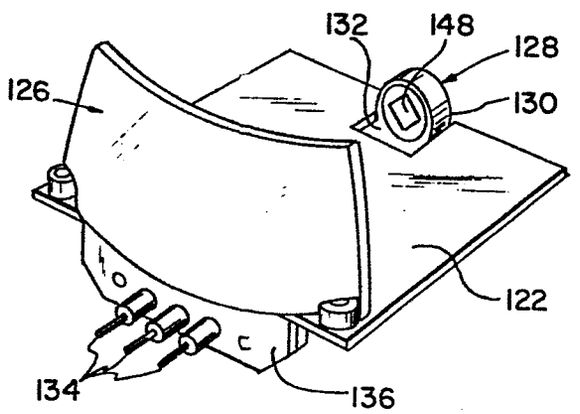

FIG. 15

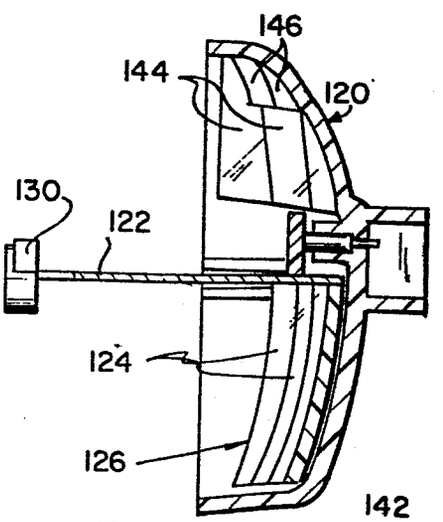

FIG. 16

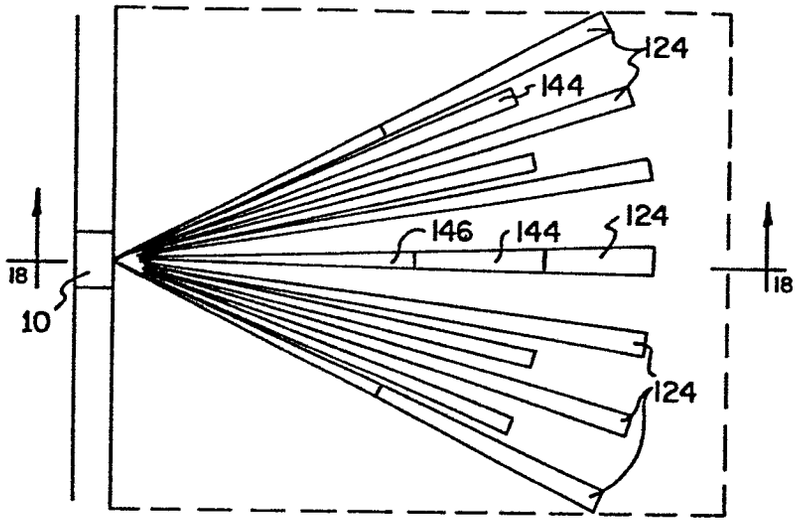

FIG. 17

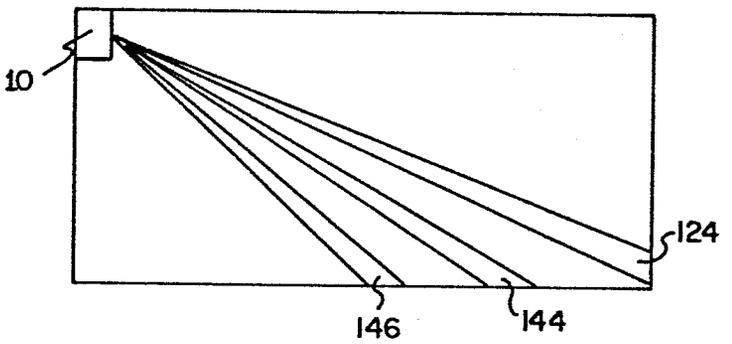

FIG. 18

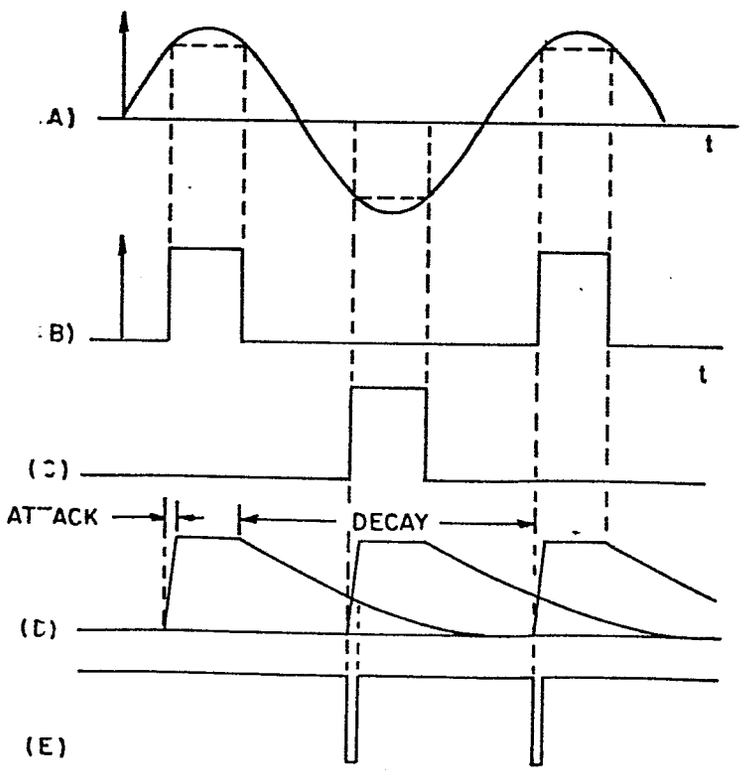

FIG. 19

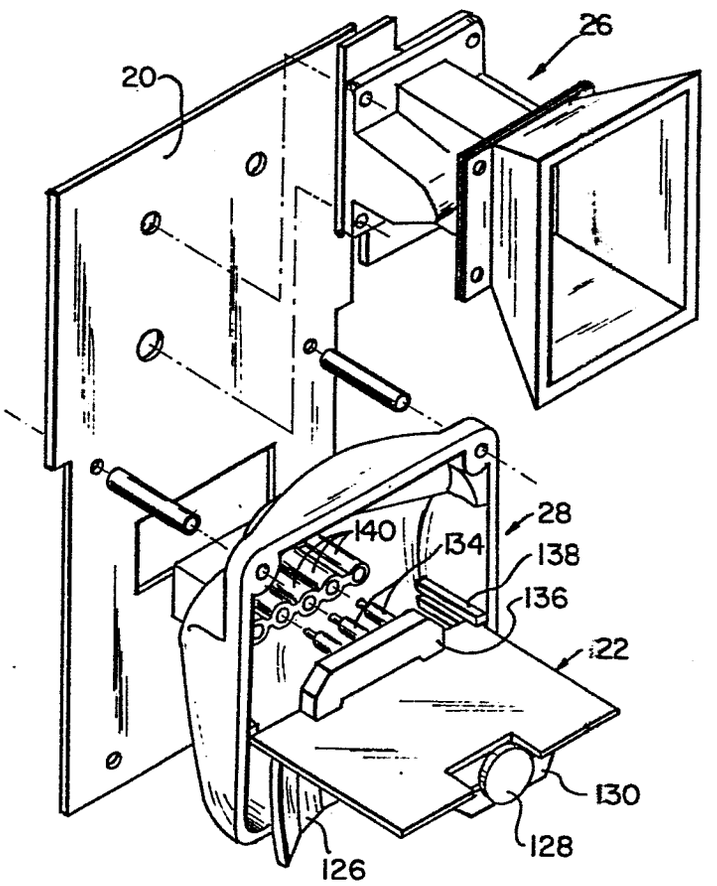

FIG. 20

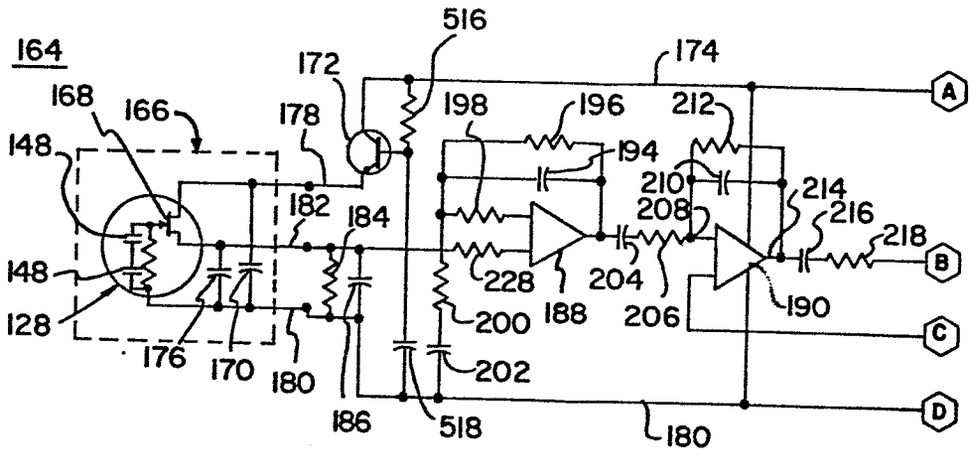
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FIG. 21

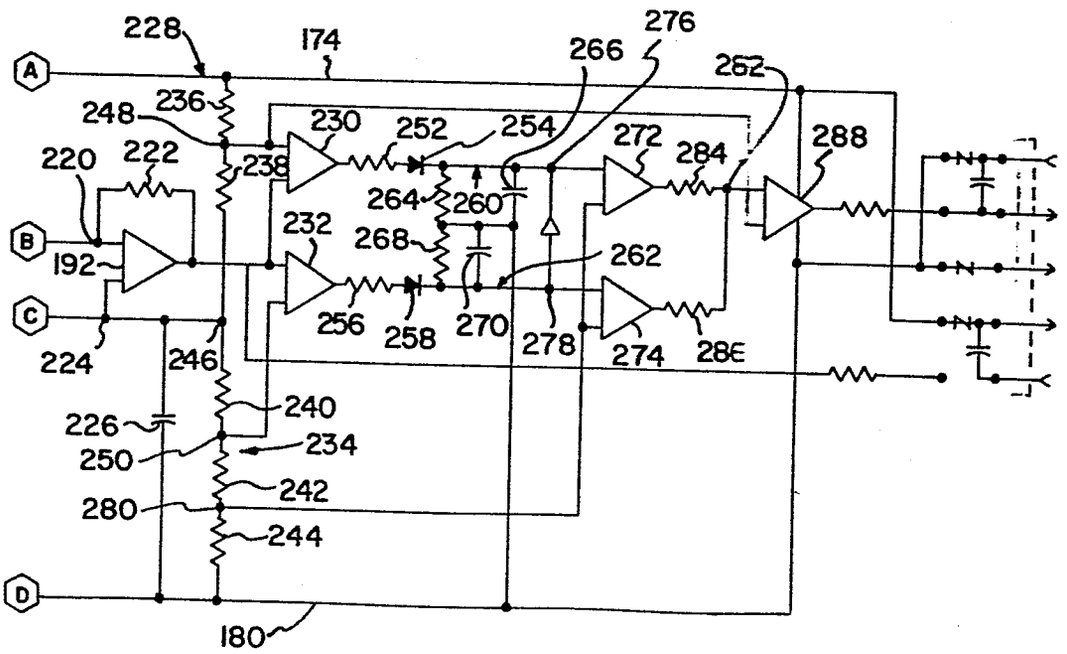
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FIG. 22

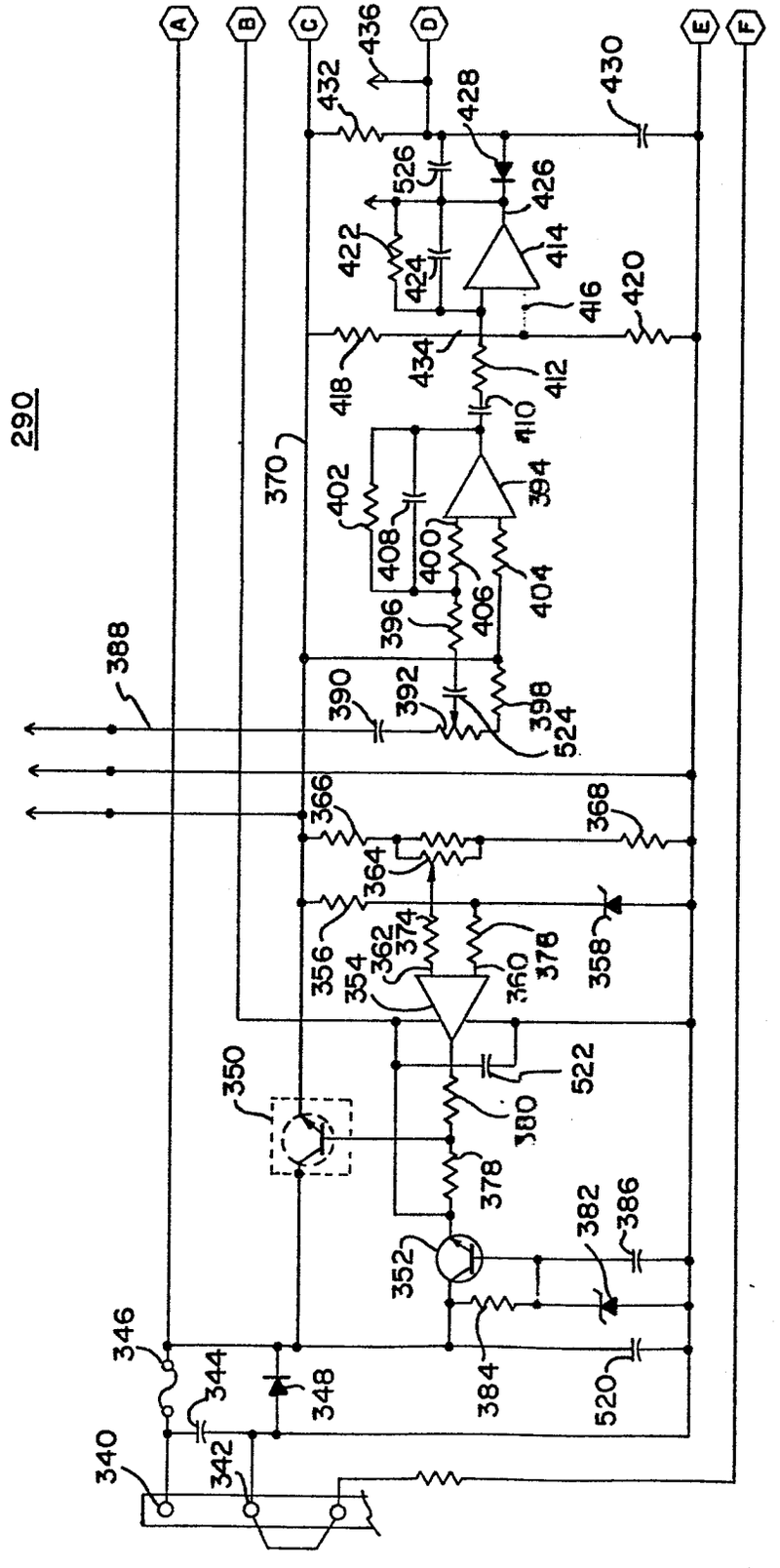
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FIG. 23

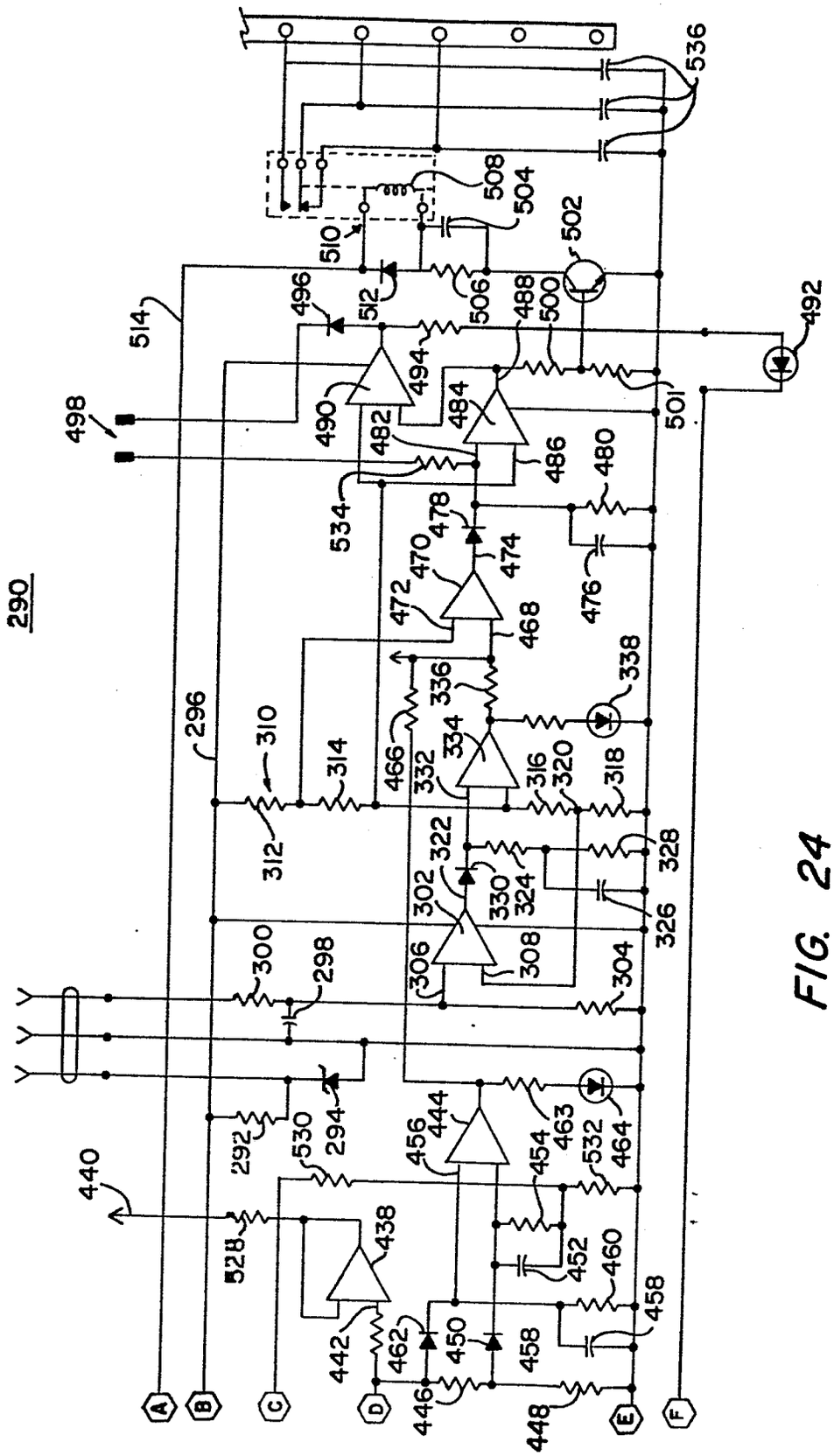

FIG. 24

European Patent Office

EUROPEAN SEARCH REPORT

0147925
Application number

EP 84 30 6871

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int Cl 4)
Y	US-A-4 258 255 (J.K. GUSCOTT) * Figure 1, claim 1 *	1	G 08 B 13/18
Y	EP-A-0 069 782 (TAKENAKA) * Figure 2, abstract *	1	
P,A	EP-A-0 103 375 (MONICELL) * Figure 4; abstract, claims 2,3 *	1	
A	US-A-4 364 030 (J.A. ROSSIN) * Figures 5,6; column 7, line 28 - column 8, line 54 *	2,7	
A	DE-A-2 656 318 (TELENOT WUNDERLE) * Claims 1,3 *	15	TECHNICAL FIELDS SEARCHED (Int. Cl 4)
A	US-A-3 725 888 (E.E. SOLOMON) * Figure 1, abstract *	16	G 08 B 13/18

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	14-01-1985	BREUSING J

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X : particularly relevant if taken alone
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