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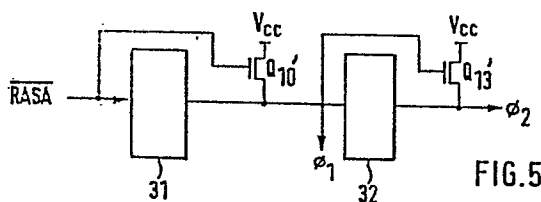
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(54) **Timing signal generator.**

(57) A timing signal generator which can operate stably even when, or directly after, a power supply is switched on. The generator is of the type having a first delay circuit (31) for generating a first timing signal (ϕ_1) in response to said input control signal and a second delay circuit (32) for generating a second timing signal (ϕ_2) in response to the first timing signal (ϕ_1), and is featured by a first transistor (Q_{10}) connected between the output of the first delay circuit (31) and a voltage terminal, with a gate connected to the input of the first delay circuit and a second transistor (Q_{13}), connected to the output of the second delay circuit (32) and the voltage terminal with a gate connected to receive the first timing signal (ϕ_1).





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EUROPEAN SEARCH REPORT

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 23, no. 2, July 1980, pages 723,724, IBM Corp., New York, US; P. EVRENIDIS et al.. "On-chip power-on-reset circuit" * Whole document *	1	H 03 K 5/15 H 03 K 17/22 G 11 C 8/00
A	GB-A-1 337 910 (ITT) * Figure; page 1, line 82 - page 2, line 24 *	1	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 21, no. 2, July 1978, pages 734-737, IBM Corp., New York, US; J. BULA et al.: "On-chip clock generator" * Whole document *	1	
A	PATENTS ABSTRACTS OF JAPAN, vol. 7, no. 129 (E-179)[1274], 4th June 1983; & JP - A - 58 43 622 (HITACHI SEISAKUSHO K.K.) 14-03-1983 * Figure; abstract *	1	H 03 K G 11 C G 06 F
The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int. Cl. 4)
Place of search THE HAGUE		Date of completion of the search 07-08-1986	Examiner DAVIS A.G.W.
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			



DOCUMENTS CONSIDERED TO BE RELEVANT			Page 2
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-13, no. 5, October 1978, pages 536-541, IEEE, New York, US; O. TOMISAWA et al.: "A 920 gate DSA MOS masterslice" * Figures 4,5; page 536, right-hand column, line 33 - page 537, left-hand column, line 25 *	1	
A	GB-A-2 091 008 (HITACHI) * Figures 4,5; page 2, lines 99-105 *		
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