(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 149 788**
A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **84115208.5**

(22) Date of filing: **12.12.84**

(51) Int. Cl.⁴: **G 09 G 1/16**

(30) Priority: **14.12.83 JP 234334/83**
26.12.83 JP 243677/83
26.12.83 JP 243678/83

(43) Date of publication of application:
31.07.85 Bulletin 85/31

(84) Designated Contracting States:
DE FR GB NL

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(54) Display control system.

(57) An improved display control system is disclosed which is capable of reducing the time necessary for executing its display operation. In this display control system, when a display memory (4) is to be accessed, its software supplies values of the X, Y coordinates of a display screen and these values are then converted into the physical addresses of the memory (4). For this purpose, a limit check function (33) is provided. Also, an X register (30) for setting up values on the X coordinate in a display unit (3A) may be formed by a counter, thereby eliminating the need for setting the values on the X coordinate each time.

The display control system may also be capable of dealing with the change of a plurality of screen configurations in the above-mentioned X, Y coordinate system.

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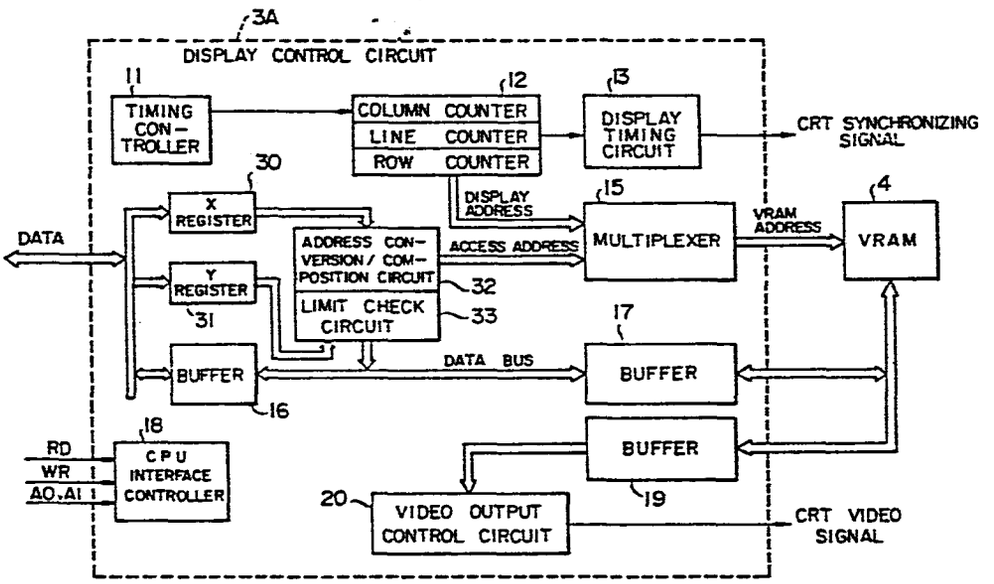
FIG. 4


3A
DISPLAY CONTROL CIRCUIT
11
TIMING CON-TROLLER
12
COLUMN COUNTER
LINE COUNTER
ROW COUNTER
13
DISPLAY TIMING CIRCUIT
CRT SYNCHRONIZING SIGNAL
30
X REGISTER
Y REGISTER
31
DISPLAY ADDRESS
15
MULTIPLEXER
VRAM ADDRESS
4
VRAM
DATA
ADDRESS CON-VERSION / COM-POSITION CIRCUIT
ACCESS ADDRESS
32
LIMIT CHECK CIRCUIT
33
17
BUFFER
DATA BUS
BUFFER
16
18
RD
WR
A0, A1
CPU INTERFACE CONTROLLER
BUFFER
19
20
VIDEO OUTPUT CONTROL CIRCUIT
CRT VIDEO SIGNAL

DISPLAY CONTROL SYSTEM

The present invention relates to a display control system e.g. for use in a computer.

Fig. 1 illustrates a block diagram of a conventional color graphics display system.

In this figure, there is provided a CPU(microprocessor) 1 for controlling the whole system, and a main memory 2 and a display control circuit 3 are respectively connected to CPU 1. Main memory 2 is used to hold programs and data, and Display Control Circuit 3 is dedicated to control the display of color graphics. Reference 4 designates a VRAM(video memory) for holding CRT display data, and 5 represents a CRT color display unit.

In Fig. 2, there is shown a block diagram of an example of the display control circuit 3 illustrated in Fig. 1.

A timing controller 11 is operated to generate a clock signal which is in turn input to a counter 12 having a column counter, a line counter and a row counter. This counter 12 generates a CRT display synchronizing signal via a display timing circuit 13, while this counter 12 creates a display

address which is output via a multiplexer 15 as a VRAM address.

The data that is read out from VRAM 4 for display access is inputted via a buffer 19 into a video output control circuit 20, where a CRT video signal is created.

On the other hand, in the case when CPU 1 tries to access VRAM 4, if an address of VRAM 4 is set in a VRAM address register 14 and a write strobe is input to a CPU interface controller 18, then the output of VRAM Address Register 14 due to CPU 1 is selected by a multiplexer 15 as the VRAM address, and the write data from CPU 1 is written via buffers 16, 17 into VRAM 4.

Fig. 3 illustrates an example of the above-mentioned VRAM 4, the screen configuration of which comprises 640 horizontal dots, 200 vertical dots, and 4-bit (16-color) color information.

Let us take a conventional example of operation where the block data of a source area within VRAM 4 is transferred to a destination area based on the X, Y coordinates as shown in Fig. 3.

CPU 1 calculates the physical address of VRAM 4 based on the source area coordinates (Sx, Sy) and sets the calculated physical address in VRAM Address Register 14 within Display Control Circuit 3. Also, CPU 1 outputs a read command to

read out the color data within VRAM 4 that corresponds to the coordinates (Sx, Sy).

Next, CPU 1 calculates the physical address in VRAM 4 based on the coordinates (Dx, Dy) of the destination area to which the block data is to be transferred, and sets the calculated physical address in VRAM Address Register 14 within Display Control Circuit 3. Also, CPU 1 writes the color data corresponding to the coordinates (Sx, Sy) into VRAM 4, that is, the locations thereof that correspond to the coordinates (Dx, Dy).

Then, it is necessary to repeat the above-mentioned read/write operations NX times regarding the horizontal direction and NY times regarding the vertical direction, or a total of (NX X NY) times before the block data of the source area can be transferred to the destination area.

In order to satisfy the needs of small size and low cost of a personal computer, the conventional display control system for use in the personal computer is designed such that its hardware is reduced in amount. As a result of this, its software must take heavy loads to make up for the reduction of the hardware amount.

As can be seen from the example of the transfer of the block data mentioned above, CPU 1 must perform all of the

processing operations and thus it takes a lot of time to transfer such block data in the prior art system.

Also, in the above-mentioned conventional system, normally, CPU 1 and Display Control Circuit 3 are operating independently of each other and the display timing of Display Control Circuit 3 has priority over the VRAM access timing of CPU 1. As a result of this, a wait time arises when CPU 1 accesses VRAM 4, which extremely decreases the efficiency of the data transfer.

In other words, in the above-mentioned prior art system, since the software must take greater processes in the display control, there is a problem that it takes a very long time to execute its operations. Also, as the computer is graded up with its display specifications increased, the time necessary for its operation execution becomes outstandingly longer.

On the other hand, in the above-mentioned prior art system, when the software is used to calculate the physical address of VRAM 4, if the values of the physical address on the X, Y coordinates are not contained in the display screen, then a proper conversion into the physical address is not performed. Therefore, it is necessary by all means to carry out a check (which is referred to as a limit check) whether the values on the X, Y coordinates exist within the limit of

the display screen, before the physical address is calculated. This limit check increases the loads of the software considerably, and, in this sense, the time required for execution of the operations becomes also long. In particular, when drawing a circle, such limit check must be performed quite frequently so that the operation execution time becomes longer.

The present invention aims at eliminating the problems seen in the above-mentioned conventional system.

Accordingly, it is an object of the invention to provide an improved display control system for a computer which can reduce the execution time of its display operations.

In accomplishing the above object, according to the invention, when accessing a display memory, software gives the values on the X, Y coordinates on a display screen and these values are converted to the physical address of the memory. There are also provided a limit check function and means for operating on the values on the X, Y coordinates step-by-step for each access to the display memory.

The above and other related objects and features of the invention will be apparent from a reading of the following description of the disclosure with reference to the accompanying

drawings in which:

Fig. 1 is a block diagram of a typical conventional color display system;

Fig. 2 is a block diagram of a display control circuit employed in Fig. 1;

Fig. 3 is a block diagram of a VRAM in Fig. 1, illustrating the transfer operation of a block data;

Fig. 4 is a block diagram of an embodiment of the invention;

Fig. 5 is a view to explain the operation of an address conversion/composition circuit employed in the above-mentioned embodiment of the invention;

Fig. 6 is a block diagram of a limit check circuit in the above embodiment;

Fig. 7 is a view to illustrate an example of a comparison circuit contained the above-mentioned limit check circuit;

Fig. 8 is a block diagram of another embodiment of the invention;

Fig. 9 is a view to illustrate the operation of an address conversion/composition circuit employed in the embodiment in Fig. 8;

Fig. 10 is a view to illustrate an X counter employed in the above-mentioned embodiments of the invention;

Fig. 11 is a schematic view of a decoder circuit for distributing the respective read/write signals from CPU to registers;

Fig. 12 is a block diagram of still another embodiment of the invention;

Figs. 13 and 14 are schematic views respectively showing an address conversion/composition circuit that corresponds to a plurality of screen resolutions or configurations; and,

Fig. 15 is a view to illustrate a mode register and a count signal generation circuit.

In Fig. 4, there is illustrated a block diagram of an embodiment of the invention. This embodiment is different from the conventional system shown in Fig. 2 in that an X register 30, a Y register 31 and an address conversion/composition circuit 32 are provided instead of the VRAM address register 14 in Fig. 2, and that a limit check circuit 33 is provided. Limit Check Circuit 33 is a circuit that checks whether the values of the coordinates to be accessed exist

or not on a display screen. The illustrated display control circuit 3A otherwise corresponds to the display control circuit 3 in Fig. 2.

When CPU 1 tries to access VRAM 4, a value of the X coordinate corresponding to its screen position on the VRAM 4 is set in X Register 30 and an associated value of the Y coordinate is set in Y Register.

Address Conversion/Composition Circuit 32 inputs the value set in X Register 30 and the value set in Y Register 31 to convert or compose these values into the physical address of VRAM 4, and always supplies the thus-converted or composed physical address as an access address to Multiplexer 15.

Accordingly, after setting of the values on the X, Y coordinates, CPU 1 can access color information via a data bus by giving a write strobe or a read strobe to CPU Interface Controller 18.

X Register 30 and Y Register 31 may each comprise an ordinary register.

Address Conversion/Composition Circuit 32 may be realized by use of a simple adder or by means of rearrangement of bits of X Register 30 and Y Register 31. Some examples of the address conversion/composition circuit 32 are shown in Fig. 5.

Fig. 5 illustrates the operation of an adder when the

adder is employed as the address conversion/composition circuit 32.

First, Fig. 5(a) illustrates how an address created by a value in X Register 30 and a value in Y Register 31 is converted into a physical address for VRAM 4 in case of a screen configuration comprising 640 x 200 dots as shown in Fig. 3. In other words, a value contained in the bit array of X Register 30, a value in the bit array of Y Register 31 shifted by 7 bits from X Register 30, and a value in the bit array of Y Register 31 shifted by 2 bits shifted from the above Y Register 31 are added. Addition of these three values permits execution of 640 X Y + X based on the values of X Register 30 and Y Register 31 (that is, these values can be converted into the physical address of VRAM 4).

Next, Figs. 5(b) and (c) respectively illustrate cases in which the number of dots in the X axis direction comprises the power value of 2. In these cases, in order to convert the address created by the value of X Register 30 and the value of Y Register 31 to the physical address of VRAM 4, Y Register 31 needs only be connected as a higher bit of X Register 30.

That is, Fig. 5(b) illustrates a case wherein the screen is composed of 512 x 200 dots and thus Y Register 31 need

only be connected to the higher position of the 8 bit of X Register to provide for conversion into the physical address. Also, Fig. 5(c) shows a case in which the screen has a configuration of 256 x 200 dots and thus the bit array of Y Register 31 need only be connected to the higher position of the lower 7 bit of X Register 30 to provide for conversion into the physical address.

When the transfer of the block data shown in Fig. 3 is executed, the information that occurs first is values on the X, Y coordinates. Therefore, if it is possible to specify such values on the X, Y coordinates as they are, to hardware, then CPU 1 can save all of processings necessary to calculate the physical address.

In other cases than that shown in Fig. 3 as well, if the system which is using the display screen has a higher level language as its original language, then when the screen is accessed, the first occurring information, most of all, is positions on the screen. In particular, the positions on the screen are expressed as values on the X, Y coordinates.

Therefore, even in an ordinary case, it is possible to lighten the loads of its software to a great extent, if it happens to be a case in which these X, Y coordinates can be used to provide access to a display memory.

Now, Fig. 6 illustrates a block diagram of an example of Limit Check Circuit 33, and Fig. 7 illustrates comparison circuits included in this limit check circuit 33.

When CPU 1 is going to access VRAM 4, if coordinate values are set in X Register 30 and Y Register 31 respectively, then Limit Check Circuit 33, together with Address Conversion/Composition Circuit 32, is operated. That is, Comparison Circuits 40 and 41 are operated to check whether the respective values on the X, Y coordinates are in excess of maximum values or not. If either of them exceeds the maximum value, then an interrupt signal is generated. In this way, by interrupting CPU 1, it is possible to inform to the effect that the coordinates to be accessed do not exist in the associated display screen.

Also, Comparison Circuits 40 and 41 may be connected to a data bus by means of a gate circuit 42 such that their output conditions can be written in the form of a status indication, so that it is possible to know which of the coordinate values is in excess of the maximum value.

Even in case when CPU 1 is operated in a condition in which it cannot or does not initiate an interrupt, if, after setting of the X, Y coordinates, such status is always examined, then it is possible to judge which of the comparison

circuits 40, 41 exceeds the maximum value.

Fig. 7(a) illustrates an example of a comparison circuit for checking whether the value of X Register 30 is in excess of 640 or not.

When the bits 9 - 7 of X Register 30 are equal to or more than "101", NL (NOT LESS) signal is output from Comparison Circuit 40. This NL signal and a value in the bits 15 - 10 of X Register 30 is ORed to create an X Limit Out signal having the meaning that the associated value has exceeded the maximum value on the X coordinate.

The value on the X coordinate is stored in terms of 2 bytes (16 bits) of software. The respective values of the X coordinate should have been determined in accordance with the respective demand items of the system previously occurred, and if the value is other than "0 - Max. value", then its position on the coordinates exists outside the screen and thus any access to it must be prohibited. Since the value of the coordinates is operated in terms of a binary number sufficiently greater than its maximum value, when it is out of position in either of a positive or negative direction, it becomes a value other than "0 - Max. value". Here, the bit 15 is interpreted as a sign.

Fig. 7(b) illustrates an example of a comparison circuit for checking whether a value on the Y coordinate is in

excess of 200 or not. If the value is more than 200, then a Y Limit Out signal is output.

Fig. 7(c) illustrates a check circuit for checking whether a value on the X coordinate is in excess of 512 or not. If its screen is structured such that its limit value is composed of a power value of 2 in this manner, then Check Circuit 33 can be realized very simply.

Fig. 8 illustrates a block diagram of another embodiment of the invention. This embodiment is substantially similar to the prior embodiment in Fig. 4, but a display control circuit 3B in Fig. 8 is different from the display control circuit 3A in Fig. 4 in that an X counter 30c is employed in place of the X register 30. The discussion made in connection with the embodiment in Fig. 4 may also apply to the embodiment in Fig. 8, with X Register 30 being replaced by X Counter 30c.

Fig. 9 illustrates the operation of an adder when the adder is used as Adress Conversion/Composition Circuit 32. Similarly, the description given in connection with Fig. 5 can also apply to Fig. 9, only with X Register 30 replaced by X Counter 30c.

Fig. 10 illustrates X Counter 30c, and Fig. 11 illustrates a decoder circuit for distributing the respective read/write signals from CPU 1 to registers.

X Counter 30c is used as means to set up a value on the X coordinate, and as a load signal to X Counter 30c an indication signal is used which is employed by CPU 1 to set up the value on the X coordinate. As a count-up signal, a signal is used which indicates that CPU 1 has accessed VRAM 4.

Each of the signals is outputted from Decoder 18d. Decoder 18d is included within CPU Interface Controller 18 and is operated when CPU 1 reads/writes data between the respective registers.

X Counter 30c may be counted up by use of the trailing edge of the count signal.

Y Register 31 may also be composed of a counter. In this case, its count-up signal may be supplied from CPU 1 or it may occur automatically within Display Control Circuit 3. This automatic occurrence may include such an operation as to count up by 1 a value on the Y coordinate when X Counter 30c counts N times. Thus, such automatic operation can improve the performance of the system. Alternatively, it may be possible not only to count up the value on the Y coordinate but also to specify its count-down.

Fig. 12 illustrates a block diagram of another embodiment of the invention.

This embodiment is different from the above-mentioned

embodiment in Fig. 8 in that it is further provided with a mode register 34. The thus-modified display control circuit is designated by 3C in this Figure.

At an initialization time or the like, prior to access to VRAM 4, CPU 1 sets up a value to specify a screen configuration to Mode Register 34. Based on this value, Column Counter/Line Counter/Row Counter 12 performs its counting operation and at the same time outputs a signal and a display address to Display Timing Circuit 13.

In Fig. 3 the value of the X coordinate ranges up to 639 and thus it can display 640 dots, while this horizontal display dot number can be changed. The change of the number is referred to as change of the screen configuration.

Further, since it is also necessary to change the contents of Address Conversion/Composition Circuit 32 correspondingly to the change of the respective screen configurations, the contents of Mode Register 34 are inputted to Address Conversion/Composition Circuit 32 as well. Address Conversion/Composition Circuit 32 is composed of two selectors 321, 322 and an adder 323 as shown in Fig. 13.

In this embodiment, three kinds of screen configurations (or M0, M1, M2) are employed and, therefore, the following correspondences are necessary:

For M0, 640 X Y + X

For M1, 512 X Y + X

For M2, 256 X Y + X

These equations can be generalized by the following equations:

$$X + Y \times 256 \times S1 + 128 \times S2$$

where, S1 is 1 for M2 and 2 for M1, M0, while S2 is 1 for M0 and 0 for M1 and M2.

Selector 1(321) shown in Fig. 13 has shifted the values of Y Register by one bit for M0,M1, thereby realizing the conditions of S1. Selector 2 (322) selects 0 for M1,M2 and thus realizes the conditions of S2.

When the number of horizontal dots in the screen configuration is a power number of 2 only, for example, when it is only M1, M2, the circuit shown in Fig. 10 may be used to compose the bits (that is, re-arrange them) only, which eliminates the need for Adder 323.

Next, we will describe the specification function of such an X counter as shown in Fig. 15 for specifying count modes in addition to the specification of the screen configuration.

In Fig. 15, there are provided a mode register 34 used to perform such mode specification and a circuit 18d responsive to the mode register 34 to generate count signals.

When we take account of the operation of an X counter that corresponds to the operation of software, in case of a read/modify/write operation, it may be convenient to count up only for the write operations. However, when a continuous reading or a continuous writing is carried out, it is convenient to count up for not only the write operations but alos the read operations. Also, it would be more convenient to be able to specify a count-down operation according to the direction of processings on the screen, which can improve the performance of a display control system.

Recently, with progress in the semi-conductor technology, even a relatively complicated circuit has been made in the form of an LSI, a gate array or the like which can reduce its effect to the cost of the finished product. Thus, situations permitting addition of hardware have been under arrangement.

In the above-mentioned description, various controlling operations not directly concerned with the present invention can be realized by the techniques well known in the art. For example, the timing of the display control circuits 3A, 3B, and 3C and the setting of the registers are to be performed by Timing Controller 11 and CPU Interface Controller 18.

Also, in the above-mentioned embodiment, although the principles of the invention have been described by way of

the memory so contructed as to have 4 bits for 1 memory address (= 1 dot, each display color information is composed of 16 colors), as shown in Fig. 3, it should be understood that they are not limited to the illustrated example but other embodiments can also be included within the scope of the invention. For example, the invention is adaptable to a configuration that employs 8 bits for 1 memory address (= 2 dots,each display color information of 16 colors, or, 4 dots, each display color information of 4 colors) in accordance with the contruction of a memory element, the access time of the memory, the adjustability relative to CPU 1 and the like. Further, the invention is able to cope with a configuration employing 16 bits for 1 memory address by specifying the modification portions of a word by means of the lower bits of X Counter 30c and using the higher bits of X Counter 30c as address values.

As can be seen from the foregoing description, according to the invention, most of the operations of the software relating to the display operations can be processed by the hardware. Accordingly, the invention is advantageous in that it is able to speed up its display memory access and that, in doing so, the amount of the hardware added is comparatively small.

Also, the present invention eliminates the need to set up values on the X coordinate every time, when the X, Y coordinate system is employed.

Claims:

1. A display control system comprising:

means (30) for setting up values of the X coordinate in a display unit (5);

means (31) for setting up values of the Y coordinate in said display unit (5); and

means (32) for converting or composing said set-up values of said X, Y coordinates into the physical addresses of a display memory (4),

characterised in that memory access data for reading, modifying or writing into the contents of said display memory (4) is specified for said X, Y coordinates.

2. A display control system comprising:

means (30) for setting up values of the X coordinate in a display unit (5);

means (31) for setting up values of the Y coordinate in said display unit (5); and

means (32) for converting or composing said set-up values on said X, Y coordinates into the physical addresses of a display memory (4);

characterised in that X coordinate comparison means (40) is provided for comparing said values on said X coordinate with a maximum value on said X coordinate that is determined according to the screen configuration of said display unit (5); in that Y coordinate comparison means (41) is provided for comparing said values on said Y coordinate with a maximum value on said Y coordinate that is determined according to the screen configuration of said display unit (5); in that means is provided for informing a CPU (1) of the results compared by said X and Y coordinate comparison means (33); in that memory access data for reading, modifying or writing the contents of said display memory (4) is specified for said

X, Y coordinates respectively, and in that said CPU (1) is informed if the X, Y coordinates to be accessed are present outside the limit of said screen (5).

3. A display control system as claimed in claim 2, characterised in that said informing means is constructed (42) such that said CPU (1) is able to read the outputs of said X, Y coordinate comparison means as a status indication.

4. A display control system as claimed in claim 2 or 3 characterised in that said informing means is adapted to interrupt said CPU when it judges that at least one of said X, Y coordinate comparison means is greater than said maximum value.

5. A display control system comprising:

means (30) for setting up values on the X coordinate in a display unit (5);

means (31) for setting up values on the Y coordinate in said display unit (5); and

means (32) for converting or composing said set-up values on said X, Y coordinates into the physical addresses of a display memory;

characterised in that step-by-step means is provided for advancing said values of said X coordinate step by step for each access to said display memory (4), in that memory accesses for reading, modifying or writing the contents of said display memory (4) are specified on said X, Y coordinates, and that for access operations for the X coordinate direction the need for resetting said values on said X coordinate is eliminated.

6. A display control system comprising:

means (30) for setting up values on the X coordinate in a display unit (5);

means (31) for setting up values on the Y coordinate in said display unit (5); and

means (32) for converting or composing said set-up values on said X, Y coordinates into the physical addresses of a display memory;

characterised in that means (34) are provided for setting up a plurality of screen configurations and specifying one of said screen configurations; in that means (30c,31) is provided for changing the contents of said conversion or composition means (32) in accordance with said specified screen configuration; in that memory accesses for reading, modifying or writing the contents of said display memory (4) are specified on said X, Y coordinates, and that a plurality of screen configurations are available.

7. A display control system comprising:

means (30) for setting up values on the X coordinate in a display unit (5);

means (31) for setting up values on the Y coordinate in said display unit (5); and

means (32) for converting or composing said set-up values on said X, Y coordinates into the physical addresses of a display memory 4;

characterised in that step-by-step means is provided for advancing said values of said X coordinate for each access to said display memory (4); in that means (34) is provided for specifying count modes; means (30c) is provided which is responsive to said memory access based on said specification for generating a pulse signal for count-up or count-down; in that memory accesses for reading, modifying or writing the contents of said display memory (4) are specified on said X, Y coordinates, and in that various count modes can be realized corresponding to said memory accesses.

FIG. 1

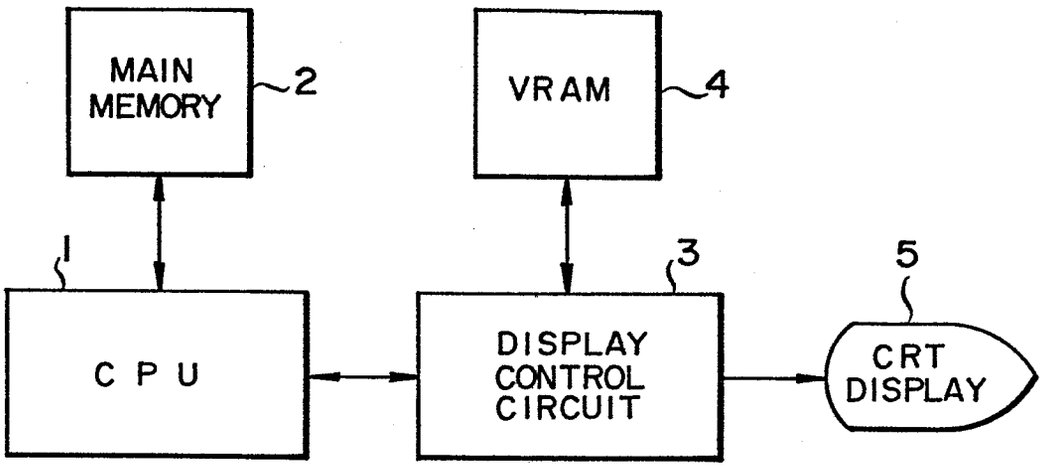

MAIN MEMORY
2
VRAM
4
1
3
5
C P U
DISPLAY CONTROL CIRCUIT
CRT DISPLAY

FIG. 3

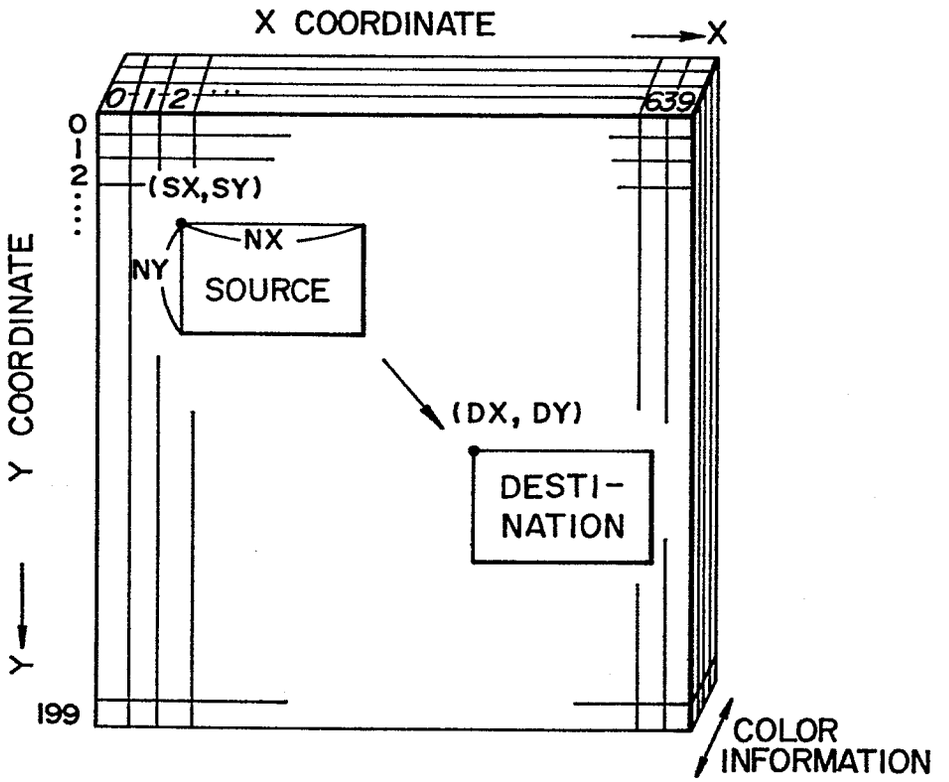

X COORDINATE
X
0 1 2 ... 639
0
1
2
....
199
Y
Y COORDINATE
(SX,SY)
NX
NY
SOURCE
(DX, DY)
DESTI-
NATION
COLOR INFORMATION

FIG. 2

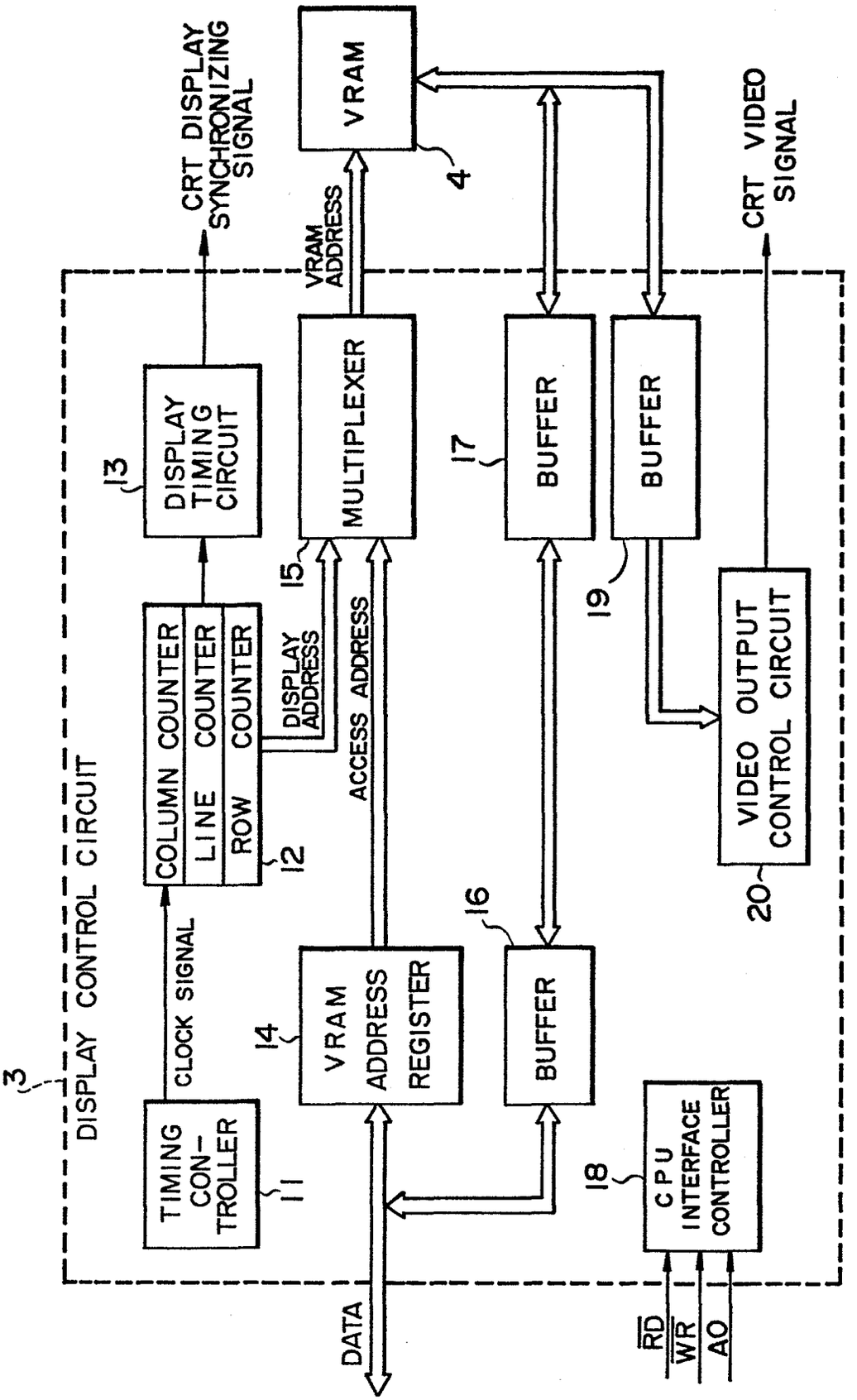

3
DISPLAY CONTROL CIRCUIT
TIMING CON-TROLLER
11
CLOCK SIGNAL
COLUMN COUNTER
LINE COUNTER
ROW COUNTER
12
DISPLAY ADDRESS
13
DISPLAY TIMING CIRCUIT
CRT DISPLAY SYNCHRONIZING SIGNAL
VRAM
4
VRAM ADDRESS
MULTIPLEXER
15
ACCESS ADDRESS
14
VRAM ADDRESS REGISTER
16
BUFFER
17
BUFFER
BUFFER
19
CRT VIDEO SIGNAL
VIDEO OUTPUT CONTROL CIRCUIT
20
18
CPU INTERFACE CONTROLLER
DATA
RD
WR
AO

FIG. 4

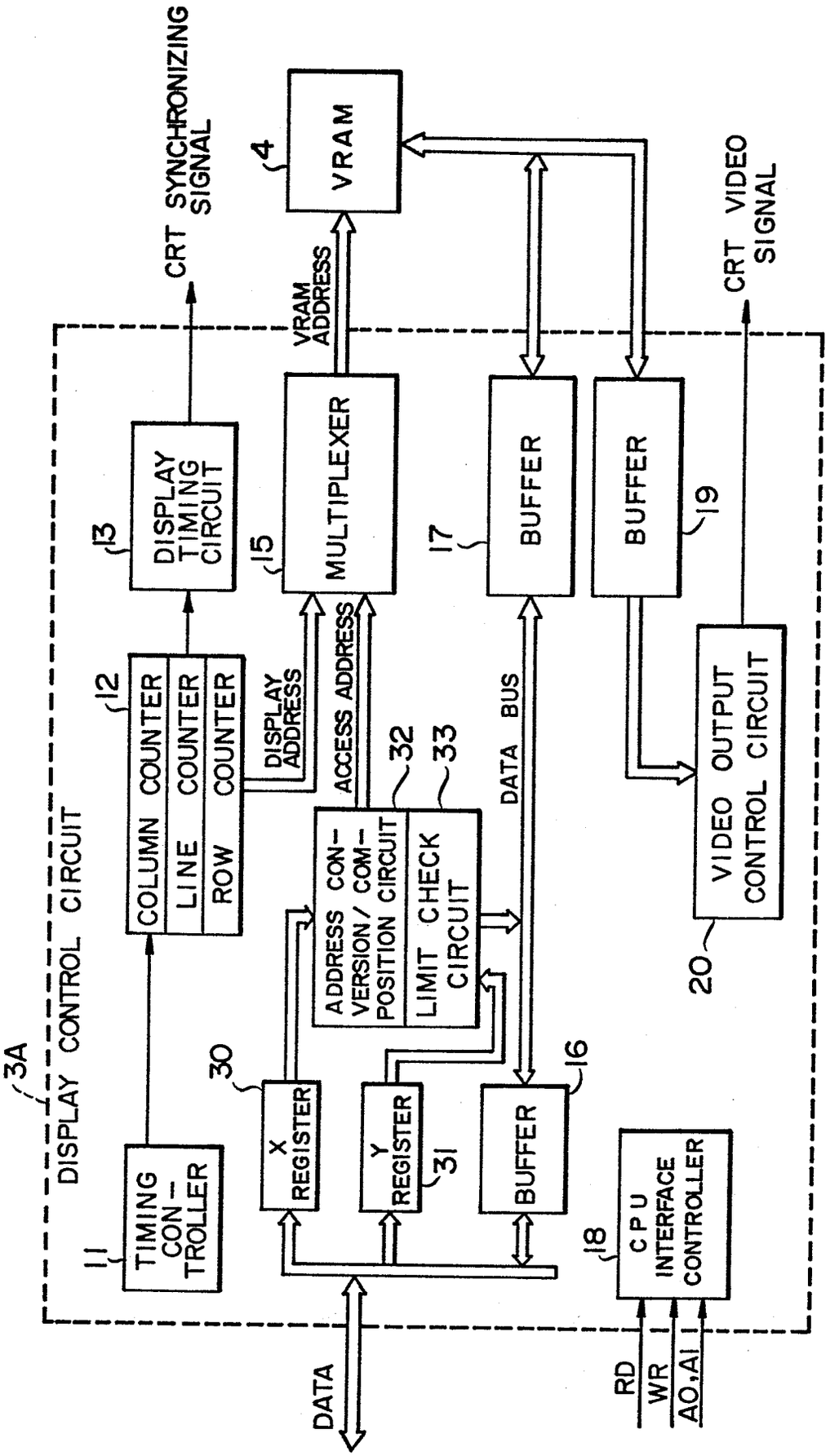

3A
DISPLAY CONTROL CIRCUIT
TIMING CON-TROLLER
11
COLUMN COUNTER
LINE COUNTER
ROW COUNTER
12
DISPLAY TIMING CIRCUIT
13
CRT SYNCHRONIZING SIGNAL
MULTIPLEXER
15
VRAM
4
VRAM ADDRESS
BUFFER
17
BUFFER
19
CRT VIDEO SIGNAL
VIDEO OUTPUT CONTROL CIRCUIT
20
DISPLAY ADDRESS
ACCESS ADDRESS
32
33
ADDRESS CON-VERSION/ COM-POSITION CIRCUIT
LIMIT CHECK CIRCUIT
DATA BUS
30
X REGISTER
Y REGISTER
31
BUFFER
16
CPU INTERFACE CONTROLLER
18
DATA
RD
WR
A0,A1

FIG. 5

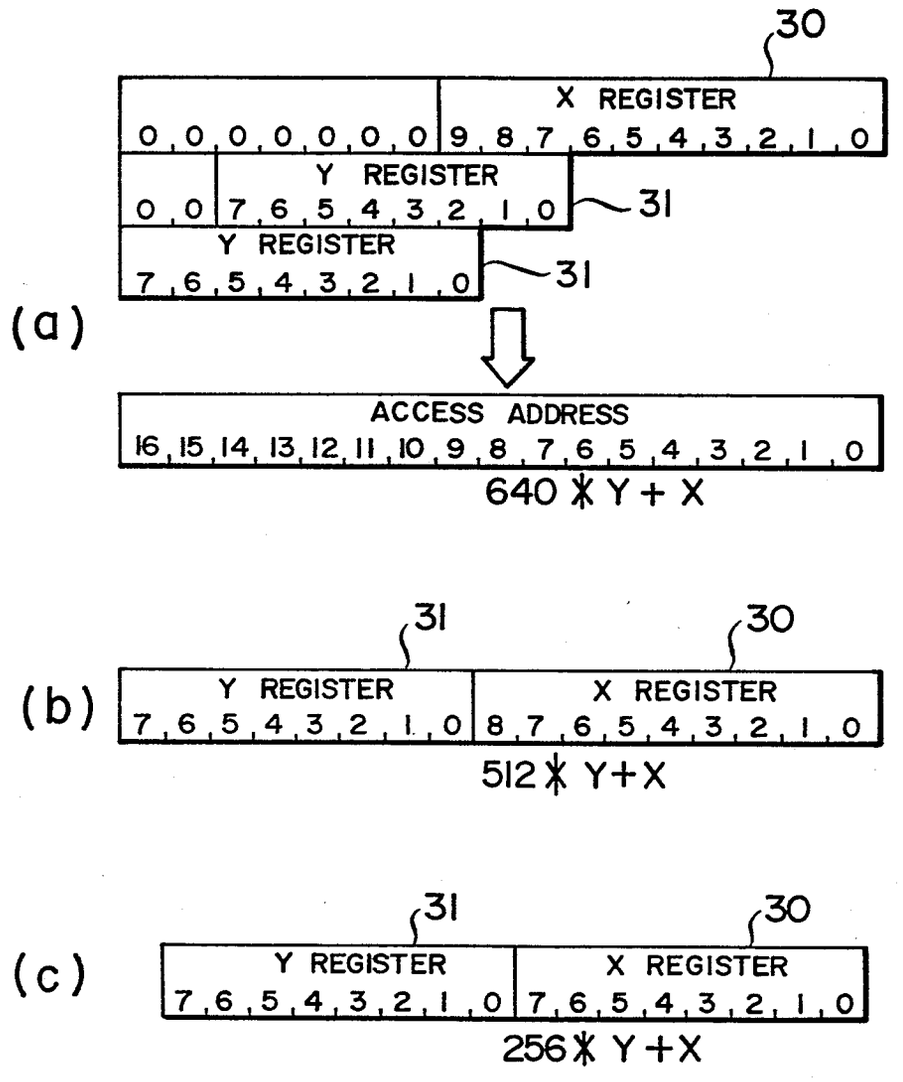

30
X REGISTER
0 0 0 0 0 0 0 9 8 7 6 5 4 3 2 1 0
Y REGISTER
0 0 7 6 5 4 3 2 1 0
31
Y REGISTER
7 6 5 4 3 2 1 0
31
(a)
ACCESS ADDRESS
16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
640 * Y + X
31
30
(b)
Y REGISTER
7 6 5 4 3 2 1 0
X REGISTER
8 7 6 5 4 3 2 1 0
512 * Y+X
31
30
(c)
Y REGISTER
7 6 5 4 3 2 1 0
X REGISTER
7 6 5 4 3 2 1 0
256 * Y+X

FIG. 6

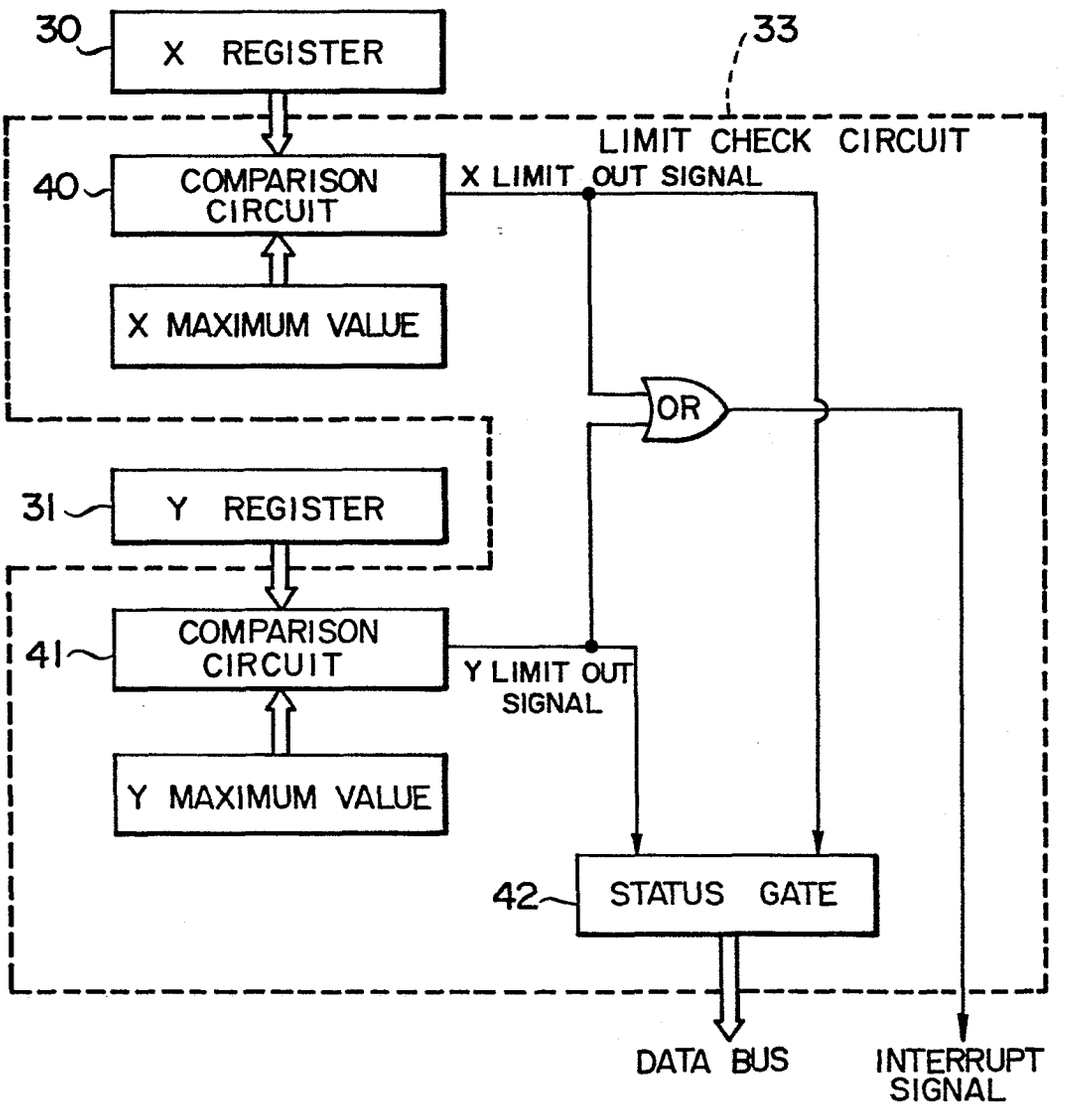

30
X REGISTER
33
LIMIT CHECK CIRCUIT
40
COMPARISON CIRCUIT
X LIMIT OUT SIGNAL
X MAXIMUM VALUE
OR
31
Y REGISTER
41
COMPARISON CIRCUIT
Y LIMIT OUT SIGNAL
Y MAXIMUM VALUE
42
STATUS GATE
DATA BUS
INTERRUPT SIGNAL

FIG. 7

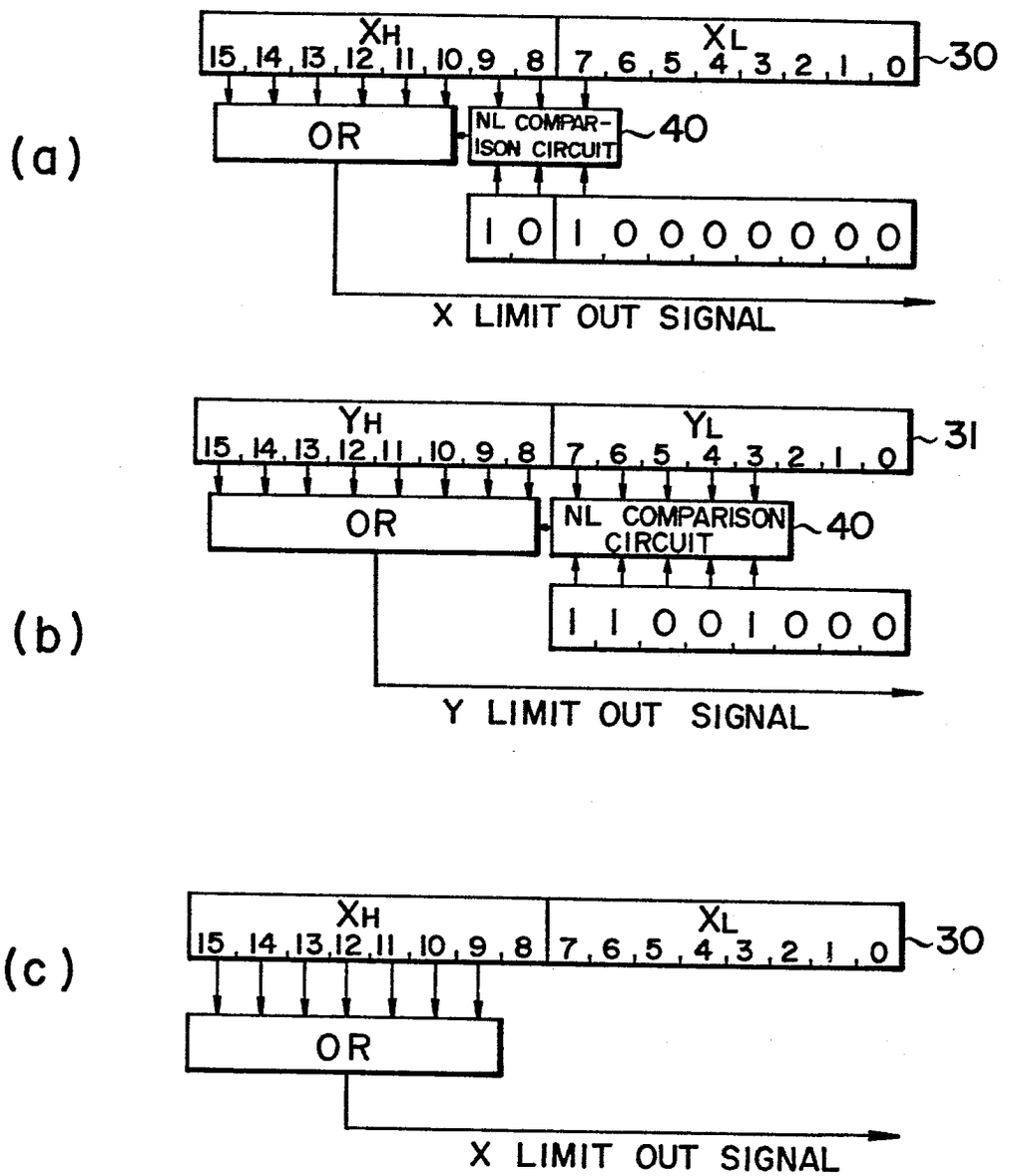

(a)
XH
15 14 13 12 11 10 9 8
XL
7 6 5 4 3 2 1 0
30
OR
NL COMPAR-ISON CIRCUIT
40
1 0 1 0 0 0 0 0 0
X LIMIT OUT SIGNAL
(b)
YH
15 14 13 12 11 10 9 8
YL
7 6 5 4 3 2 1 0
31
OR
NL COMPARISON CIRCUIT
40
1 1 0 0 1 0 0 0
Y LIMIT OUT SIGNAL
(c)
XH
15 14 13 12 11 10 9 8
XL
7 6 5 4 3 2 1 0
30
OR
X LIMIT OUT SIGNAL

FIG. 8

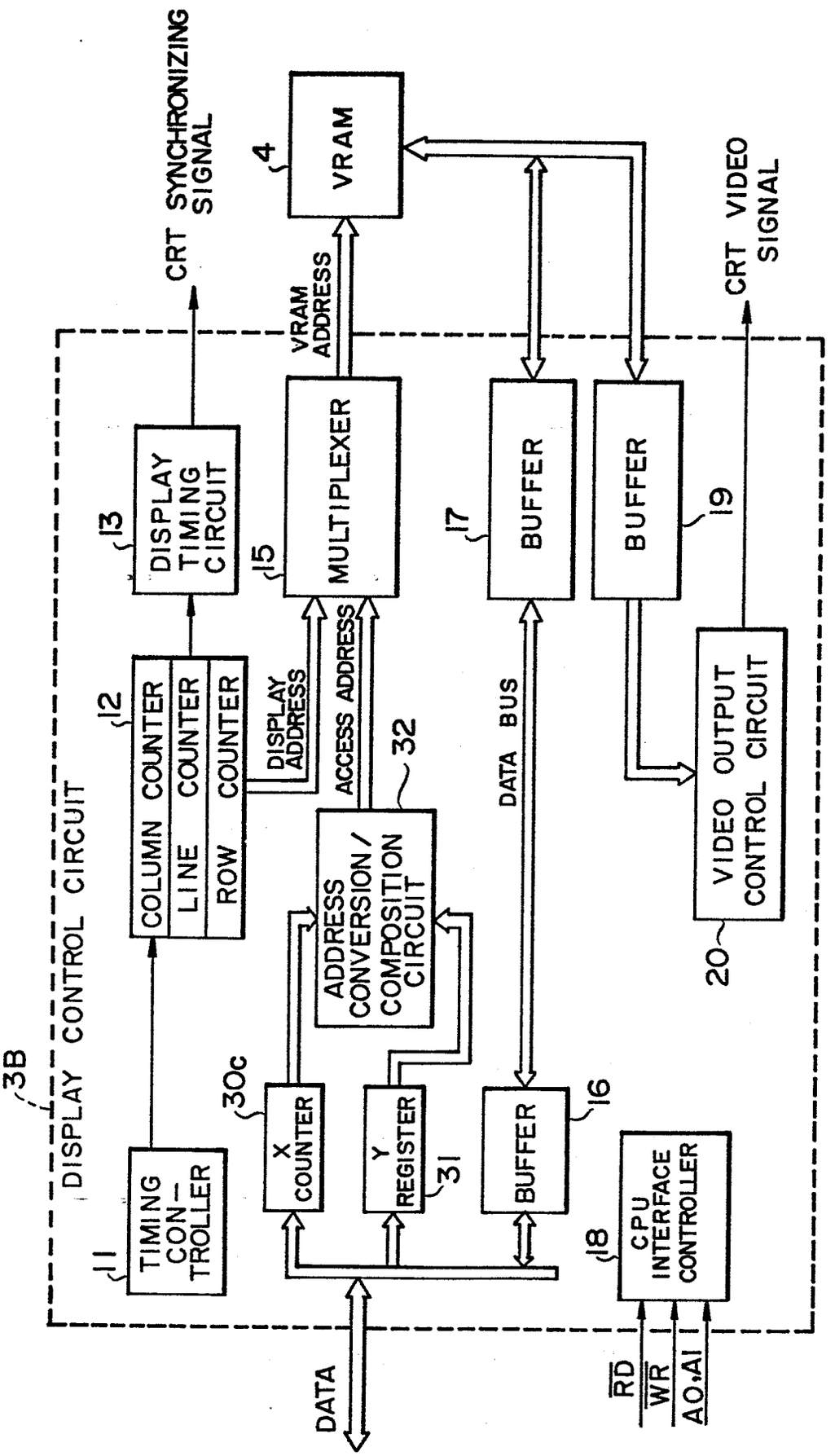

3B
DISPLAY CONTROL CIRCUIT
11
TIMING CON-TROLLER
12
COLUMN COUNTER
LINE COUNTER
ROW COUNTER
13
DISPLAY TIMING CIRCUIT
15
MULTIPLEXER
4
VRAM
17
BUFFER
19
BUFFER
16
BUFFER
18
CPU INTERFACE CONTROLLER
20
VIDEO OUTPUT CONTROL CIRCUIT
30c
X COUNTER
31
Y REGISTER
32
ADDRESS CONVERSION / COMPOSITION CIRCUIT
CRT SYNCHRONIZING SIGNAL
VRAM ADDRESS
CRT VIDEO SIGNAL
DISPLAY ADDRESS
ACCESS ADDRESS
DATA BUS
DATA
RD
WR
A0,A1

FIG. 9

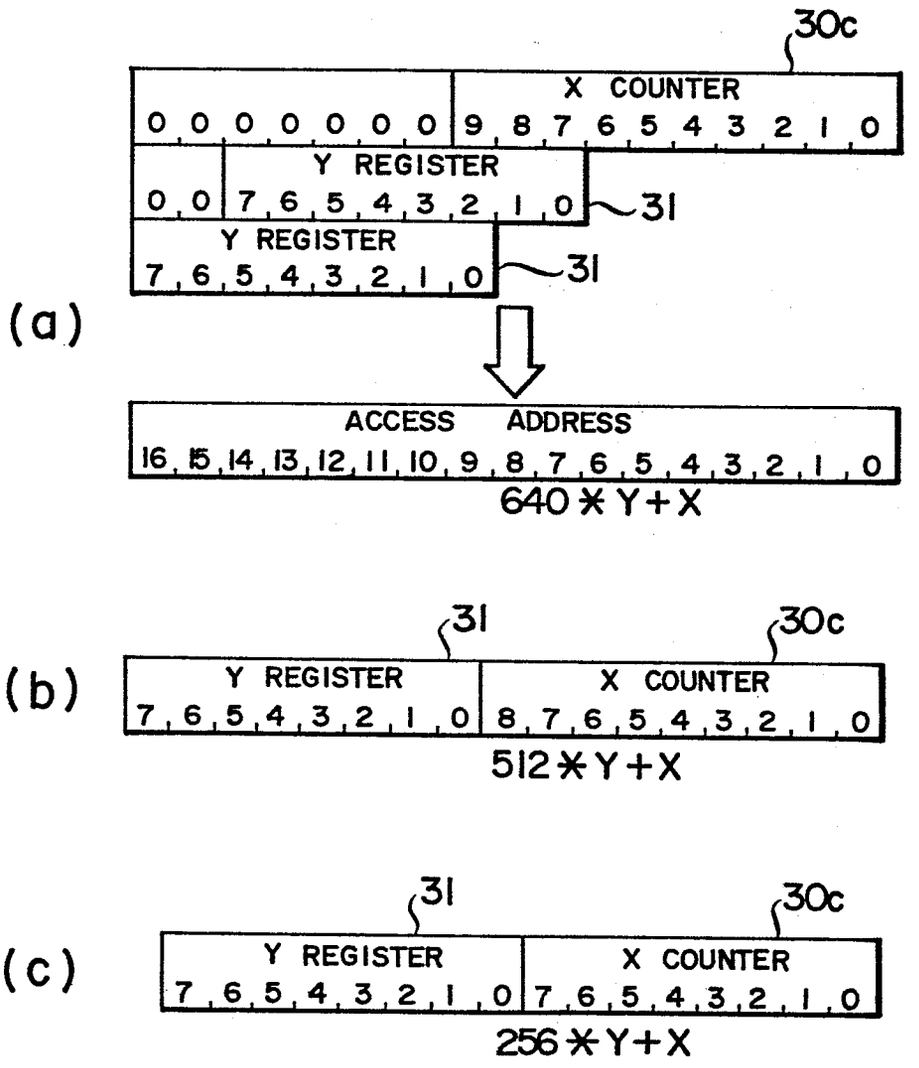

30c
X COUNTER
0 0 0 0 0 0 0 9 8 7 6 5 4 3 2 1 0
Y REGISTER
0 0 7 6 5 4 3 2 1 0
31
Y REGISTER
7 6 5 4 3 2 1 0
31
(a)
ACCESS ADDRESS
16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
640 * Y + X
31
30c
(b)
Y REGISTER
7 6 5 4 3 2 1 0
X COUNTER
8 7 6 5 4 3 2 1 0
512 * Y + X
31
30c
(c)
Y REGISTER
7 6 5 4 3 2 1 0
X COUNTER
7 6 5 4 3 2 1 0
256 * Y + X

FIG. 10

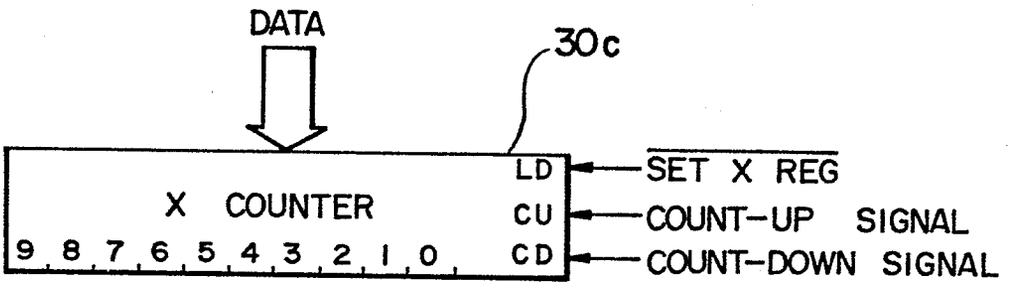

DATA
30c
X COUNTER
9 8 7 6 5 4 3 2 1 0
LD
CU
CD
SET X REG
COUNT-UP SIGNAL
COUNT-DOWN SIGNAL

FIG. 11

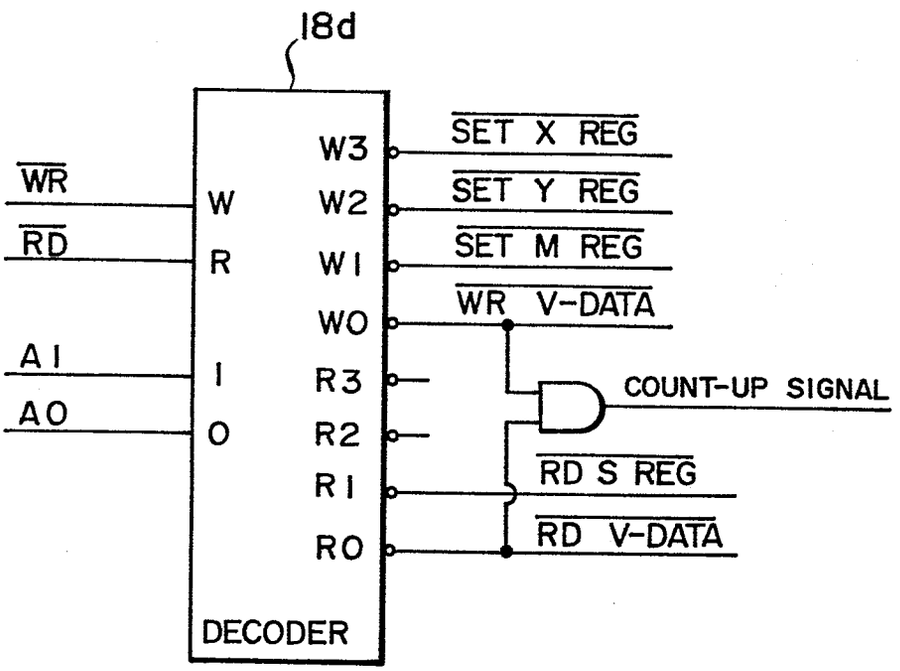

18d
WR
RD
A1
A0
W
R
1
0
W3
W2
W1
W0
R3
R2
R1
R0
DECODER
SET X REG
SET Y REG
SET M REG
WR V-DATA
COUNT-UP SIGNAL
RD S REG
RD V-DATA

FIG. 12

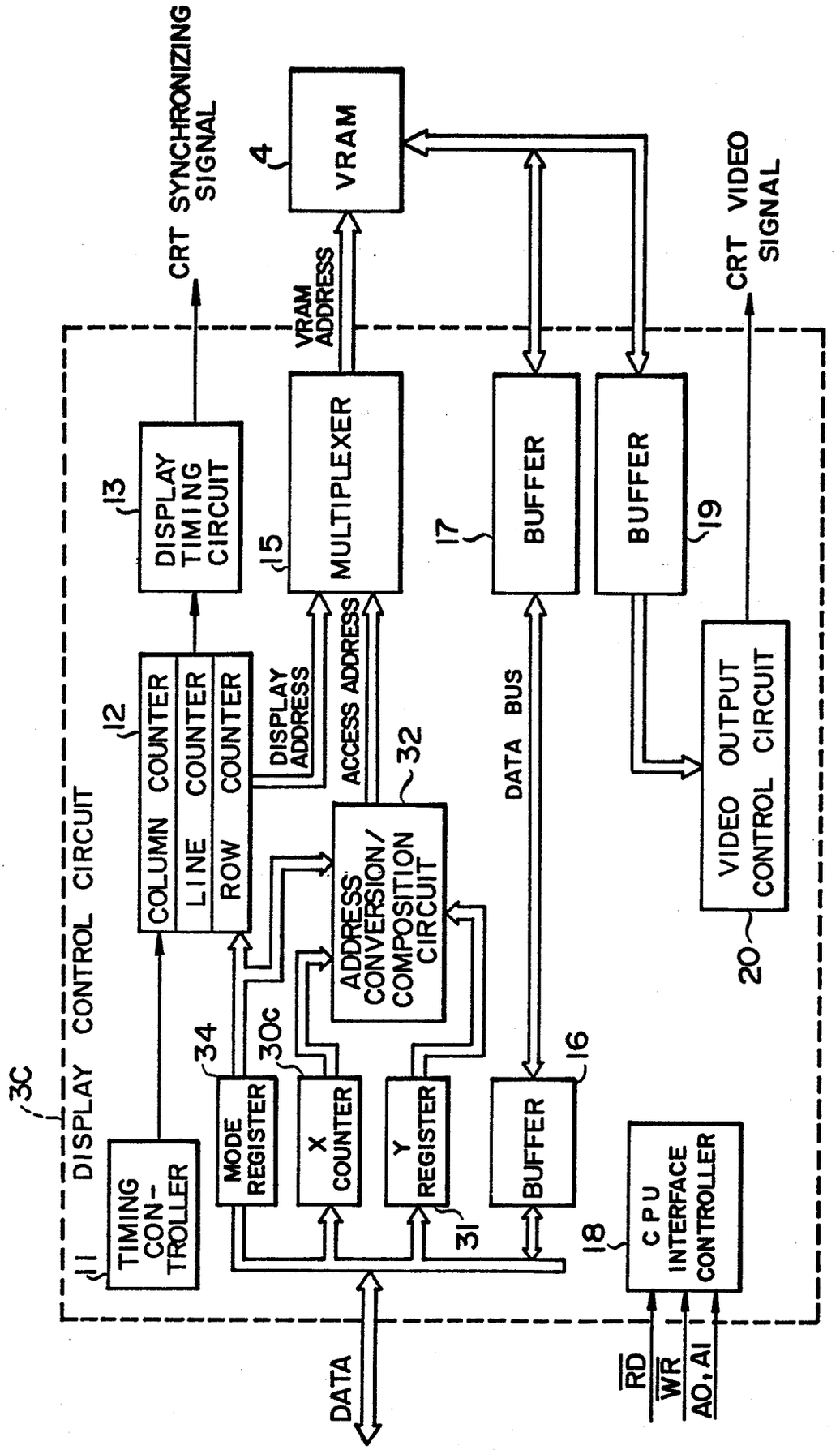
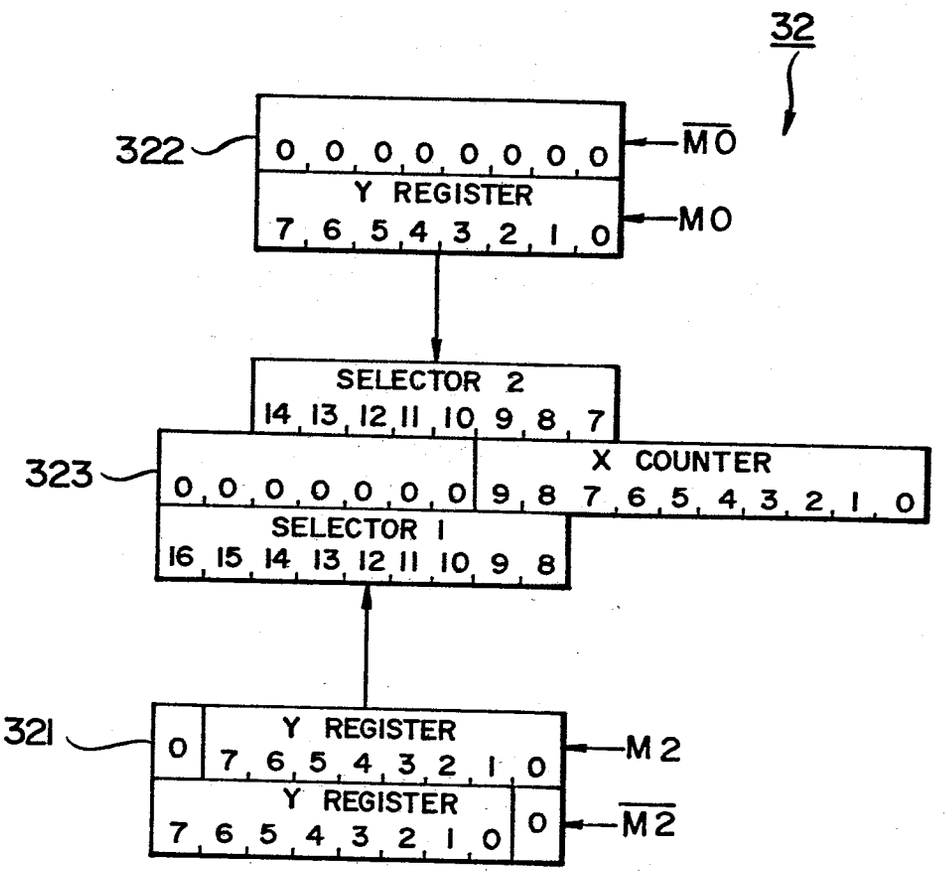

DISPLAY CONTROL CIRCUIT
3C
TIMING CONTROLLER
11
MODE REGISTER
34
X COUNTER
30c
Y REGISTER
31
ADDRESS CONVERSION/ COMPOSITION CIRCUIT
32
COLUMN COUNTER
LINE COUNTER
ROW COUNTER
12
DISPLAY TIMING CIRCUIT
13
MULTIPLEXER
15
VRAM
4
VRAM ADDRESS
CRT SYNCHRONIZING SIGNAL
DISPLAY ADDRESS
ACCESS ADDRESS
DATA BUS
BUFFER
16
BUFFER
17
BUFFER
19
CPU INTERFACE CONTROLLER
18
VIDEO OUTPUT CONTROL CIRCUIT
20
CRT VIDEO SIGNAL
DATA
RD
WR
A0, A1

FIG. 13



MODE	SCREEN CONFIGURATION
MO	640 X 200
M1	512 X 200
M2	256 X 200

FIG. 14

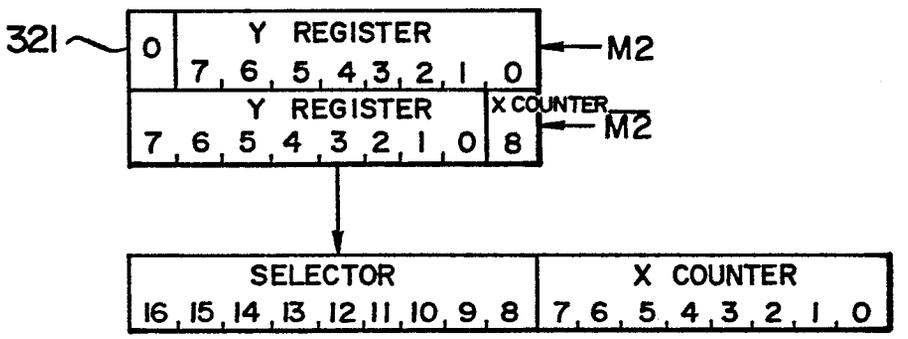
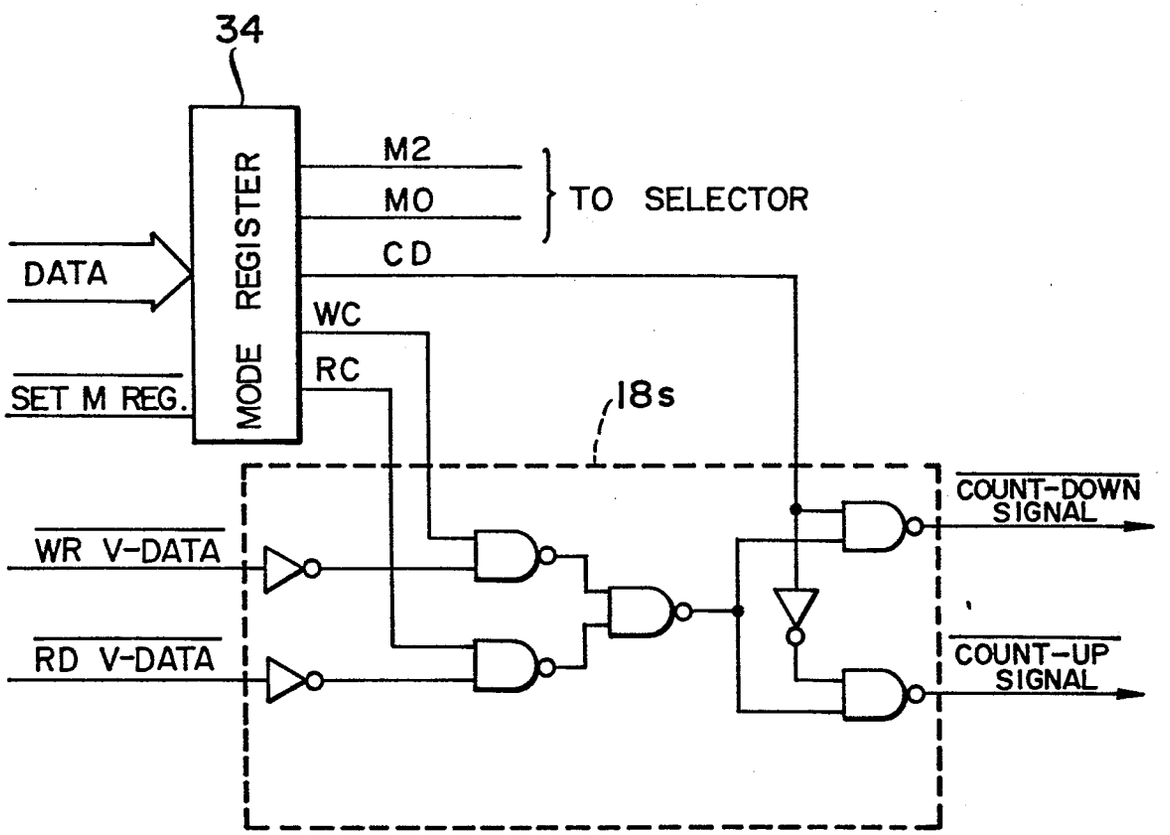

321
0
Y REGISTER
7 6 5 4 3 2 1 0
M2
Y REGISTER
7 6 5 4 3 2 1 0
X COUNTER
8
M2
SELECTOR
16 15 14 13 12 11 10 9 8
X COUNTER
7 6 5 4 3 2 1 0

FIG. 15


34
MODE REGISTER
M2
MO
TO SELECTOR
CD
DATA
WC
RC
SET M REG.
18s
WR V-DATA
RD V-DATA
COUNT-DOWN SIGNAL
COUNT-UP SIGNAL