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(54) Circuit for generating test signals for in-circuit digital testing.

(57) A circuit for use with a central processor for the in-circuit testing of the electrical properties of components interconnected at electrical nodes in a circuit under test is disclosed. The nodal test signals have first, second, and disconnect logic states. A test vector processor responds to the central processor to control the generation of the nodal test signals during a test cycle. A plurality of digital test signal means responsive to the vector processor are also provided. Each test means includes a circuit means for storing test signal generating data, and responsive to the stored data, controls the generation of the logic state of a nodal test signal where the logic state of the test signal is controlled to (1) keep the same logic state as the previous logic state, (2) toggle to the opposite state as the previous logic state, or (3) assume either a logic zero or a logic one state regardless of the previous logic state.

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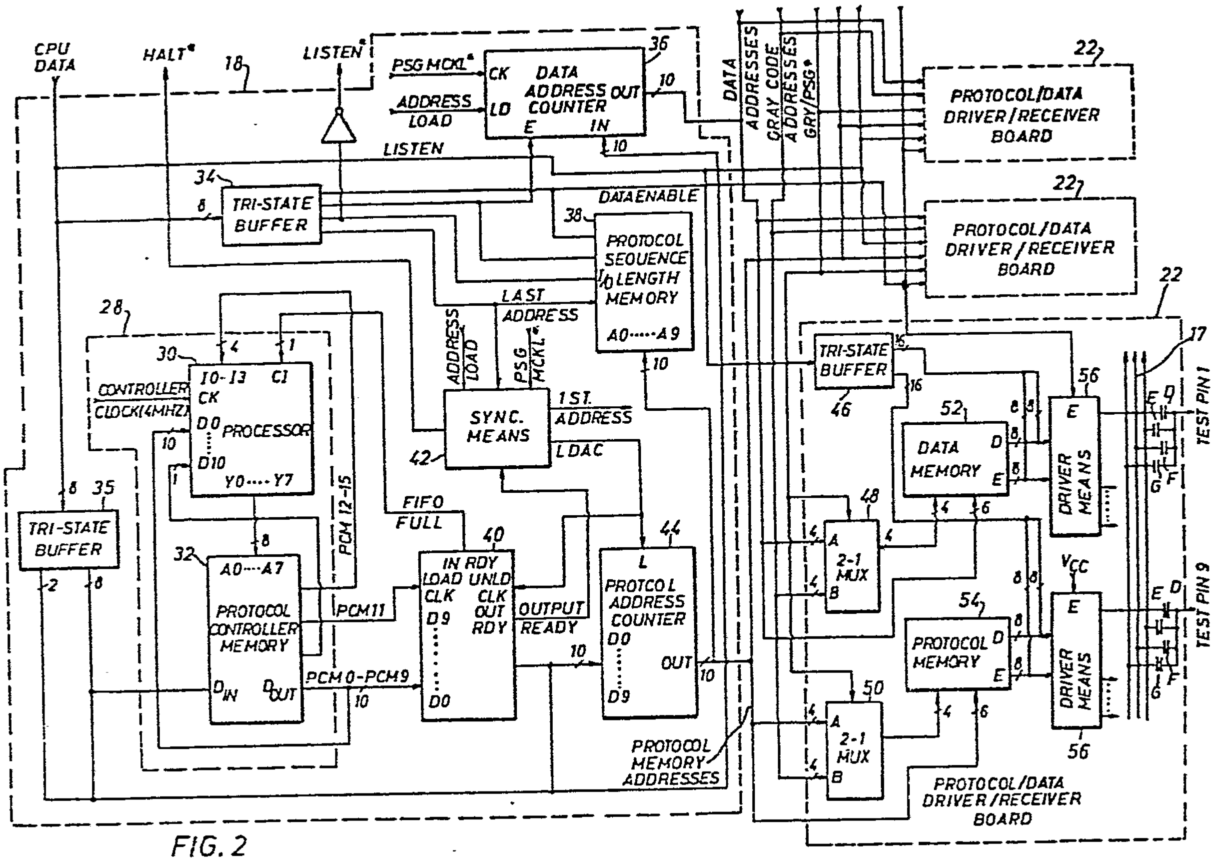
CPU DATA
HALT*
18
LISTEN*
PSG MCKL*
ADDRESS LOAD
CK
LD
E
IN
OUT
DATA ADDRESS COUNTER
36
10
LISTEN
34
8
TRI-STATE BUFFER
DATA ENABLE
38
PROTOCOL SEQUENCE LENGTH MEMORY
I/O
A0·····A9
LAST ADDRESS
ADDRESS LOAD
PSG MCKL*
28
30
I0-I3
CI
4
1
CONTROLLER CLOCK(4MHZ)
CK
D0
PROCESSOR
D10
Y0····Y7
PCM 12-15
SYNC. MEANS
42
1ST. ADDRESS
LDAC
FIFO FULL
35
TRI-STATE BUFFER
2
32
A0···A7
PROTOCOL CONTROLLER MEMORY
DIN
DOUT
PCM11
PCM 0-PCM9
40
IN RDY
LOAD UNLD
CLK
CLK
OUT
RDY
D9
D0
OUTPUT READY
44
L
PROTOCOL ADDRESS COUNTER
D0
D9
OUT
PROTOCOL MEMORY ADDRESSES
DATA
ADDRESSES
GRAY CODE
ADDRESSES
GRY/PSG*
22
PROTOCOL/DATA DRIVER/RECEIVER BOARD
22
PROTOCOL/DATA DRIVER/RECEIVER BOARD
22
17
TRI-STATE BUFFER
46
15
16
52
DATA MEMORY
D
E
56
E
DRIVER MEANS
D
G
F
TEST PIN 1
48
A
B
2-1 MUX
4
6
VCC
54
PROTOCOL MEMORY
DRIVER MEANS
TEST PIN 9
50
2-1 MUX
56
PROTOCOL/DATA DRIVER/RECEIVER BOARD

FIG. 2

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EUROPEAN SEARCH REPORT

0154048
Application Number

EP 84 20 1743

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	EP-A-0 011 352 (GENRAD) * Page 5, line 27 - page 6, line 34 * ---	1	G 01 R 31/28
A	GB-A-2 019 012 (NCR) * Page 4, lines 51-58; page 5, line 30 - page 31, line 5; page 9, line 38 - page 10, line 4; page 11, lines 30-32; figures 2,3B,5 * ---	1	
A	WESCON TECHNICAL PAPERS, vol. 19, 16th-19th September 1975, pages 27/2-1 - 27/2-4, North Hollywood, US; J.F. CAMPBELL: "A new real-time function test generation system for complex LSI testing" * Figure 1 * ---	1	
A,D	GB-A-2 020 439 (ZEHNTEL) * Page 5, line 15 - page 6, line 2; figures 2a,2b * ---	2	
A	US-A-4 070 565 (ZEHNTEL) * Abstract * ---	1	TECHNICAL FIELDS SEARCHED (Int. Cl.4)
A	US-A-4 125 763 (DRABING) * Column 3, line 47 - column 4, line 15; figure 2 * -----	1	G 01 R 31/28 G 06 F 11/26

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16-11-1987	GUIVOL Y.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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