(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 157 524**
**A2**

# (12) EUROPEAN PATENT APPLICATION

(21) Application number: **85301823.2**

(22) Date of filing: **15.03.85**

(51) Int. Cl.⁴: **G 09 G 3/00**, G 09 G 3/36

(30) Priority: **30.03.84 GB 8408216**

(43) Date of publication of application: **09.10.85 Bulletin 85/41**

(84) Designated Contracting States: **CH DE FR LI NL**

(71) Applicant: **NATIONAL RESEARCH DEVELOPMENT CORPORATION, 101 Newington Causeway, London SE1 6BU (GB)**

(72) Inventor: **Clark, Michael George, 12 Churchdown Road, Malvern Worcestershire WR14 2JX (GB)**
Inventor: **Glasper, John Lewis, 'Eastlea' Homend Crescent, Ledbury Herefordshire (GB)**
Inventor: **Hughes, Anthony James, 8 Birchwood Road, Malvern Worcestershire (GB)**
Inventor: **Smith, Charles James Thomas, 61 Clerkenwell Crescent, Malvern Worcestershire (GB)**

(74) Representative: **Beckham, Robert William et al, *Procurement Executive Ministry of Defence* Patents 1A(4), Room 2014, Empress State Building Lillie Road London SW6 1TR (GB)**

## (54) Flat panel display.

(57) A flat-panel display (1) comprising a panel (3) including intersecting row and column electrodes (11, 13) and using selected unipolar isogonal waveform signals to address each set of row electrodes (11) and each set of column electrodes. This allows display of simple geometric structures - reference lines, grids, cross-wire features and reference symbols such as boxes and line markers, structures all requiring representation by two or more picture elements in some of the colums (13). The panel matrix may be of cartesian or polar format. As example, a cross-wire feature display (1) is shown and described. Two isogonal signals, a squarewave and its inverse, are generated using two shift and store bus registers (7 & 9). Signal and electrode selection is controlled in response to input co-ordinate address data, using a comparator (27; 29) and an exclusive-OR gate (15; 17) to control the data input (D) of each register (7; 9).

The flat panel display (1) may be used as a graticule in an optical sight or image projection system. Alternatively it may be used as an overlay to printed, back projected, and other static images and pictures. It may be used as an accessory to a cathode ray tube or to another flat-panel electronic display. Also, it may take the form of a quasi-analogue meter display with an additional hand used to denote or record some particular value or values of the variable displayed by the main hand.

EP 0 157 524 A2

# FLAT-PANEL DISPLAY

## TECHNICAL FIELD:-

The present invention concerns a flat-panel display, in particular a display for use as a graticule or as an overlay, one suitable for displaying graticule or grid features, or graphics symbols of simple geometric shape, in outline or in solid form, eg. for co-ordinate reference or for labelling.

## BACKGROUND ART:-

A flat-panel liquid crystal display, in particular a graticule, is described in UK Patent Specification No. 1,432,558. This graticule comprises a film of liquid crystal material sandwiched between electrode bearing transparent plates. The electrodes on each plate are arranged in rows and columns to define, by their intersection, a matrix of co-ordinate addressable picture elements. Antiphase or in-phase alternating-voltage address signals are applied to one row electrode and to one column electrode. All remaining electrodes are referred to earth potential. This results in the display of a cross-wire graticule feature. By applying the address signals to different rows and columns, the cross-wire feature may be centred on any selected co-ordinate position of the display. Although in that specification, reference is made to the application of dc signal address, such form of address is impractical for sustained liquid crystal panel display. Liquid crystal materials and panel performance tend to degrade in the presence of sustained unipolar fields. This is due to electrolytic polarisation phenomena. An alternating current power source is required. Where these displays are battery powered, an inverter or oscillator must be employed to provide the necessary alternating power. In consequence of this, there is loss in power efficiency.

DISCLOSURE OF THE INVENTION

It has now been found that unipolar, isogonal, waveform signals, instead, may be used as address signals for the above application. Furthermore, these signals may be used not only to display cross-wire features, but also to display other features and symbols of simple geometric form. These signals are characterised by the following properties:-

Signals $W_n(t)$. $n = 1$ to $N$;

$$\oint (W_n - W_m)\, dt = 0; \text{ and,}$$

$$\oint (W_n - W_m)^2 dt = V_o^2 \sin \alpha, \; n \neq m,$$

where $\oint$ here denotes $\frac{1}{T}\int_o^T$, T being the period of one cycle.

The voltage drive signals $W_n(t)$, have, as expressed by the above formulae, non-zero RMS value. The voltage difference between any two different signals is truly alternating in nature, and this voltage difference is of constant RMS value for all pairs of different isogonal signals. Particular examples of isogonal signals are pseudo-random binary sequence coded waveforms and Walsh-function waveforms. For matrix, or matrix-equivalent electrode configuration panels, these signals have been used only where it has been possible to represent the desired feature by, at most, a single contrasting point or segment corresponding to each column. Hitherto, isogonal signal address has been used for signal-waveform displays (See UK Patent Specification Nos 2001794; 2050667; 2101786); for horological or meter displays (See UK Patent Specification Nos. 2044975; 2106298); for numeral bar-segment displays (See UK Patent Specification No. 2114354); and, for radar target plot displays (See UK Patent Specification No. 2129993). In these known applications different isogonal waveforms are applied,

in a predetermined fixed order, one to each row electrode, simultaneously. At the same time, selected waveform signals are applied one to each column electrode. The selected waveform, in each case, may be the same as one of the different row waveforms, or it may be a different isogonal signal. At the majority of picture elements the address signals carried by the intersecting row and column electrodes are different. The voltage difference is alternating, and is of sufficient RMS magnitude to maintain the sandwiched liquid crystal material in its ON state. At the remaining picture elements, however, at most one corresponding to each column electrode, the intersecting row and column electrodes are addressed by identical waveform signals. At these picture elements the difference voltage is identically zero. The sandwiched liquid crystal material at these picture elements is maintained in an OFF state. Using contrasting ON/OFF state optical effects - such as dynamic scattering, twisted nematic, or dyed cholesteric, the OFF picture elements are displayed in contrast against a background of ON picture elements.

Unipolar isogonal signals offer an advantage in that they can be generated or stored using dc power and using only low-power consuming semiconductor components. The same fabrication technology - eg. silicon MOS, can be employed for the fabrication of power circuits and address logic circuits. It is thus possible to achieve a high degree of circuit integration and this indicates the possibility of low-cost high yield mass production.

In the applications described below only a few isogonal waveform signals are required for the display of simple geometric features and symbols. The number of signal bits per cycle can therefore be chosen low. This implies low clock rates, simple electronics and low power.

Whilst similar types of display can be addressed using time multiplexed address methods, the isogonal waveform addressed displays disclosed herein have advantage in the fact that the picture element voltage differences produced are either zero or of arbitrarily high

fixed amplitude. They are in comparison, therefore, relatively immune to effects of ambient temperature drift and the nature of the electro-optic media characteristics - eg. the liquid crystal threshold voltage characteristic.

In accordance with this invention, there is provided a flat-panel display comprising:-

an optically transmissive flat-panel of the type including a set of row and a set of column electrodes, one set each side of an electro-optic medium, the electrodes providing by their intersection a matrix of co-ordinate addressable picture elements;

a source-means, for providing a set of unipolar isogonal waveform drive signals;

row-address means, co-operative with the source means, and connected to each row electrode, for applying selected drive signals to each one simultaneously, whilst being capable of applying identical signals to a plurality of the row electrodes; and,

column address means, also co-operative with the source means, and connected to each column electrode, for applying selected drive signals to each column electrode simultaneously, whilst being capable thus of applying identical signals to a plurality of the column electrodes.

The electro-optic material may be, for example, a liquid crystal material. Accordingly, the flat-panel may be of dynamic scattering, twisted nematic, dyed nematic or dyed-cholesteric type. The ON-state can be optically transmitting, or it can be chosen opaque, depending on the choice of panel type and the construction adopted. For overlay application, a zero-polariser guest-host panel is preferred as this exhibits a high ON-state transmission.

The row and column electrodes may be straight and intersect orthogonally, forming a Cartersian co-ordinate format. However, the intersection can be non-orthogonal, and the electrodes can be of curved form. The display area may be arcuate, the row electrodes-concentric

annular segments, and the column electrodes - radial segments, allowing representation in polar co-ordinate format. Alternatively, the display area may be full circular or elliptic, the row electrodes of spiral form, and the column electrodes of either radial segment or counter-spiral form.

The source means may comprise a single generator or store co-operative with both row and column address means. Alternatively it may comprise a pair of components, one co-operative with the row-address means, the other co-operative with the column-address means. Isogonal signals may be generated, for example, using a shift-register, or by clocking signal bits from a memory.

The display may be operable in a dynamic mode. In this mode it can display the chosen feature or symbol at a position centred on a data-determined co-ordinate of the display area. The row and column address means may be data address responsive, and capable therefore of selecting drive signals and electrodes in accordance with data address. It is thus possible to display a cross-wire feature or other reference symbol, such as a cross or square, in a manner allowing tracking over the display area.

The display may instead, be operable in an interchangeable static mode. For example, it may be used for the display of grid lines. The display may be changed from displaying grid lines of one dimensional scale to displaying grid lines of another scale, or from displaying one form eg. linear-linear scale, to displaying another form, eg. log-linear or log-log scale. This may be achieved using cycled co-ordinate address data. Manual switching, or form-specific address data may instead be used to select signals from a pre-loaded memory.

BRIEF INTRODUCTION OF THE DRAWINGS

In the accompanying drawings:-

Figure 1 is a block-schematic circuit drawing illustrating an embodiment of this invention, a dynamic cross-wire feature display;

Figure 2 is a block-schematic drawing showing a modification of the above display, one enabling the static display of grid-line features;

Figures 3 to 7 are illustrative schematic drawings showing different display features, or symbols and associated waveform signal allocations;

Figures 8 and 9 shown, in schematic plan, two types of electrode arrangements that may be used for the display of complex features and symbols.

Figures 10a, b show in schematic plan front and back electrode arrangements for an analog meter display; and

Figures 11a, b, c, d show, the matrix to which the arrangement of Figure 10 is equivalent.

DESCRIPTION OF PARTICULAR EMBODIMENTS

Embodiments of this invention will now be described with reference to the drawings. Such description is given by way of example only.

In figure 1, the flat panel display 1 shown comprises a liquid crystal flat-panel 3 and electrode address drive circuitry 5. The panel electrodes are addressed using no more than two isogonal unipolar waveform address signals, $W_1$, $W_2$, simple antiphase square wave signals of common amplitude V i.e. one square wave signal and its inverse. These signals are generated using a pair of clocked shift-and-store bus registers 7 and 9. These also are arranged with their outputs connected to the row electrodes 11 and to the column electrodes 13. Signal inversion, and thus generation of the isogonal inverted signals, is controlled by means of two exclusive OR-gates 15 and 17, one connected to each register 7 and 9. A clock oscillator 19 is provided to clock both registers 7 and 9. This clock 19 is also connected to the strobe input ST, of each register 7 and 9, via a divide-down counter 21 and a monostable 23. The display also includes

a flip-flop bistable 25. This is responsive to the monostable 23, and is connected to one input of each of the exclusive OR gates 15 and 17. The other input of each exclusive OR gate 15 and 17 is connected to a data comparator. One comparator 27, compares counter data with input Y-co-ordinate data. The other comparator, 29, compares the counter data with input X-co-ordinate data.

For simplicity of description, the matrix comprises 16 rows and 16 columns. However it will be apparent that the circuit can be easily expanded to drive larger matrices.

Operation is as follows:- As a first simplification, operation of the exclusive OR gates 15 and 17 and the comparators 27 and 29 can be ignored. As the counter 21, here a 4-bit counter, is clocked through its sequence, the shift registers 7 and 9 are clocked at the same rate. The ÷2 flip-flop 25 supplies a logic "0" level signal to the serial data input D of the column address register 9. At the same time, it supplies a logic "1" level signal to the serial data input D of the row address register 7. After 16 clock pulses, the shift registers 7 and 9 are fully loaded and the monostable 23, which is triggered from the negative going edge of the counter's final output, produces a strobe pulse which transfers "0"s from the column shift register 9 to all the column electrodes 3 and "1"s from the row shift register 7 to all the row electrodes 11. At the same instant, the flip-flop 25 is clocked, reversing the inputs to the shift registers. For the next 16 clock pulses, "1"s are fed to the column shift register 9 and "0"s to the row shift register 7. On the 32nd clock pulse "1"s are strobed out to the column electrodes 13, and "0"s to the row electrodes 11. The flip-flop 25 again changes state and the process repeats, resulting in square waves of opposite phase being applied to the column and row electrodes 13 and 11.

The effect on the display is that the difference of the two waveforms $W_1$ and $W_2$ is applied across all the picture elements causing the whole display 1 to be maintained in the ON state.

Consider now the operation of the exclusive-OR gates 15 and 17, and the row and column data comparators 27 and 29. When binary data from the counter 21 matches the X-co-ordinate input data, a "1" appears at the output of the column comparator 29. This is fed to one input of the column exclusive-OR gate 17 and causes the gate to invert the level applied to its other input, for one clock period only. This results in a waveform eg. $W_2$ from one of the shift register outputs, a waveform which is the inverse of all the other output waveforms, eg. $W_1$. The position that this inverted waveform occupies in the column shift register 9 is determined by the data applied to the column comparator 29. The electrode 13 to which this waveform is applied will have zero volts between it and all but one of the row electrodes, for identical signals are applied. This causes all but one of the picture elements, defined by this column electrode, to be held in the OFF state. Operation of the row register 7, row exclusive-OR gate 15 and row comparator 27 is exactly similar but for the position of the inverted level which is determined by Y-co-ordinate input data. As the X and Y co-ordinate input data is changed, the cross-wire feature 31 tracks across the display 3 to follow these changes. The cross-wire feature 31 is centred at all times on the co-ordinate positions defined by the input data.

With the simple addition (fig. 2) of a latched stack memory 33, and a strobe monostable delay 35 to act as data sources for the row and column comparators 27 and 29, it is possible to convert the display described above to a static-mode operational grid reference display. The row and column co-ordinates are stored in their respective stacks and moved on by each strobe pulse following the "1" level comparator output. With data presented in this way, the data input D to each register 7 and 9 receive an inverted level several times each strobe cycle and a plurality of rows and columns are addressed with inverted signal. This results in a grid display. Thereafter, by switching from one stack block to another, it is possible to change the position of the grid lines. The data store in each stack block can be chosen to represent different dimension scales and different scale forms.

In the above two examples the two signals $W_1$, $W_2$ used can be expressed as a string of binary digits:-

$W_1$ = 0,1,0,1, .....

$W_2$ = 1,0,1,0, .....

For these two signals:-

$\oint W_1\,dt = \oint W_2\,dt = \frac{1}{2}$, ie. each is of non-zero mean value;

and,

$W_1 - W_2 = \bar{1}, 1, \bar{1}, 1$ .....

$\oint (W_1 - W_2)\,dt = 0$, ..... a truly alternating voltage difference

but,

$\oint (W_1 - W_2)^2\,dt = 1$ , a non-zero RMS voltage.

The signals $W_1$, $W_2$ are thus isogonal, as defined.

Various waveform allocations are depicted in figures 3 - 7. These figures serve to illustrate some of the simple geometric symbols and features that can be achieved using isogonal signal drive. In the first three of these figures, figures 3 - 5, only two isogonal drive signals $W_1$ and $W_2$ are required. In both figures 3 and 5, which depict a cross-wire feature and a grid feature, respectively, most picture elements are driven ON. In the alternative cross-wire feature display, figure 4, most picture elements are driven OFF. (One input of the row gate 15 may be connected instead to the non-inverting output of the flip-flop 27, to produce this result.) According to the display effect utilised, the ON state may correspond to either a transmissive or an opaque optical state. With a greater number of isogonal waveform signals, other and more complex patterns can be

generated. In figure 6 it is shown how a box domain can be defined using only 4 different isogonal signals. A more complex tracking symbol is shown in figure 7. This uses 7 waveform signals.

More complex patterned features or symbols may be obtained by the superposition of panels. For example a double panel comprised of three electrode-bearing plates, two electro-optic media and four sets of transparent electrodes, can be utilised. The two superimposed patterns may be of different colour, and like or reverse contrasts can be employed. Alternatively, one panel may be used as an attenuator or colour filter while the other is used to show the desired feature or symbol pattern.

In figure 8 a concatenated electrode layout is shown, essentially a combination of sub-matrices.

In figure 9 an interleaved electrode layout is shown. For simple depiction, only one representative column is shown.

Concatenation or interleaving - as for example shown by figures 8 and 9 - may be used, either with single panels or with double panels, to increase the range of patterns which may be shown.

Furthermore, where broken outline patterns are acceptable, a pair of features may be displayed by using odd rows and columns, for one, and even rows and columns for the other. A complex feature can then be formed by combination of two simpler features.

The addressing technique disclosed above can be used to address an analogue meter having a variable pointer and an independently controlled additional pointer, e.g. a maximum or minimum limit stop. One suitable electrode pattern is shown in Figures 10a, b. A front electrode pattern, Figure 10a, has four sectors 41, 42, 43, 44 each with an addressing lead. A back electrode pattern, Figure 10b, has four meander electrodes 45, 46, 47, 48 each having a section in register with each sector of the rear electrode. Thus sixteen separately addressable pointers can be displayed.

When two pointers, e.g. a main pointer and a maximum (or minimum) pointer, are to be displayed at the same time the addressing circuit can be arranged to give an audible warning when the set limit is exceeded. Alternatively the additional pointer can be used to record the maximum or minimum deviation of the main pointer. If both a maximum and a minimum pointer are required they may be displayed alternately. A meter display is normally used in a reflective mode but could be used in a transmission mode.

The electrode arrangement of Figure 10 is electrically equivalent to a four by four matrix as shown in Figures 11, where the front electrodes 41, 42, 43, 44 become row electrodes, and the back electrodes 45, 46, 47, 48 become column electrodes. As before waveforms $W_n$, n is an integer, are applied to each electrode. The allocation of waveforms are of four types:

(i) those in which the main pointer alone is present, e.g. Figure 11a;

(ii) those in which the main and additional pointers correspond to two intersections lying on distinct rows and columns, e.g. Figure 11b;

(iii) those in which the main and additional pointers correspond to two intersections lying on the same row e.g. Figure 11c; and

(iv) those in which the main and additional pointers correspond to two intersections lying on the same column e.g. Figure 11d.

Waveforms $W_1$ to $W_4$ are applied as shown in Figures 11a-d.

FIELDS OF APPLICATION

The flat panel aforementioned may be used as a dynamic or static overlay to printed, back-projected, and other static images. It may be used as a graticule in an optical sight, or in an imaging system or other similar optical system, for example a projection system.

It may be used as a dynamic or static overlay as an accessory to a cathode ray tube (C.R.T.) or to another flat-panel electronic display - e.g. for use as an oscilloscope graticule.

The analogue meter display, Figures 10, 11, may be used in handheld and portable measurement instruments where low power consumption and low voltage operation are required.

Claims:-

1. A flat panel display comprising:-

an electro-optic medium contained between two spaced plates, a first set of electrodes and a second set of electrodes formed on the plates, the electrodes providing by their intersection a matrix of co-ordinate addressable picture elements;

characterised by:-

a source-means, for providing a set of unipolar isogonal waveform drive signals;

first-address means, co-operative with the source means, and connected to each electrode in the first set, for applying selected drive signals one to each electrode simultaneously with identical signals to a plurality of the electrodes; and,

second address means, also co-operative with the source means, and connected to each electrode in the second set, for applying selected drive signals one to each column electrode simultaneously, with identical signals to a plurality of the electrodes.

2. The display of claim 1 and including means for changing the order of drive signals applied to at least one set of electrodes.

3. The display of claim 1 and including means for changing the selection of drive signals applied to at least one set of electrodes.

4. The display of claim 1 wherein the first and second set of electrodes are arranged as row and column electrodes.

5. The display of claim 1 wherein the first and second set of electrodes are arranged as sector and meander electrodes.

6. The display of claim 1 wherein the electro-optic medium is a liquid crystal material.

7. The display of claim 1 wherein the source means is adapted to provide two isogonal different drive signals to both sets of electrodes to display a feature of cross or grid wire form.

8. The display of claim 1 wherein the wall plates and electrode are optically transparent.

9. The display of claim 1 wherein a reflector is incorporated at the rear of the flat panel.

10. The display of any one of claims 1 to 9 constructed, arranged and adapted to operate substantially as hereinbefore described with reference to the accompanying drawings.

0157524

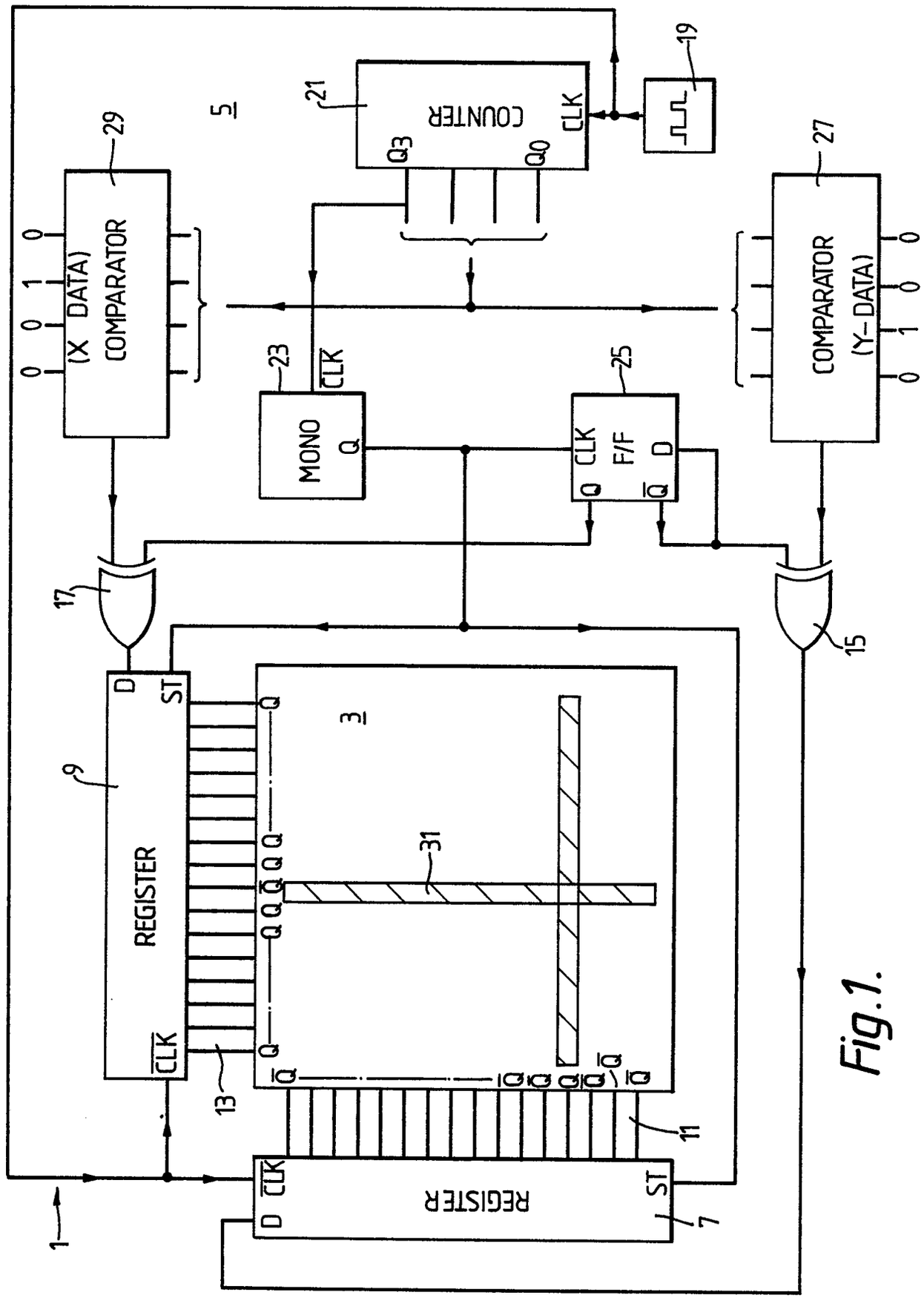



Fig.1.

0157524

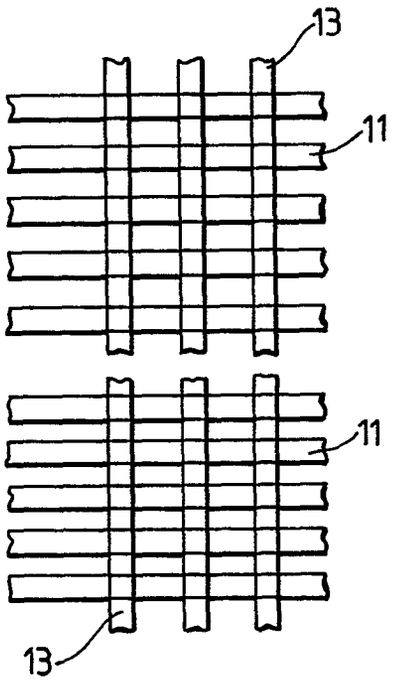



Fig.8.

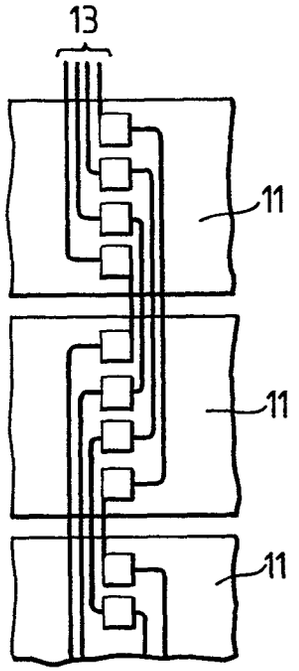



Fig.9.

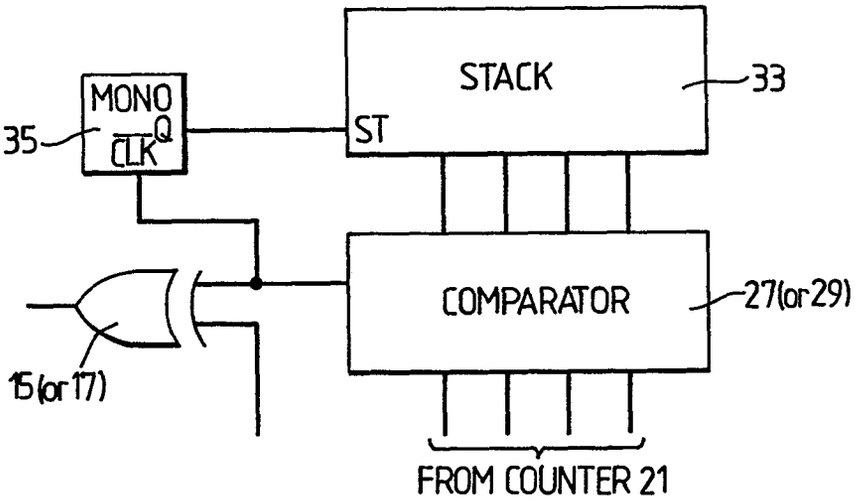



Fig.2.

0157524

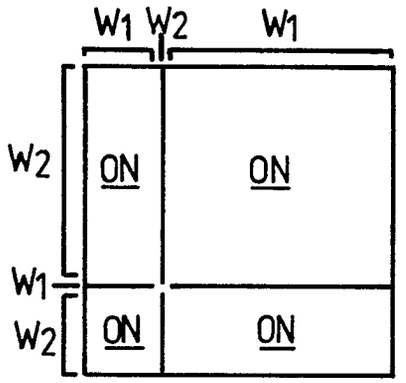



Fig. 3.

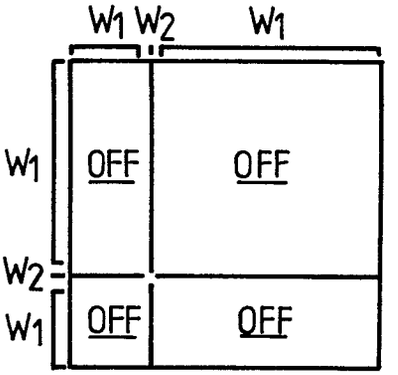



Fig. 4.

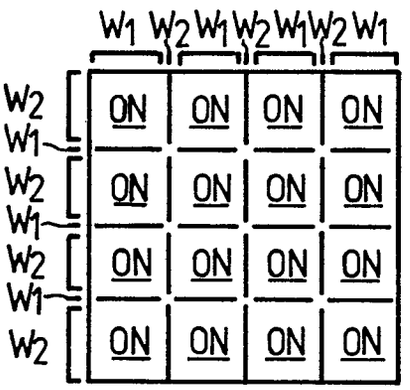



Fig. 5.

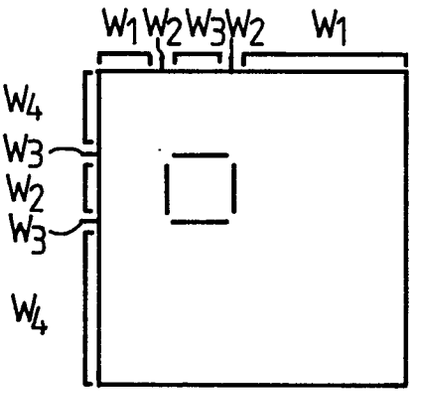



Fig. 6.

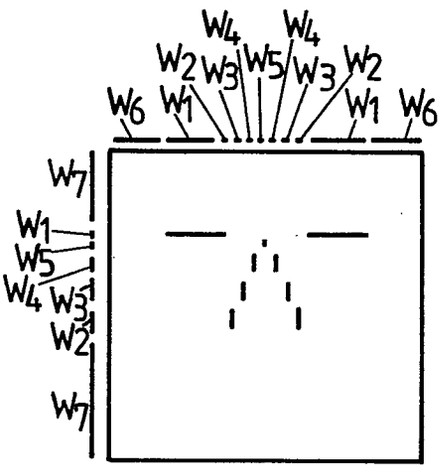



Fig. 7.

Fig.10a.

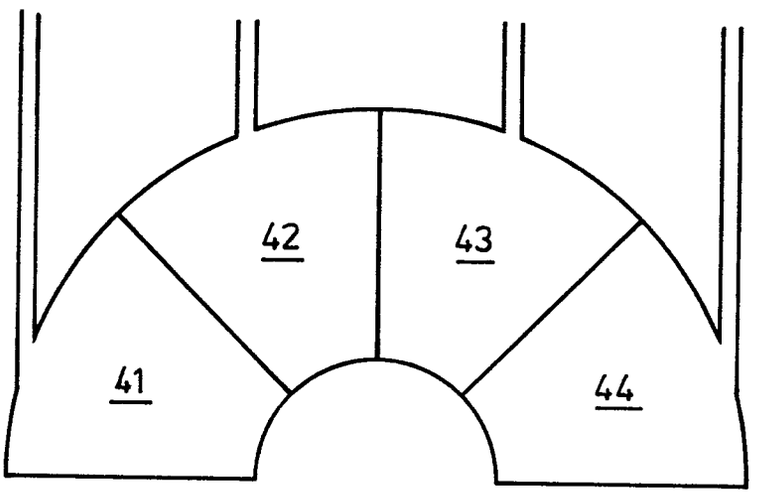
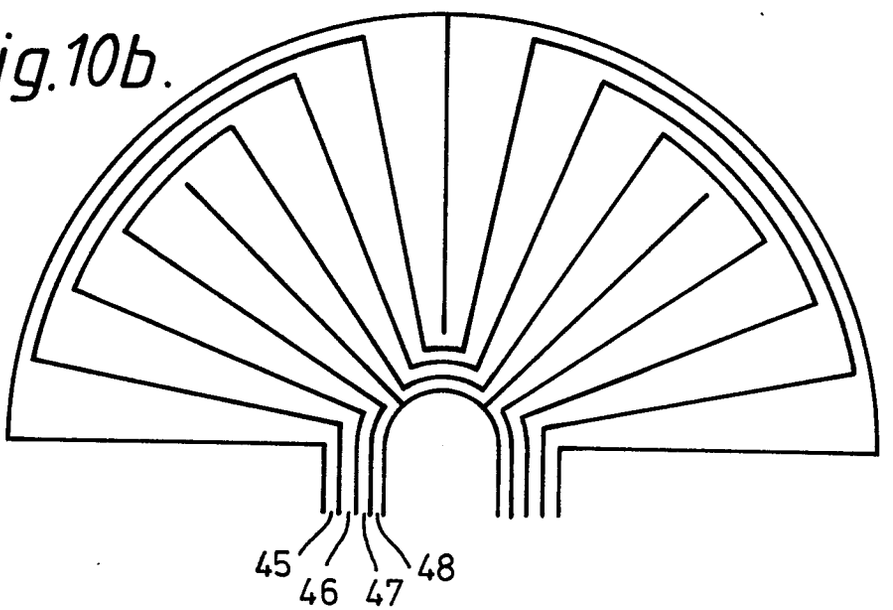



Fig.10b.



0157524

Fig.11a.

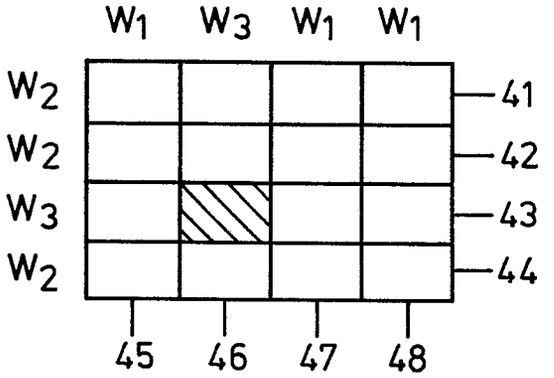



Fig.11b.

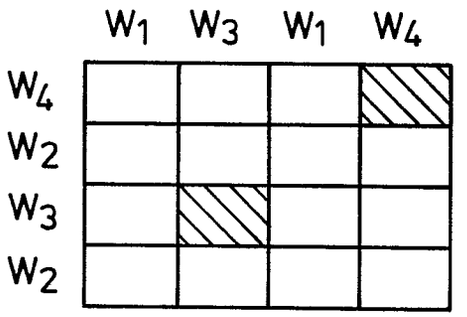



Fig.11c.

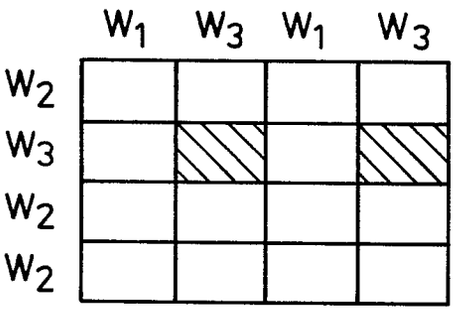



Fig.11d.