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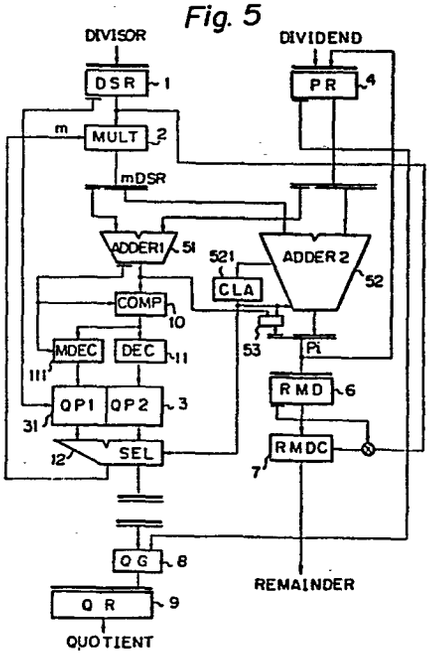
(54) Nonrestoring divider.

(57) A divider apparatus includes a divisor register (DSR) for setting a divisor, a partial remainder register (PR) for setting a dividend or a partial remainder, a predictor (QP) for predicting a partial quotient, a multiplier (MULT) for multiplying the content of the divisor register, and a first adder (ADDER 2) for subtracting the output of the multiplier from the content of the partial remainder register and for calculating the partial remainder. The apparatus further inludes a second adder (ADDER 1) for determining the difference between the upper digits of the multiplier and the upper digits of the partial remainder register, a first predictor (QP_2) for predicting the partial quotient from the output of the first adder and the upper digits of the divisor register, a second predictor (QP_1) for predicting the partial quotient in the third cycle from a corrected output of the second adder and the digits of the divisor register, a first element (CLA) for determining the carry to be propagated to the second adder from remainder digits of the multiplier and remainder digits of the partial remainder register, and a second element (SEL) for selecting either the output of the first predictor or the output of the second predictor by using the output of the first element, so that the output of the second element corresponds to a predicted quotient.

Fig. 5



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NONRESTORING DIVIDER

This invention relates to a nonrestoring divider and, more particularly, to a high speed circuit construction by which a circuit for predicting a partial quotient is formed using a smaller amount of hardware.

Conventionally, a nonrestoring divider is used as one element of a divider system. In such a system, sets of quotients used for forming digits of the quotient are controlled in such a manner that where sets of quotients exist which do not include a zero, then each digit of the quotient is selected therefrom.

These particular sets of the quotients having no zero are usually expressed as follows, wherein "r" represents the radix.

$-(r - 1), -(r - 2), \ldots, -1, +1, \ldots, r - 2, r - 1$

In many calculators, calculation is carried out by using a plurality of bit units rather than just one bit unit and, obviously, a radix larger than 2 is used.

For example, the radix is 4 in a 2 bit unit, and becomes 8 in a 3 bit unit.

Usually, an operation unit of ℓ bits is an m digit figure having r as the radix, and is expressed as;

$$r = 2^{\ell/m}$$

A characteristic feature of nonrestoring division is the use of a negative number in the digits as a result of the operation by remaining the inversion of negative and the positive of the dividend formed when the digit of the result of the operation is determined, and the dividend or multiple of the dividend is added or subtracted by the sign for the dividend by using the negative number in the result of the operation.

For example, the values multiplying the dividend by k [i.e., the multiple $-(r - 1), -(r - 2), \ldots, -1, +1, \ldots, r - 2, r - 1$] are set in the divisor registers, the

divisor registers are selected by a predicting signal output from a partial quotient predictor, and the quotient is obtained by repeatedly adding and subtracting the values multiplying the dividend by k.

In such a nonrestoring divider system, when the number of bits "n" used as the operation unit becomes large, the radix is increased, for example to 2^n, so that the number of operation repetitions can be decreased and high speed operation can be expected. However, the multiplying of the divisor becomes complex, and therefore the predicting logic for the quotient must be precise, which gives rise to the problem that the number of circuits must be considerably increased.

Concerning the logic for predicting the partial quotient, a method has not been developed for forming an effective predicting circuit for the partial quotient.

An object of the present invention is to provide a nonrestoring divider which can decrease the time needed for predicting the partial quotient.

Another object of the present invention is to provide a nonrestoring divider which can decrease the amount of hardware used for the logic needed for predicting the partial quotient.

According to the invention there is provided a divider apparatus which includes a divisor register for setting a divisor; a partial remainder register for setting a dividend or a partial remainder; a predictor for predicting a partial quotient; a multiplier for multiplying the content of the divisor register; a first adder for subtracting the output of the multiplier from the content of the partial remainder register and for calculating the partial remainder, so that the predictor predicts the partial quotient from upper digits of the divisor register and upper digits of the partial remainder, and also repeats a cycle which sets the output

of the adder at the partial remainder register so as to carry out the division, characterised by a second adder for determining the difference between the upper digits of the multiplier and the upper digits of the partial remainder register, a first predictor for predicting the partial quotient from the output of the second adder and the upper digits of the divisor register; a second predictor for predicting the partial quotient from a corrected output of the second adder and the upper digits of the divisor register; first means for determining a carry to be propagated to the second adder from the remainder digits of the multiplier and the remainder digits of the partial remainder register; and second means for selecting either the output of the first predictor or the output of the second predictor by using the output of the first means, thereby making the output of the second means correspond to a predicted quotient.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which

Figure 1 is a diagram showing the principle of one example of a conventional nonrestoring divider apparatus;

Figure 2 is a diagram showing the principle of one example of a multiplier shown in Figure 1;

Figure 3 is a diagram showing the principle of one example of a circuit for predicting a partial quotient shown in Figure 1;

Figure 4 is a diagram showing the content of the circuit for predicting a partial quotient;

Figure 5 is a block diagram of one embodiment of a nonrestoring divider apparatus according to the present invention;

Figure 6 is a diagram showing an improvement of the mutiplier shown in Figure 5;

Figure 7 is a diagram showing the content of the circuit for predicting a partial quotient shown in Figure 5;

Figures 8A and 8B are diagrams showing the logic states of the decoder shown in Figure 5; and

Figures 9A and 9B are diagrams showing another embodiment of the content shown in Figure 7.

Figure 1 is a block diagram of one example of a conventional restoring divider comprising a divisor register (DSR) 1 in which a divisor is stored and the divisor is fed to a multiplier (MULT) 2. The multiplier 2 receives a partial quotient predicting signal (hereinafter shown as "m") from a partial quotient predictor (QP) 3 and forms dividends multiplied by -15, -14, -13, ..., -2, -1, 0, +1, +2, ..., +14, +15 when the radix is 16. Note, in this circuit a method in which whole multiples are previously formed and selected, a method which uses a general adder, or a method which calculates by using a smaller number of divisor registers than the radix and multi-stage carry/save adders can be used.

In a partial remainder register (PR) 4, after the dividend is set at the first operation cycle, a new partial remainder is set at every operation cycle. A carry propagate adder (CPA) 5 carries out the addition of the partial remainder register 4 and a divisor multiplied by m ($-15 \leqq m \leqq +15$: where m is an integer), and the result thereof is output to the partial quotient register 4, the partial quotient predictor 3, and a remainder register 6.

The remainder register 6 holds the final predicted remainder for the repetition operation, and after the adding and subtracting operations are repeated, a correct quotient is output via a remainder corrector (RMDC) 7. In a concrete correcting method in the remainder corrector (RMDC) 7, when a sign bit of the remainder register (RMD) 6 is negative, the complement of 2 is determined as the quotient, and when the sign bit of the remainder register 6 is positive, the value is determined as the quotient.

A partial quotient generator (QG) 8 compares the output of the partial quotient predicting circuit (QP) 3 and the sign bit of the partial remainder register (PR) 4, so that a correct partial quotient is determined and stored in a quotient register (QR) 9.

The partial quotient predicting circuit (QP) 3, according to the present invention, calculates the value of m in m x DSR to be calculated next from the output of the carry propagate adder (CPA) 5 (hereinafter referred to as CPA) and the output of the divisor register (DSR) 1 (hereinafter referred to as DSR). Logically, the circuit (QP) 3 uses the entries in the above-mentioned CPA and DSR to retrieve the table for m.

However, when the CPA and DSR are used in this way, the table is extremely large. For example, in the nonrestoring dividing operation having a radix of 16, including the sign bit, the following table will be formed:

CPA: 6 bits (64 entries)

DSR: 9 bits (256 entries)

wherein, as shown hereinafter, it is normalized so that the most significant bit becomes 1.

Therefore, in practice, the CPA and m are used as the entry, and the DSR table is formed, in such a manner that the table is reversely retrieved. In the table mentioned above, m becomes 5 bits including the sign, CPA becomes 6 bits including the sign, and as mentioned

above, the size of the table becomes 64 x 32 entries, so that the size of the table is decreased to about 1/8. Referring to the adding and subtracting result (CPA) = 0,, the table above is almost symmetrical, and the possibility of retrenchment is included.

Figure 2 is a diagram showing the principle of the multiplier shown in Fig. 1. In Fig. 2, 11 designates multiply circuits [x(-15) ∿ x15], 12 designates divisor registers (-15DSR ∿ +15DSR), and 13 designates a selector. In the conventional system, when the radix is 16, thirty kinds of multiplier registers -15x divisor, -14x divisor, ... , -2x divisor, -1x divisor, 2x divisor, ... , 14x divisor, 15x divisor are necessary. These thirty kinds of data are formed by the multiply circuits [x(-15), ... , x15] 11, the outputs are held in the divisor registers (-15DSR ∿ +15DSR) 12, and the outputs of the divisor registers 12 are supplied to the selectors 13. In the selector 13, the values held in the registers 12 are selected by the signal m, that is, one of the multiple thirty kinds of data is selected.

Figure 3 is a diagram showing a principle of the partial quotient predicting circuit shown in Fig. 1. In Fig. 3, the six upper bits of the carry propagating adder 5 are supplied to a memory 14 as an address, and in the memory 14, the contents are divided into thirty one groups each having 9 bits, that is D_F , D_E , ... , D_O , D_{-1} , D_{-2} ... D_{-F}. The divided values D_F , D_E , ... , D_O , D_{-1} , ... , D_{-F} are supplied to comparators 15_F ... 15_O , ... 15_{-F}. Further, the upper five bits of the divisor (DSR) is supplied to other input terminals of the comparators 15_F ∿ 15_O. In the comparators 15_F ∿ 15_O , the input is formed by a 9 bit signal, the output thereof is a one bit signal. When the inputs have the relationship $A \geq B$, the output becomes "1", and when the inputs have the relationship $A < B$, the output becomes "0". In Fig. 3, 16 is a circuit for detecting "1" bit in the left most side.

Figure 4 shows a precise table which receives the CPA and m as entries and designates the DSR. The table shown in Fig. 4 has 64 x 31 entries. In Fig. 4, CPAO shows the value at which the upper 6 bits (including the sign) of CPA output are extracted and designates the decimal number, and m is the signal of the partial quotient predicting circuit (QP) 3 designated by the decimal number.

Such table look up system can be replaced by a random logic circuit which performs the same function.

The CPAO row m column in the partial quotient predicting table [QPT(CPAO, m)] designates the logical function whereby the upper 9 bits of the DSR (hereinafter referred to as DSRO) are input, and these have the value "1" or "0", (hereinafter, referred to as [LcpaO, m(DSRO)]).

For the purpose of simplifying the explanation, it is assumed that the DSR is normalized so that it is a positive integer and the most significant bit becomes 1.

First, the principle of the nonrestoring divider will be explained. When the divisor is D, the dividend is Pn, the partial remainder is Pn, and the partial remainder predicting signal is m; then the dividing operation in the nonrestoring divider is expressed by the following asymptotic equation,

$$P_{n+1} = P_n + m \times D$$

and in the n+1'th quotient Q_{n+1}, it is sufficient that the partial quotient satisfies the following condition,

$$-D < P_n + m \times D < D$$

Therefore, the logic function "LcpaO, m(DSRO)" has the following conditions.

① This logic function "LcpaO, m(DSRO)" becomes 1 when the dividing condition

$$-D < P_n + m \times D < D$$

is satisfied for all D, P which satisfy

$$DSRO \leqq D < DSRO + \delta \quad [\text{wherein } \delta = (1/2)^8]$$

$$CPAO \leqq P < CPAO + \varepsilon \quad [\text{wherein } \varepsilon = 1],$$

and this function becomes 0, except for the above,

② When the following relationship exists between m and m'

LcapO, m(DSRO) = LcpaO, m'(DSRO) = 1

wherein one is determined as "1" and the other is determined as "0".

③ The condition wherein the partial quotient predicting table formed by using the process mentioned above functions is that where one m exists for all CPAO, DSRO, and the following equation is satisfied for such an m

LcpaO, m(DSRO) = 1

This condition may be said to be "CONDITION I".

The partial quotient predicting table formed by above-mentioned method is shown in Fig. 4. In Fig. 4, when a DSRO having 9 bits is input, only one m exists for all CPAO (64 bits) and the corresponding logic function is

LcpaO, m(DSRO) = 1.

If the DSRO is 8 bits, only one m exists for all CPAO and the condition:

LcpaO, m(DSRO) = 1

is not satisfied, so that the table does not function as the partial quotient predicting table.

Further, if the DSRO is 10 bits, it becomes redundant since only one m exists for all CPAO. Therefore, when the DSRO is 9 bits, this may be said to be the most suitable number of bits in the DSRO for retrieving m in the nonrestoring divider wherein the radix is 16.

Figure 5 is a block diagram of one embodiment of the nonrestcring divider apparatus according to the present invention. In Fig. 5, the same symbols correspond to the same elements as shown in Fig. 1.

In Fig. 5, an adder 51 adds the upper bits of the partial remainder register (PR) 4 and the upper bits of output of the multiplier (MULT) 2 that is, the upper bits of mDSR without using the carry signal from an adder 52

(the output signal of the carry predicting circuit (CLA) 521), and the output thereof is supplied to a complement generator 10 and the remainder register (RMD) 6.

In the complement generator 10, when the sign bit of the adder (ADDER 1) 51 is "1", the complement of the input data (output of the adder 51) is output to the decoder 11, and when the sign bit is "0", the input data is directly output to the decoder 11.

In the decoder 11, the result obtained from the complement generator (COMP) 10 is decoded and supplied to the partial quotient predicting circuit (QP2) 3.

An adder (ADDER 2) 52 receives the lower bits of the partial remainder register (PR) 4 and the lower bits of the output (mDSR) of the multiplier (MULT) 2, and a carry look-ahead circuit (CLA) 521 is attached thereto for the purpose of carrying out high speed operations.

The output of the adder 51 is also input to a carry adding circuit 53 and compensated by the output of CLA 521 and fed to RMD6 by being concatinated with the output of adder 52.

The characteristic feature of the present invention is to provide new functional blocks, that is, a modified decoder circuit (MDEC) 111, a selector (SEL) 12, and a partial quotient predicting circuit (QP1) 31 having the same function as that of the partial quotient predicting circuit (QP) 3 explained in Fig. 1 to Fig. 4.

The basic operation of the apparatus shown in Fig. 5 is similar to the conventional system, therefore, only the characteristic feature of the present invention will be explained hereinafter.

First, the modified decoder circuit (MDEC) 111 forms, in principle, the decode signal assuming +1 when the sign bit of the adder (ADDER 1) 51 is "0" (positive) and the decode signal assuming -1 when the sign bit of the adder 51 is "1" (negative). The selector 12 selects either the partial quotient predicting circuit (QP1) 3

or (QP2) 31 by using the output signal of the carry predicting circuit (CLA) 521.

Concretely, when the output of the carry predicting circuit (CLA) 521 is "1" (that is, a carry exists), the selector 12 selects the partial quotient circuit (QP1) 31, and where the output of the circuit (CLA) 521 is "0" (that is, no carry exists), the partial quotient circuit (QP2) 3 is selected. The function of the modified decoder circuit (MDEC) will be explained in detail later referring to Figs. 8A and 8B.

Figure 6 is a block diagram of another embodiment of the present invention.

In Fig. 6, 22 designates multipliers ($\pm$1x, $\pm$2/$\pm$4x, $\pm$8/$\pm$16x) which are formed by a complement circuit and a shifter, wherein multiplication in the + side is achieved by shift only and multiplication in the - side is achieved by using the complement; 23 designates divisor registers (SR #1, SR #2, SR #3); 24 and 25 carry save adders (CSA1, CSA2) having three inputs; C designates a carry signal; and S designates a sum signal.

In the circuit shown in Fig. 6, the divisor registers 23 [corresponding to (+15DSR ∿ -15 DSR) in Fig. 2] are formed by three registers (SR #1 ∿ SR #3) the number of which is smaller than the number of bits (4), and the outputs of four registers SR #1, SR #2, SR #3 and the partial remainder register(PR) 4 are added by using two carry/save adders 24, 25 having three inputs.

When the divisor is set in the divisor register (DSR) 1 and the dividend is set in the partial remainder register (PR) 4, the dividend is supplied via the three-input carry/save adder (CSA 2) 25 to the partial quotient predicting circuit (QP) 3, and a signal predicting the most significant digit of the quotient is output. This predicting signal selects a plurality of routes by which the output of the divisor register 1 is multiplied by the adders 22 ($\pm$1x, $\pm$2/$\pm$4x, $\pm$8/$\pm$16x), and the outputs thereof are set in the divisor registers (SR #1, SR #2,

SR #3) 23.

Next, the outputs of the divisor registers (SR #1, SR #2, SR #3) 23 and the output of the partial remainder register (PR) 4 are added by using the three-input carry/save adders (CSA1, CSA2) 24, 25 and the carry propagation adder 5, and the output thereof is again input to the partial remainder register (PR) 4.

The output (C, S) of the three-input carry/save adder (CSA2) 25 is supplied to the partial quotient predicting circuit (QP) 3, so as to determine the inputs of the three kinds of divisor registers (SR #1, SR #2, SR #3) which will be selected next.

Fig. 7 is a diagram showing one embodiment of the partial quotient predicting table according to the present invention.

First, the concept of the present invention will be explained. At the i'th step of the non-restoring division, the following equations are used.

$$P_{i+1} = p_i - m_i \times d \qquad (1)$$

$$-d < P_{i+1} < d \qquad (2)$$

wherein pi designates a partial remainder, d is a divisor, r is a radix, and when the radix is r, mi is expressed as

$$-r + 1 \leq m_i \leq r - 1$$

The value m_i is selected so that the value of P_{i+1} obtained by calculating the equation (1) satisfies the equation (2), and the equation (1) is calculated by using the selected m_i.

In the actual computer, at the best case, the upper bits of p_i and d [corresponded to P_i in CPA and D in DSR] are extracted by digits sufficient to ensure accuracy in determining m_i , the value of m_i is determined by using the partial quotient predicting table, and thereafter precise P_{i+1} is calculated by using equation (1).

As an operation for $m_i \times d$, a method for using the multiplier, a method for using a divisor register at

every multiple, a method for using carry/save adders, etc., are well known and the subtraction $p_i - m_i \times d$ is carried out by using a well known adding and subtracting circuit, etc.

The feature of the present invention lies within the carrying out of the function of determining m_i which satisfies the equation (2) from P_i and D above by using the smallest possible amount of hardware.

As mentioned above, when P_i , D are fixed, a plurality values of m_i exist which satisfy the equations (1), (2) at the same time.

When the quotient sets in the nonrestoring divider is x [= (-r, -r + 1, ... , -1, 0, 1, ... , r - 1 , r) wherein r is a radix], the set $M(P_i , D)$ of m_i , which satisfies the equations (1), (2) at the i'th step, is a partial set of X, and usually a plurality of elements exist. That is,

$$M(P_i , D) \subset X \qquad (3)$$

Wherein N is specified as the mapping which is mapped from the partial set X and in which the sign of each element is inverted. That is, when

$$A \subset X, \ B \subset X,$$

then

$$[N(A) = B] \overset{+}{\div} [x \in A \overset{+}{\div} -x \in B \text{ for all x's}]$$

When the complement of P_i is shown by $\bar{P}_i$, $M(P_i , D)$, $N[M(P_i , D)]$ have a common portion, but they are not coincident. That is, generally,

$$M(P_i , D) \neq N[M(\bar{P}_i , D)] \qquad (4)$$

$$M(P_i , D) \cap N[M(\bar{P}_i , D)] \neq \phi \qquad (5)$$

In the above mentioned equation, when the common portion is set as M',

$$M'(P_i , D) = M(P_i , D) \cap N[M(\bar{P}_i , D)]$$

In other words, when $P_i \geq 0$, a suitable mi is determined by selecting one element from $M'(P_i , D)$, and when $P_i < 0$, a suitable m_i is determined by selecting one element from $N[M'(P_i , D)]$.

Therefore, when the system of the present invention

is used, the table which determines m_i from any P_i and D is provided only for $P_i \geq 0$, so that the size of the table can be reduced by about one-half.

The above-mentioned will be explained by using the example of the nonrestoring division by which the quotient having 4 bits (that is radix r = 16) is obtained in one cycle time (one step).

When r = 16, for the purpose of determining m_i, P_i requires 6 bits including the sign and D requires 9 bits (however, for the purpose of simplicity, it is previously normalized so that D is positive and the most significant bit is "1").

Further, the following relationship exists between the accuracies of the P_i, D mentioned above. That is, when one is rough, the other requires high accuracy. The above relationship, that is, P_i = 6 bits and D = 9 bits, is one combination relating to that relationship.

As a concrete example of the P_i and D mentioned above, when

P_i = 001011 (upper 6 bits)

D = 110000000 (upper 9 bits)

it is known that in the value of m_i which satisfies the above equations (1), (2), two values exist, that is, 7 and 8. That is,

$$M(P_i, D) = \{7, 8\},$$

and similarly, it is known that

$$M(\bar{P}_i, D) = \{-8\}$$

Then, from the definition of the mapping mentioned above, it may be said that

$$N[M(\bar{P}_i, D)] = \{8\}$$

and

$$M(P_i, D) \neq N[M(\bar{P}_i, D)]$$

and further

$$M'(P_i, D) = M(P_i, D) \subset N[M(\bar{P}_i, D)] = \{8\}$$

If, by providing the table of $M'(P_i, D)$, the upper bits P_i of the input P_i are

"001011" = $(P_i)_a$ (that is $P_i \geq 0$)

P_i is

$$P_i = (P_i)_a$$

therefore,

$$M(P_i , D) = M[(P_i)_a , D] = \{7, 8\}$$

and $M'((P_i)_a , D) = M'(P_i , D) = \{8\}$

and then, if

$$M(P_i , D) \supset M'(P_i , D) = \{8\}$$

therefore,

$$M(P_i , D) \ni 8$$

Similarly, when

'110100' = $(P_i)_b$ (that is, $P_i < 0$),

if $\bar{P}_i$ is set as

$$\bar{P}_i = (P_i)_b$$

it becomes

$$\overline{(P_i)_b} = P_i = \text{'001011'} = (P_i)_a$$

and $M'((P_i)_b , D) = M'(\bar{P}_i , D)$

On the other hand,

$$N[M(\bar{P}_i , D)] \supset M'(P_i , D) = \{8\}$$

therefore,

$$N[M(\bar{P}_i , D)] \ni 8$$

Accordingly, in accordance with the definition of the mapping, the following relationship can be obtained:

$$M[(P_i)_b , D] = M(\bar{P}_i , D) \ni -8$$

Also, when $P_i < 0$, the same result as that calculated above is obtained by the table of $M'(P_i , D)$. Therefore, it is known that the correct result can be obtained even if such a table is used.

To summarize the above-mentioned explanation concerning the concept of the present invention, the following relationship exists between the partial sets $M(P_i , D)$ and $M(\bar{P}_i , D)$ of the quotient set X,

$$M(P_i , D) \neq N[M(\bar{P}_i , D)]$$

$$M(P_i , D) \cap N[M(\bar{P}_i , D)] = M'(P_i , D) \neq \phi$$

and,

$$M'(P_i , D) \subset M(P_i , D)$$

$$M'(P_i , D) \subset N[M(\bar{P}_i , D)]$$

Therefore, when set as $M'(P_i , D) \ni a$,

it becomes

$$M(P_i , D) \ni a$$
$$N[M(\bar{P}_i , D)] \ni a,$$

that is,

$$M(\bar{P}_i , D) \ni -a$$

Thus, the elements of the partial sets $M(P_i , D)$, $M(\bar{P}_i , D)$ can be obtained by providing one table of $M'(P_i , D)$.

Figure 7 shows the table in which the relationship between P_i, D, and m_i is obtained by using the above-mentioned principle.

In Fig. 7, m_i is 4 bits, P_i is 5 bits without a sign, D is 9 bits (however, it is normalized so that the most significant bit becomes "1"), and several discontinuous points exist therebetween. However, it is known that a comparative continuous relationship exists, that is, when D increases, m_i decreases.

As mentioned above, the process for determining m_i logically corresponds to the retrieval of the table which uses P_i and D as entries to determine the value of m_i. As P_i becomes 6 bits including the sign, a table must be formed having 64 entries x 256 entries, and this is not practical.

Therefore, it is considered that the construction of the table which uses P_i, m_i as entries and the range for D as elements as shown in Fig. 6 is the most efficient.

In the table shown in Fig. 7, the upper 5 bits of P_i are designated as a hexadecimal number, the 4 bits of m_i are designated as a hexadecimal number, and the upper 9 bits (wherein the most significant bit is "1") of D are designated as a hexadecimal number. The upper 9 bits of D designates a lower limit value for the elements entry.

Therefore, when the elements of the table are

$$T_{pi} , m_i$$

the range of D which satisfies the following relationship

$$M'(P_i , D) \ni m_i$$

is determined by following:

$$T_{Pi}, m_i \leqq D \leqq T_{Pi}, m_{i-1} - 1$$

As a concrete example, when P_i = '001011' is designated as a hexadecimal number without a sign, it becomes '0B'(H), and similarly, D = '110000000' becomes '180'(H). Therefore, in the table, as

T'0B', 8 $\leqq$ D $\leqq$ T'0B', 7-1 (shown by thick line frame)

and referring to the following relationship

$$160_H \leqq 180_H \leqq 18F_H$$

it is known that the value to be determined is '8'.

When the following relationship is given

$$P_i = (P_i)_b = \text{'110100'}$$

the sign is negative, so that '001011' is obtained as the complement of $(P_i)_b$. Therefore, 0B' excepting the sign can be designated as a hexadecimal number, and the entry is the same as mentioned above, and thus $m_i = 8$ is obtained. Finally, the sign is adjusted, and '-8' is obtained as a true predicting partial quotient.

Fig. 8A shows one example of the function of the usual decoder (DEC) 11 shown in Fig. 5 and the function of the modified decoder (MDEC) 111 shown in Fig. 5.

The example of the operation of the invention by which the partial quotient predicting signal m is output when the output data of the adder 51 [that is, the upper digit of PR_i + mDSR] is positive and negative.

[Example 1]

When the output data of the adder 51 is '00100' the sign bit of the data is "0" (positive). Therefore a carry is not input from the carry predicting circuit 521, and the output of the decoder 11 [that is the decoded output which makes the line 4 (see Fig. 8A) to an ON state, shown by (1) in Fig. 8A] is supplied to the partial quotient predicting circuit 3. When the obtained partial quotient predicting signal has a carry, it is predicted that the above-mentioned data will become '00101' and the sector 12 exerts a control through the

carry from the carry predicting circuit 52 so that the output of the decode circuit input as '00100' including the sign [shown in ② in Fig. 8B, that is, the output which places the line 5 (see Fig. 8B) to an ON state] is supplied to the modified decoder 111, and the input partial quotient predicting signal is supplied to the partial quotient predicting circuit 31. Thus, the correct partial quotient predicting signal m is obtained.

[Example 2]

When the output data of the adder 51 is '11011', the sign bit of the data is "1" (negative). Therefore, according to the logic disclosed in the prior Japanese Unexamined Application No. 59-070353, the output of the adder 51, that is the complemental output of "1", is supplied to the decoder circuits 11 and 111, and the absolute value of the partial quotient predicting signal m is output.

Therefore, in this case, if no carry from the carry predicting circuit 521 exists, the complement of 1 of the data '1011' excepting the sign is '0100'. Then the output [shown in ① on Fig. 8A, that is, the decoded output which places the line 4 to an ON state] of the decoder 11 corresponding to the complemental output is supplied to the partial quotient predicting circuit 3. When the output of the partial quotient predicting circuit 3 includes a carry, the original data becomes '11100' and then it is predicted that the complemental output will become '0011'. Then the selector 12 exerts control through the carry from the carry predicting circuit 521 so that the output of the decode circuit input as '10100' including the sign [shown in ③ on Fig. 7B, that is, the output which places the line 3 to an ON state] is supplied to the modified decoder 111 and the input partial quotient predicting signal is supplied to the partial quotient predicting circuit 31. Thus, the correct partial quotient predicting signal m is obtained.

As mentioned above, the characteristic feature is that, the modified decoder 111 forms the decode signal predicting +1 when the sign bit of the adder 51 is principally "0" positive, and forms the decode signal predicting -1 when the sign bit thereof is "1" (negative).

Figures 9A and 9B are an alternative to the example shown in Fig. 7.

In the table shown in Fig. 4, the CPAO is 6 bits (64 entries), the obtained m is 5 bits including the sign (32 entries), and the radix is 16. However, also when m is 4 bits including the signal (expressed by m1), $\delta = (1/2)^5$ [that is, the table is formed by inputting the upper 6 bits (DSR1) of the DSR] and $\varepsilon = 2$ [the CPA is 4 bits (CPA1) including the sign], the table which satisfies the table shown in Fig. 4, (that is, the CONDITION I above) can be obtained.

This table is a rough portion of quotient predicting table shown in Fig. 9A.

When the table is as shown in Fig. 9A and as shown in Fig. 4, the following can be known. That is, even when the portion corresponding to add number m in the precise portion of the partial quotient predicting table shown in Fig. 4 is "1", the value m1 smaller by "1" than in the table shown in Fig. 4 is obtained in the table shown in Fig. 9A.

Therefore, for the purpose of correcting the error in both cases, when "1" exists in the portion for the odd number m in the table shown in Fig. 4, the precise m can be obtained by storing its information as another correcting table and by referring to the same. Figure 9B is a table which schematically shows the above mentioned correcting table.

Hereinafter, the correcting method will be concretely explained.

First, referring one column CPA1 = -30 in the rough portion of the quotient predicting table, when,

for example,

L' -30, -14 = 1

and, in the correcting table, the corresponding column (that is, CPA2 = -30) is

L" -30 = 1

the correction is carried out to the value corresponding to the odd number m (that is, m = -13), that is

L' -30, -13 = 1.

When the corrected value in the same column is

L" -30 = 0

this shows that "1" does not exist at any portion for the odd number m for CPA0 = -30. Therefore, in the rough portion of quotient predicting table, for example,

L' -30, -14 = 1

is used as it stands as the precise portion of quotient predicting table.

Further, when in one column in CPA1 = -30 in the rough portion of the quotient predicting table, for example,

L' -30, -14 = 1

and in the column in CPA2 = -29 in the correcting table,

L" -29 = 1,

the correction is carried out to the value corresponding to the odd number m (i.e., corresponding to m = -13), that is

L' -29, -13 = 1.

That is, when L" -30 = 1 in the correcting table, it shows that, in the column corresponding to CPA0 = -30 in the precise portion of quotient predicting table shown in Fig. 4, one "1" exists at any portion for the odd number m. This is retrieved from the rough portion of quotient predicting table shown in Fig. 9A, and when as mentioned above,

L' -30, -14 = 1

it is determined that

L' -30, -13 = 1.

This is the gist of the present invention.

Therefore,

$$L' -30, -12 = 1$$

it becomes

$$L' -30, -11 = 1$$

and subsequent same operations are repeated.

The above-mentioned correcting table is formed by the above-mentioned condition, and each element thereof is expressed by the following equation.

$$L"cpa2, m2(DSR2) = \Sigma Lcpa2, 2i+1(DSR2) = 1$$

wherein Σ shows the logical sum from $i = -8$ to $i = +7$, cpa2 is the upper 6 bits including the sign in the output of the carry propagate adder, and DSR2 is the upper 9 bits of the dividend.

The correcting table formed by the equation showing the condition mentioned above is shown in Fig. 9B.

According to the present invention, the same function as shown in the precise portion the quotient predicting table shown in Fig. 4 can be realized by the rough portion of the quotient predicting table shown in Fig. 9A and the correcting table shown in Fig. 9B, so that it is recognized that the amount of hardware needed can be decreased.

In the explanation above, CPA and m are used as the entry of the partial quotient predicting table, however, m can be placed to the value coded by using a plurality of desired values from -16 to +15, to form an effective signal in the subsequent process.

CLAIMS

1. A divider apparatus including a divisor register (DSR) for setting a divisor; a partial remainder register (PR) for setting a dividend or a partial remainder; a predictor (QP) for predicting a partial quotient (m); a multiplier (MULT) for multiplying the content of the divisor register (DSR); and a first adder (ADDER 2) for subtracting the outout of the (MULT) from the content of the partial remainder register (PR) and for calculating the partial remainder, so that the predictor (QP) predicts the partial quotient (m) from upper digits of the divisor register (DSR) and upper digits of the partial remainder, and repeats a cycle which sets the output of the adder at the partial remainder register (PR) so as to carry out the division; characterised by a second adder (ADDER 1) for determining the difference between the upper digits of the multiplier and the upper digits of the partial remainder register; a first predictor (QP_2) for predicting the partial quotient (m) from the output of the second adder (ADDER 1) and the upper digits of the divisor register (DSR); a second predictor (QP_1) for predicting the partial quotient (m) from a corrected output of the second adder (ADDER 1) and the upper digits of the divisor register (DSR); first means (CLA) for determining a carry to be propagated to the second adder (ADDER 1) from remainder digits of the multiplier (MULT) and remainder digits of the partial remainder register (PR); and second means (SEL) for selecting either the output of the first predictor (QP_1) or the output of the second predictor (QP_2) by using the output of the first means (CLA)), thereby making the output of the second means (SEL) correspond to a predicted quotient.

2. Apparatus according to claim 1, characterised in that the first predictor (QP_1)/second predictor (QP_2)

output positive partial quotient (m) when the output of the second adder (ADDER 1) is positive, and a negative partial quotient (m) when the output of the second adder is negative, and feed the quotient correcting circuit (QG) which corrects the predicted m by using the sign of the partial remainder formed by the partial quotient so as to determine a true value of the quotient.

3. Apparatus according to claim 2, characterised in that the first predictor (QP_1)/second predictor (QP_2) respectively comprise a circuit (COMP) by which when the output of the second adder (ADDER 1) is + (or -), the value is not changed and when the output of the second adder is - (or +), the complemental value is determined; a circuit for determining the partial quotient (m) from the output of the complemental value determining circuit (COMP) and the upper digits of the divisor register (DSR); and a circuit for compensating the partial quotient (m) by the sign of the output of the second adder.

4. Apparatus according to claim 3, characterised in that the circuit for determining the partial quotient further comprises means for outputting partial bits of the partial quotient by using partial bits of the output of the complemental value determining circuit (COMP) and means for outputting remainder bits of the partial quotient by using whole bits of the output of said determining circuit (COMP).

5. Apparatus according to claim 2, characterised in that the first predictor (QP_1)/ second predictor (QP_2) comprise means for outputting partial bits of the partial quotient by using partial bits of the output of the second adder (ADDER 1) and means for outputting remainder bits of the partial quotient by using whole bits of the output of the second adder.

6. Apparatus according to any one of claims 1 to 5, characterised in that the multiplier comprises a shift circuit which generates the values multiplying the value of the divisor register by ±1, ±2, ±4, ...$\pm 2^i$; means for selecting the combination of the multiples in accordance with the value of the partial quotient; and an adder for adding the selected multiples.

Fig. 1

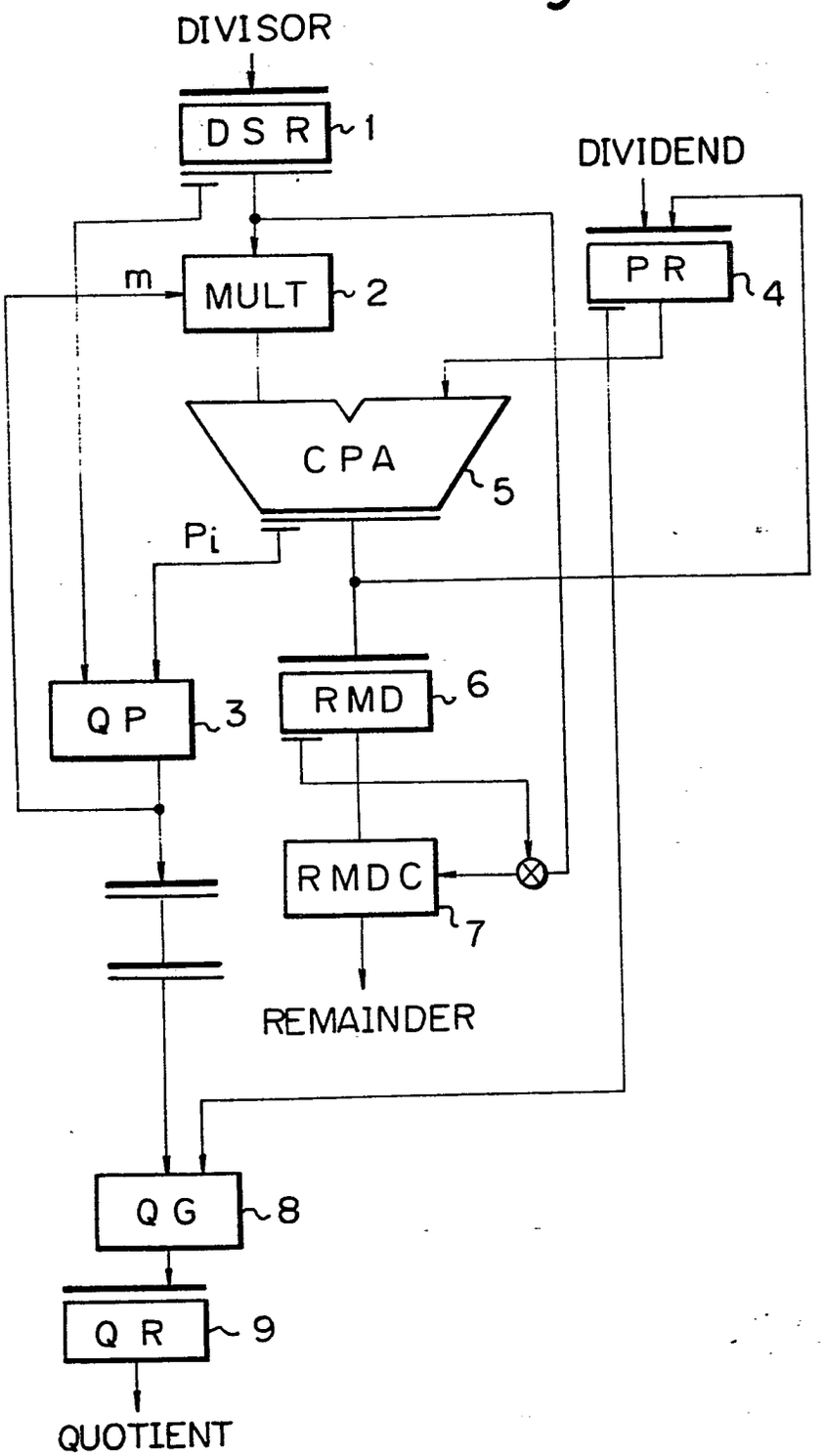

DIVISOR
DSR
1
DIVIDEND
m
MULT
2
PR
4
CPA
5
Pi
QP
3
RMD
6
RMDC
7
REMAINDER
QG
8
QR
9
QUOTIENT

Fig. 2

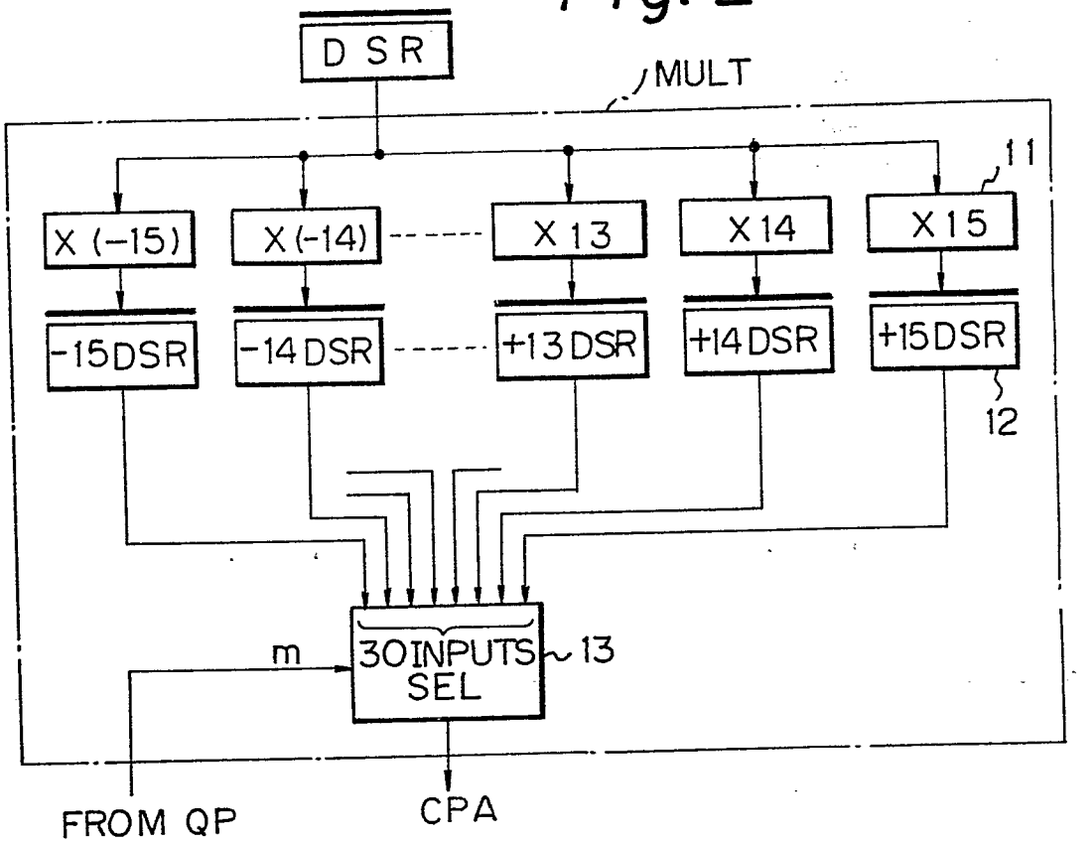

D S R
MULT
11
X (−15)
X(-14)
X 13
X 14
X 15
-15DSR
-14 DSR
+13 DSR
+14 DSR
+15DSR
12
m
30INPUTS SEL
13
FROM QP
CPA

Fig. 3

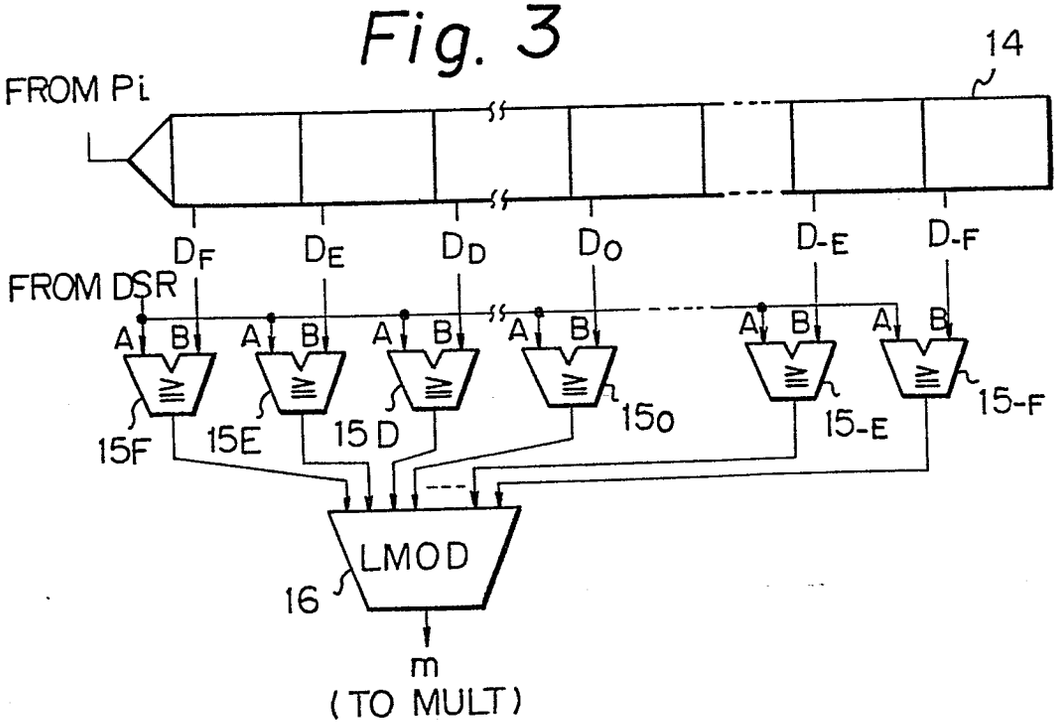
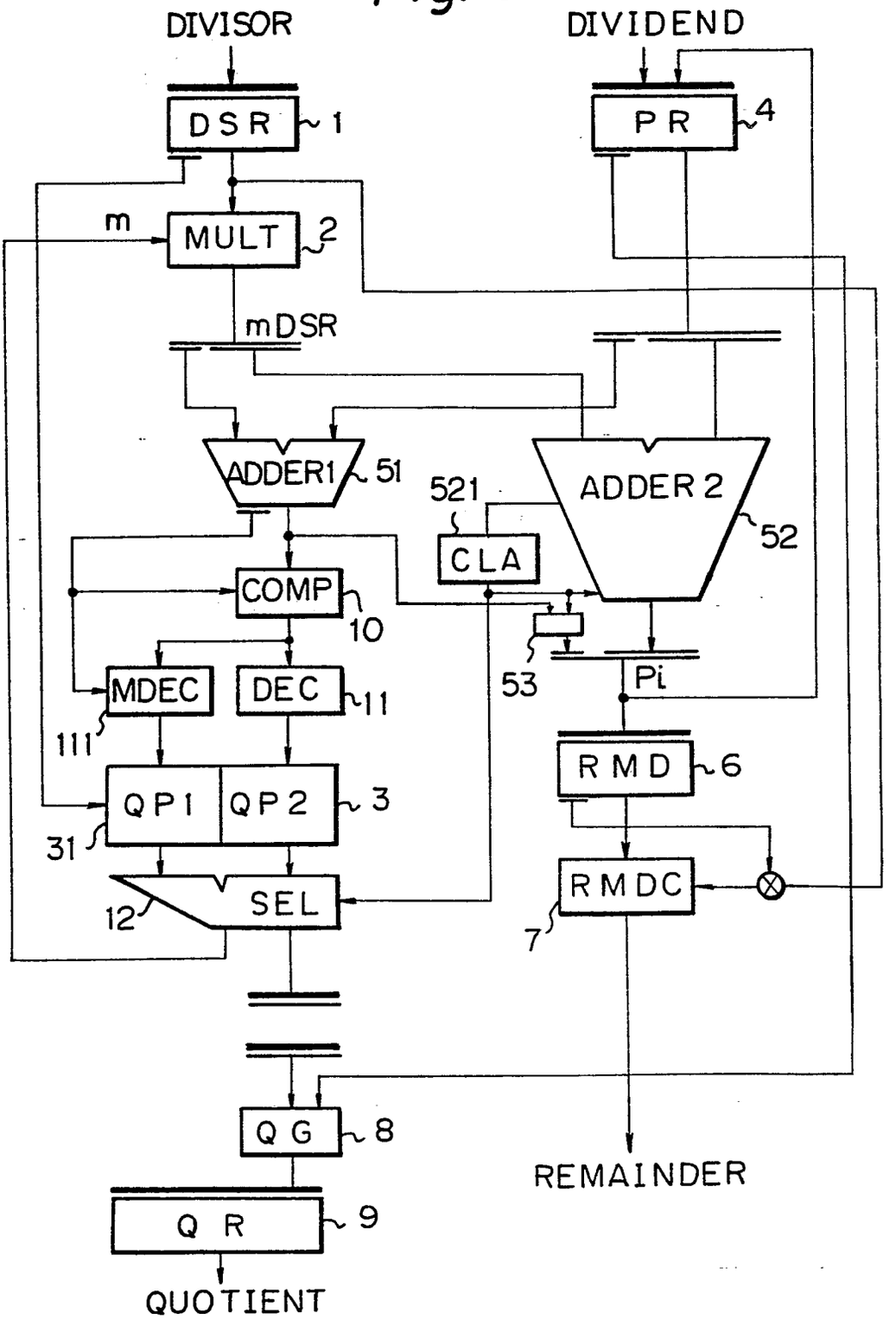

14
FROM Pi
D_F
D_E
D_D
D_O
D-E
D-F
FROM DSR
A
B
15F
15E
15 D
15o
15-E
15-F
LMOD
16
m
(TO MULT)

Fig. 4

CPAO \ m	− 15	− 14	− 13	+14	+15
− 32	L-32,-15	L-32,-14	L-32,-13	L-32,-14	L-32,15
− 32	L-31,-15	L-31,-14	L-31,-13		
− 30	L-30,-15	L-30,-14	L-30,-13		
− 29	L-29,-15	L-29,-14	L-29,-13		
− 28					
− 3	L-3,-15	L-3,-14	L-3,-13		
− 2					
− 1					
0					
+ 1					
+ 2					
+ 29					
+ 30					
+ 31	L31,-15	L31,-14	L31,-13	L31, 14	L31, 15

Fig. 5


DIVISOR
DIVIDEND
DSR
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PR
4
m
MULT
2
mDSR
ADDER1
51
521
ADDER 2
52
CLA
COMP
10
53
Pi
MDEC
DEC
11
111
RMD
6
QP1
QP2
3
31
RMDC
SEL
12
7
QG
8
REMAINDER
QR
9
QUOTIENT

Fig. 6

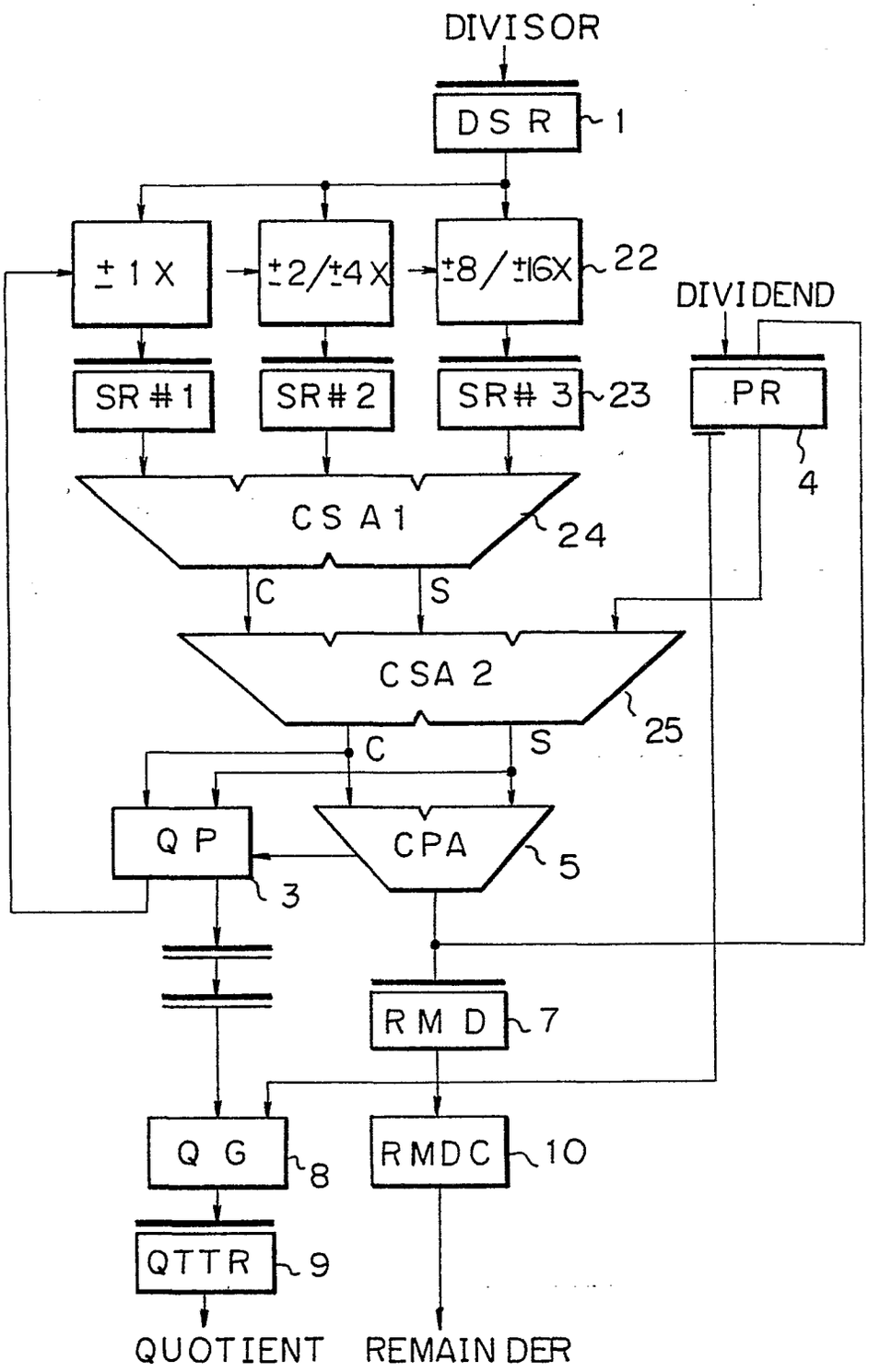
DIVISOR
DSR
1
±1X
±2/±4X
±8/±16X
22
DIVIDEND
SR#1
SR#2
SR#3
23
PR
4
CSA1
24
C
S
CSA2
25
C
S
QP
3
CPA
5
RMD
7
QG
8
RMDC
10
QTTR
9
QUOTIENT
REMAINDER

Fig. 7

Pi \ mi	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0 0																100
0 1															100	
0 2														100		
0 3													100	180		
0 4												100	150			
0 5											100	140	1A0			
0 6										100	130	180				
0 7									100	128	160	100				
0 8								100	124	150	190					
0 9							100	120	148	180	1C0					
0 A						100	11C	140	168	1A0						
0 B					100	118	138	[160]	190	1C0						
0 C				100	116	130	150	180	180							
0 D			100	114	12C	148	170	1A0	1D0							
0 E		100	113	128	144	160	188	1C0								
0 F	100	112	126	140	158	180	1A0	1E0								
1 0	100	124	138	150	172	190	1C0									
1 1	100	134	14C	168	188	180	1E0									
1 2	100	148	160	180	1A0	1C0										
1 3	100	158	170	190	1B0	1E0										
1 4	100	168	188	1A0	1D0											
1 5	100	180	198	1C0	1E0											
1 6	100	190	1B0	1D0												
1 7	100	1A0	1D0	1E0												
1 8	100	1B0	1D0													
1 9	100	1C0	1E0													
1 A	100	1D0														
1 B	100	1E0														
1 C	100															
1 D	100															
1 E	100															
1 F	100															

Fig. 8A

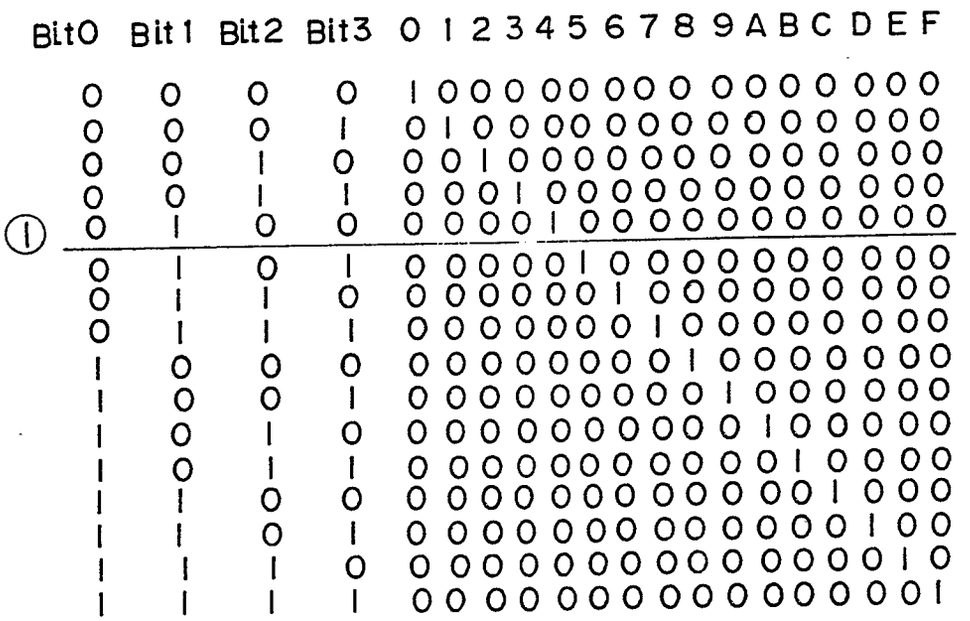

Fig. 8B

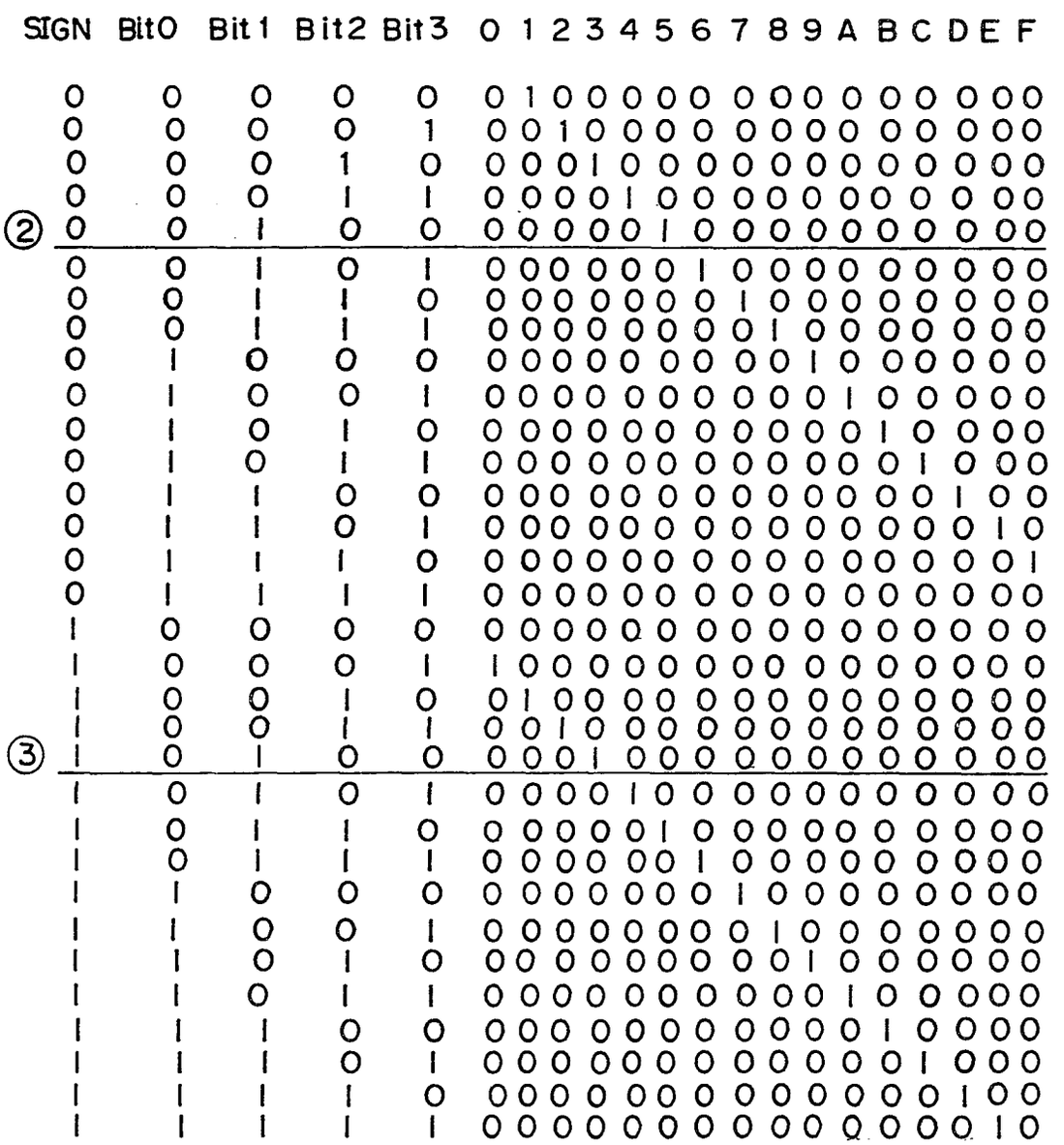

Fig. 9A

CPA1 \ mi	− 16	− 14	− 12		+ 12	+ 14
− 32	L'-32;16	L'-32,-14	L'-32;-12		L'-32;12	L'-32, 14
− 30	L'-30,-16	L'-30,-14	L'-30,-12			
− 28	L'-28;16					
− 2	L'-2,-16					
0	L' 0,-16					
+ 2	L' 2,-16					
+ 28	L'28;16					
+ 30	L'-30,-16					

Fig. 9B

CPA 2 \ m 2	+ 1
- 32	L″ - 32
- 31	L″ - 31
- 30	L″ - 30
− 2	L″ - 2
− 1	L″ - 1
0	L″ 0
+ 1	L″ 1
+ 30	L″ 30
+ 31	L″ 31