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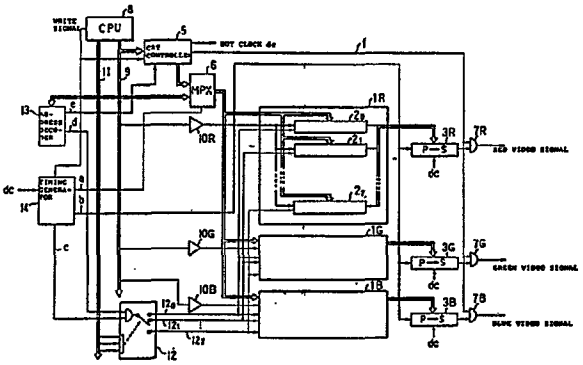
(54) **APPARATUS FOR CONTROLLING WRITING AND READING IN RELATION TO GRAPHIC MEMORY.**

(57) Apparatus for controlling writing and reading in relation to graphic memories (1R, 1G, 1B) for a red screen, a green screen and a blue screen, respectively, each of the graphic memories having a capacity of N × M bits. The apparatus operates in such a manner that data is written into the graphic memories (1R, 1G, 1B) bit by bit and is read out therefrom in units of M bits. The apparatus is capable of modification of one bit per cycle of a CPU (8) with a reduced number of hardware elements. Each of the graphic memories (1R, 1G, 1B) is constituted by an M-bit output RAM group consisting of M 1-bit output RAMs ($2_0$ to $2_7$) each having a capacity of 1 X N bits. Further, the same address space is allotted to the graphic memories (1R, 1G, 1B), and 1-bit data lines of a data bus (9) of the CPU (8) are respectively connected to all the RAMs ($2_0$ to $2_7$) in each of the graphic memories (1R, 1G, 1B). The writing of data, which is effected bit by bit, is carried out in such a manner that one bit of each of the RAMs ($2_0$ to $2_7$) in each of the graphic memories (1R, 1G, 1B) is specified by the CPU address, and a write signal is delivered to any of the desired M RAMs ($2_0$ to $2_7$) with a part of the CPU address.




EP 0 161 319 A1

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# S P E C I F I C A T I O N

## WRITE/READ CONTROL UNIT FOR GRAPHIC MEMORIES

### TECHNICAL FIELD

The present invention relates to a write/read control unit for a graphic memories in a color graphic display.

### BACKGRAOUND ART

In general color graphic displays, since one bit of a graphic memory corresponds to one picture element on the display screen, the preparation of graphic data in the graphic memory calls for a bitwise data write. Conventionally, this bitwise processing is accomplished by such methods as follows:

1) A processor (CPU) reads out data from the graphic memory byte by byte, modifies the concerned bit in the byte and writes the data again into the graphic memory byte by byte.

2) Hardware commonly referred to as a bit operation circuit is provided between the CPU and the graphic memory for effecting the read, modification and write mentioned above in 1).

However, the method 1) is small in the amount of hardware required but needs at least two cycles of operation of the CPU for the one-bit write, and hence has the defect of low processing speed. The method 2) permits the modification of one bit in one cycle of the CPU but requires very complex hardware, and hence is costly.

## DISCLOSURE OF THE INVENTION

An object of the present invention is to make it possible to modify one bit in one cycle of the CPU simply by the additional provision of a small amount of hardware.

Briefly stated, the graphic memory write/read control unit according to the present invention writes data, bit by bit, into graphic memories for red, green and blue pictures, each having a capacity of N × M bits, and reads out data therefrom in units of M bits. The graphic memories for red, green and blue pictures each comprise an RAM group of an M-bit output which includes M RAMs each having a one-bit output and a 1 × N bit capacity. The graphic memories for red, green and blue pictures are assigned the same address spacer, and different one-bit data lines of a data bus of the CPU are connected to all the RAMs of the graphic memories for red, green and blue pictures. The aforementioned bitwise data write is effected specifying one bit of each RAM of each graphic memory by a CPU address and by sending a write signal to an arbitrary one of the M RAMs by a part of the CPU address.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram illustrating the principal part of an example of the hardware structure of the write/read control unit according to the present invention; Figs. 2 and 3 are diagrams showing the relationships between respective areas of RAMs $2_0$ to $2_7$ and display positions on

the display screen; Fig. 4 is a diagram showing examples of signal waveform occurring at respective parts in Fig. 1; Fig. 5 is a folwchart showing an example of processing by a CPU 8 for writing graphic data into graphic memories 1R, 1G and 1B; Fig. 6 is a diagram showing an example of the data format of the CPU; and Fig. 7 is a block diagram illustrating an embodiment of a timing gererator 14.

BEST MODE FOR CARRYING OUT THE INVENTION

In Fig. 1, reference numeral 1R indicates a graphic memory for a red picture, 1G a graphic memory for a green picture and 1B a graphic memory for a blue color, each of which is provided with eight RAMs $2_0$ to $2_7$ each having a capacity of 1 × N bits. These graphic memories have the same address space. In Fig. 1 only the graphic memory 1R for a red color picture is shown to have the eight RAMs $2_0$ to $2_7$ for convenience sake, but the other graphic memories 1R and 1B also have the eight RAMs. The outputs of the graphic memories 1R, 1G and 1B are eight-bit, that is, one bit is o obtained from each of the RAMs $2_0$ to $2_7$ and a total of eight bits are set in each of shift registers 3R, 3G and 3B. For example, if the respective output bits of the RAMs $2_0$ to $2_7$ are numbered, as shown in Fig. 2, then each of a total of 8 × N bits corresponds, on a display screen 4, to one of areas shown in Fig. 3, for instance. The reason for this is as follows: Bits (for example, 0 to 7, 8 to 15, etc.) at the same locations in the RAMs $2_0$ to $2_7$ are read out by one of addresses for display which are applied via multiplexer 6

from a CRT controller 5, and the eight bits are simultaneously set in each of the shift registers 3R, 3G and 3B and then input as red, green and blue video signals, in the form of serial data, by a dot clock dc (the frequency of which is eight times higher than that of a clock for counting up a display address counter) from the CRT controller 5, via AND circuits 7R, 7G and 7B into a CPU not shown. Incidentally, a signal f input into each of the AND circuits 7R, 7G and 7B from the CRT controller 5 is a signal which is a "0" only during the horizontal flyback period and is a gate signal which causes the red, green and blue video signals to be output only during the display period.

The data input to the RAMs $2_0$ to $2_7$ is effected by zeroth, first and second biys ($a_0$), ($a_1$) and ($a_2$) of a data bus 9 of a CPU 8 in connection with the graphic memories 1R, 1G and 1B for red, green and blue pictures, respectively. Namely, in any of the graphic memories, only a rewrite of one-bit data is effected in one cycle of operation of the CPU 8. Reference numerals 10R, 10G and 10B indicate drivers.

Addressing and sending of a write signal for writing one-bit data from the CPU 8 into the RAMs $2_0$ to $2_7$ are carried out in the following manner: Of a 16-bit address bus 11 of the CPU 8, zeroth to second bits ($a_0$, $a_1$ and $a_2$), i.e. a total of three bits, are provided to a RAM selector 12 and, for example, 10 bits of the remaining bits are

applied to the multiplexer 6. The addressing of each graphic memory is effected by the CPU address that is input via the multiplexer 6. On the other hand, the RAM selector 12 is further supplied witha signal d from an address decoder 13 and a signal c from a timing generator 14, and the AND signal of the signasls d and c is provided on any one of eight output lines $12_0$ to $12_7$. It is dependent upon the contents of the three low-order bits ($a_2$, $a_1$ and $a_0$) to which output line the above AND signal is output. The eight output lines $12_0$ to $12_7$ are each connected to one of write terminals of the RAMs $2_0$ to $2_7$ of each of the graphic memories 1R, 1G and 1B. Accordingly, it is determined by addresses $a_2$, $a_1$and $a_0$ of the three low-order bits in which RAM of each of the graphic memories 1R, 1G and 1B the one-bit data is written. Incidentally, the address decoder 13 decodes address information on the address bus 11 and makes the signal d a "1" when the CPU is to access the graphic memories 1R, 1G and 1B, and makes a signal e a "1" when the CPU is to access the CRT controller 5. The address decoder 13 can be constituted by an AND circuit which, assuming that the address space of each of the graphic memories 1R, 1G and 1B is F0000 to FFFF, makes the signal d a "1" when four bits of addresses a16 to a19 of the CPU a11 go to "is", and an AND circuit which makes the signal e a "1" when the address space of the CRT controller is accessed.

The timing generator 14, when receiving the write signal from the CPU 8, makes the signal c a "1" in tne

write cycle of the RAMs $2_0$ ro $2_7$ immediately thereafter. Furthermore, the timing generator 14 outputs a signal a to the multiplexer 6 and a signal b to the shift registers 3R, 3G and 3B. The signal a is to make a distinction between the cycle of reading out data from the graphic memories 1R, 1G and 1B and the cycle of writing thereinto data from the CPU 8, and by this signal a, the output of the multiplexer 6 is switched between the side of the address bus 9 of the CPU and the side of the CRT controller 5. A signal b is a strobe signal by which eight-git data read out of the graphic memories 1R, 1G and 1B is latched in the shift registers 3R, 3G and 3B, respectively.

The timing generator 14 can be arranged, for instance, as shown in Fig 7. In Fig. 7, an octal counter 70 is counted up by the dot clock dc and outputs $Q_1$, $Q_2$ and $Q_3$ of its three low-order bits are taken out. The outputs $Q_1$ to $Q_3$ are provided to an AND circuit 71, the output of which is used as the signal b. The signal $Q_3$ becomes the signal a. The dot clock dc is applied to the clock terminals of flip-flops 73 and 74 as well. The write signal and the output of the AND circuit 71 are ANDed by an AND circuit 72, the output of which is input to the set terminal S of the flip-flop 73. The output Q of the flop-flop 73 is connected to the set terminal S of the flip-flop 74, the inverting output $\overline{Q}$ of the flip-flop 73 is connected to the reset terminal R of the flip-flop 74 and the output Q of the

flip-flop 74 is connected to the reset terminal R of the flip-flop 73. The output Q of the flip-flop 74 is used as the signal c.

Fig. 4 shows timing charts of the dot clock which serves as shift pulses of the shift registers 3R, 3G and 3B, a word clock for counting up the display address, the output of the multiplexer 6, the input to each of the graphic memories 1R, 1G and 1B, the output of each of the graphic memories 1R, 1G and 1B, the signals a, b and c and the write signal from the CPU 8. As shown in Fig. 4, the contents of the graphic memories 1R, 1G and 1B are read out by steps of eight bits and the write cycle occurs in the interval between the read cycles.

Next, a description will be given of the operation of the unit illustrated in Fig. 1. Fig. 5 is a flowchart showing an example of processing by the CPU 8 for writing graphic data into the graphic memories 1R, 1G and 1B. As shown in Fig. 5, the creation of a graphic form starts with deciding the color in which the graphic form is to be cisplayed. Then the following information is stored in three low-order bits of an eight-bit register such as an internal register of the CPU. That is, as shown in Fig. 6, red information is set in the least significant bit $a_0$, green information in the next bit $a_1$ and blue information in the next bit $a_2$.

| | | | | | |
|---|---|---|---|---|---|
| Display color | black | 000 | Display color | red | 001 |
| Display color | green | 010 | Display color | blue | 100 |
| Display color | yellow | 011 | Display color | magenta | 101 |
| Display color | cyan | 110 | Display color | white | 111 |

Next, the data of the above register is written into an address of the concerned one of the RAMs $2_0$ to $2_7$. For instance, in the case of displaying a red dot at one point on the display screen, if the area of the graphic memory corresponding to that point is a second area (numbered 9 in Fig. 2) of the RAM $2_1$, then a write signal is produced, as shown in Fig. 4, after which the three low-order bits of the CPU address are made, for example, (0, 0, 1) so as to select the output line $12_1$ and the address being applied to the multiplexer 6 is set so that the second area of the RAM $2_1$ is selected. Then data (00000001) is provided on the data bus 9. Since the least significant bit of the data bus 9 is connected to the graphic memory 1R for red picture, as mentioned previously, data"1" is stored in the second area of the RAM $2_1$. At this time, a "1" is stored in each of second areas of the graphic memories 1G and 1B.

On On the other hand, when the multiplexer 6 is changed over by the signal a, the contents of the graphic memories 1R, 1G and 1B are read out by steps of eight bits and the data of the RAM $2_1$ is read out and displayed in at least one scanning period of the display screen.

As described above, according to the present invention,

in grapnic memory a write/read control unit which writes, bit by bit, data into graphic memories for red, green and blue pictures, each having a capacity of N × M bits, and reads out therefrom the data by steps of M bits, since the graphic memories for red, green and blue pictures are each formed by a RAM group of an M-bit output which includes M RAMs each having a one-bit output and a 1 × N bit capacity and since the graphic memories for red, green and blue pictures are assigned the same address space, it is possible to specify, by one addressing from a CPU, eight bits of the same addresses of the graphic memories for red, green and blue pictures. Furthermore, since different one-bit data lines of the CPU are connected to all the RAMs of the graphic memories for red, green and blue pictures and since the abovesaid bitwise data write is effected by specifying one bit of each RAM of each graphic memory by a CPU address and by sending a write signal to an arbitrary one of the M RAMs by a part of the CPU address, it is possible to write data bit by bit from the CPU and to specify the display color simultaneously with the data write. Thus the present invention makes it possible to modify one bit of each graphic memory in one cycle of the CPU simply by the additional provision of a small amount of hardware.

C L A I M

A graphic memory write/read control unit which writes, bit by bit, data in graphic memories for red, green and blue pictures and reads out therefrom the data in units of M bits, characterized in that the graphic memories for red, green and blue pictures each comprise a RAM group of an M-bit output which includes M RAMs each having a one-bit output and a 1 × N bit capacity; the graphic memories for red, green and blue pictures are assigned the same address space; different one-bit data lines of a data bus of a CPU are connected to all the RAMs of the graphic memories for red, green and blue pictures; and the bitwise data write is effected by specifying one bit of each RAM of each graphic memory by a CPU address and by sending a write signal to an arbitrary one of the M RAMs by a part of the CPU address.

FIG. 1

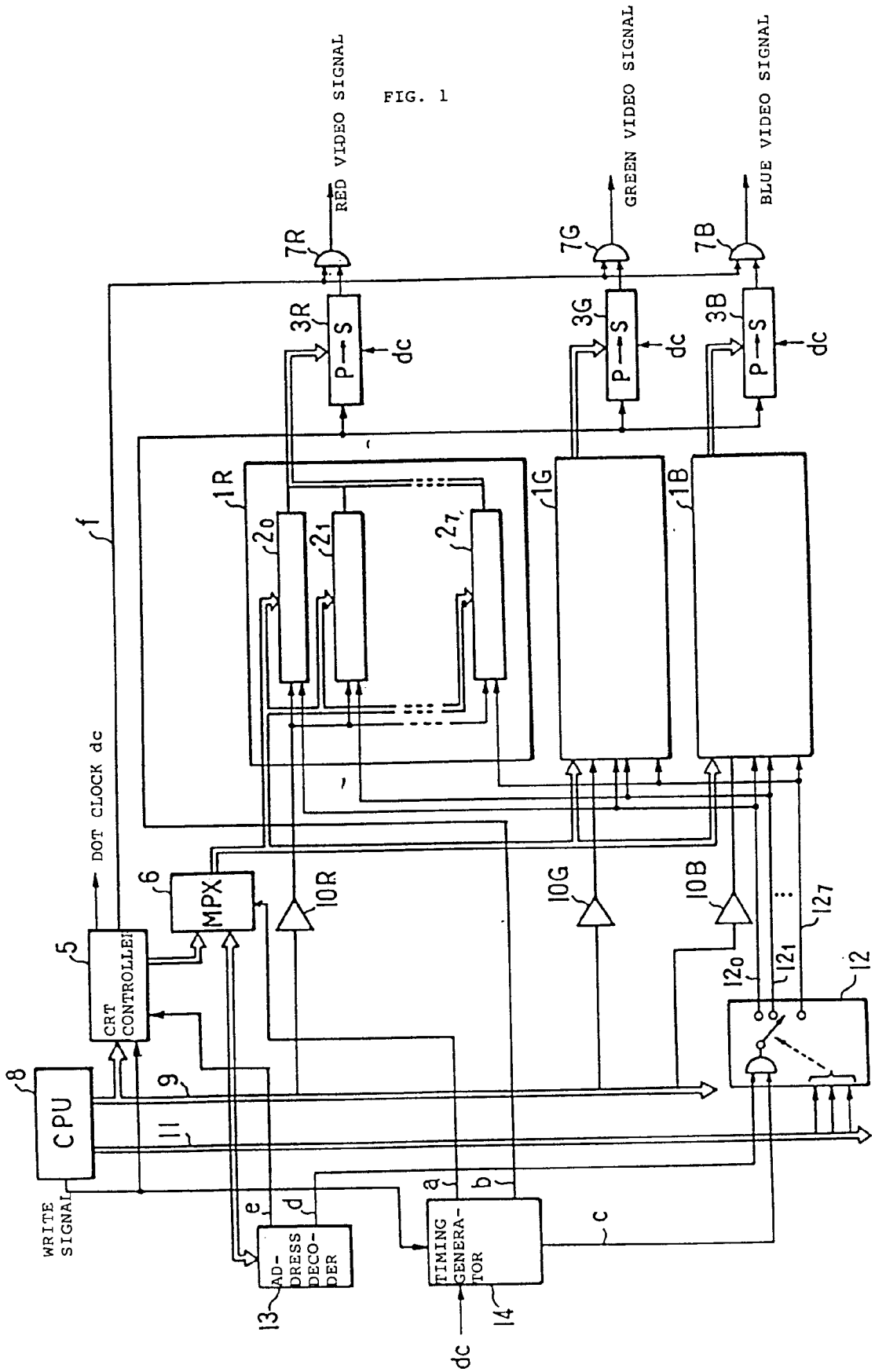

RED VIDEO SIGNAL
GREEN VIDEO SIGNAL
BLUE VIDEO SIGNAL
7R
7G
7B
3R
3G
3B
P—S
dc
1R
1G
1B
20
21
27
1
DOT CLOCK dc
6
MPX
10R
10G
10B
5
CRT CONTROLLER
8
CPU
9
11
WRITE SIGNAL
e
d
a
b
c
ADDRESS DECODER
TIMING GENERATOR
13
14
120
121
127
12

FIG. 2

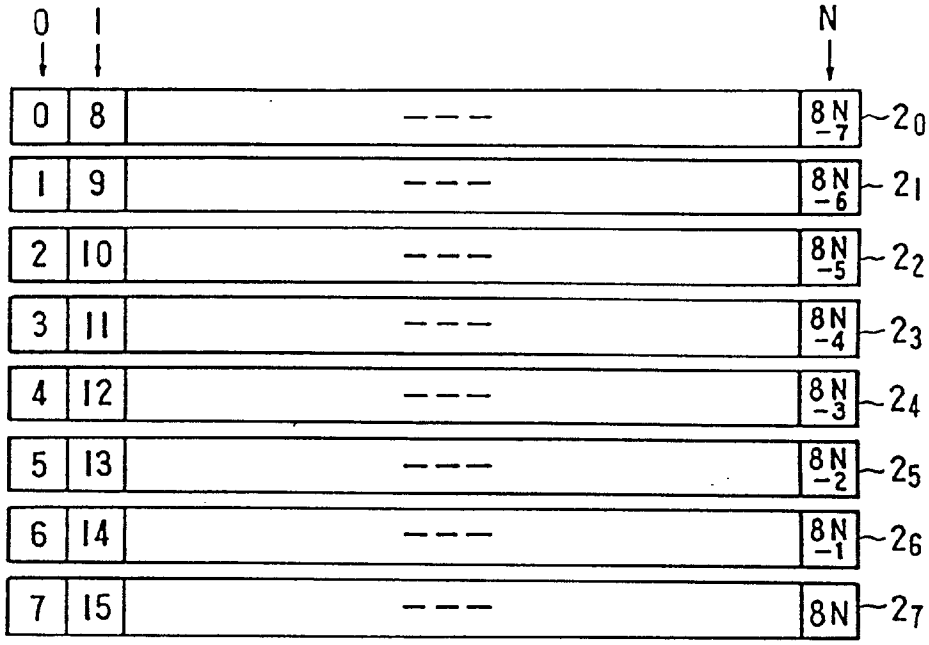

0
1
N
0
8
8N−7
20
1
9
8N−6
21
2
10
8N−5
22
3
11
8N−4
23
4
12
8N−3
24
5
13
8N−2
25
6
14
8N−1
26
7
15
8N
27

FIG. 3

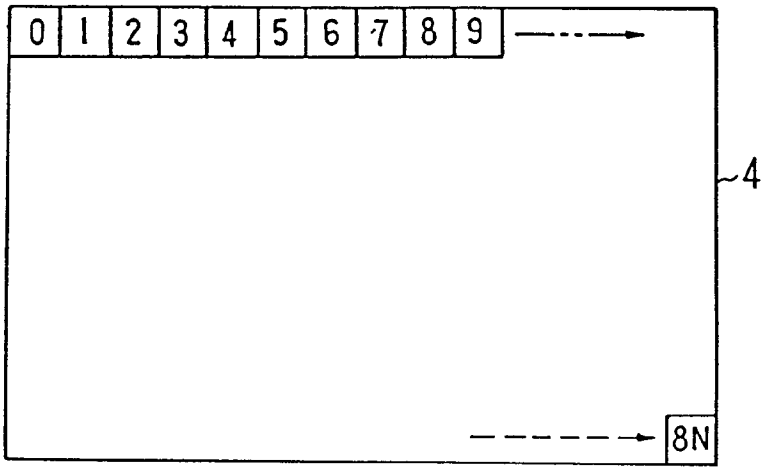

0
1
2
3
4
5
6
7
8
9
4
8N

FIG. 4

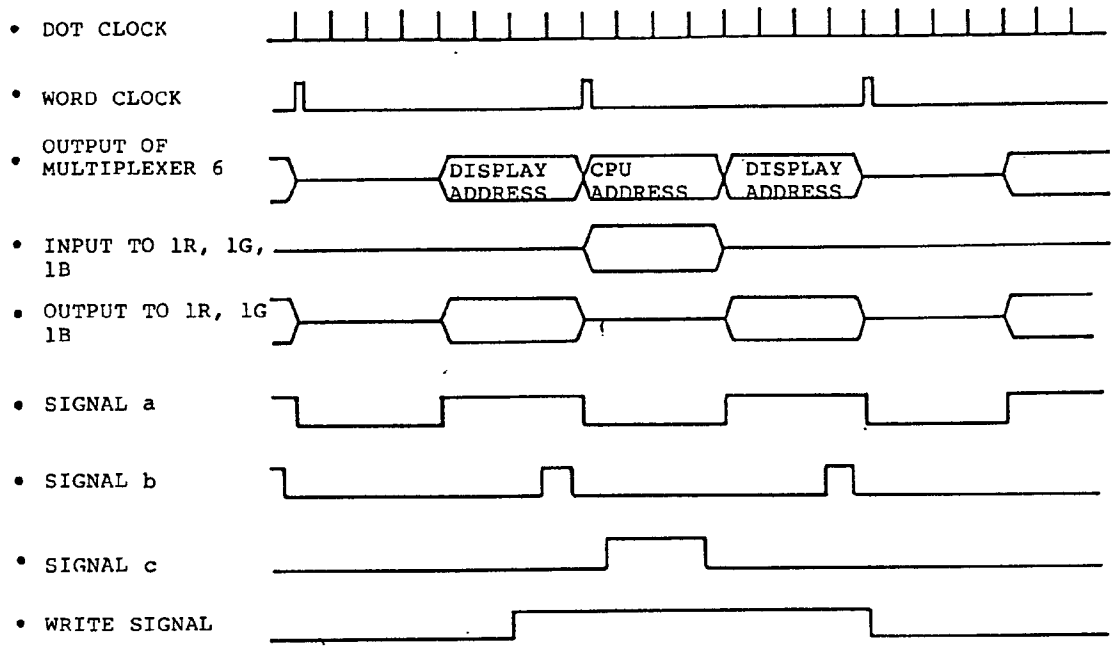

• DOT CLOCK
• WORD CLOCK
• OUTPUT OF MULTIPLEXER 6
DISPLAY ADDRESS
CPU ADDRESS
DISPLAY ADDRESS
• INPUT TO 1R, 1G, 1B
• OUTPUT TO 1R, 1G 1B
• SIGNAL a
• SIGNAL b
• SIGNAL c
• WRITE SIGNAL

FIG. 6

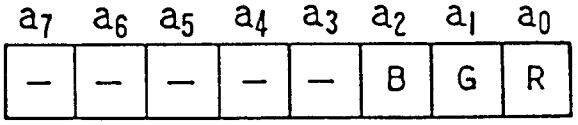

a7 a6 a5 a4 a3 a2 a1 a0
— — — — — B G R

FIG. 5

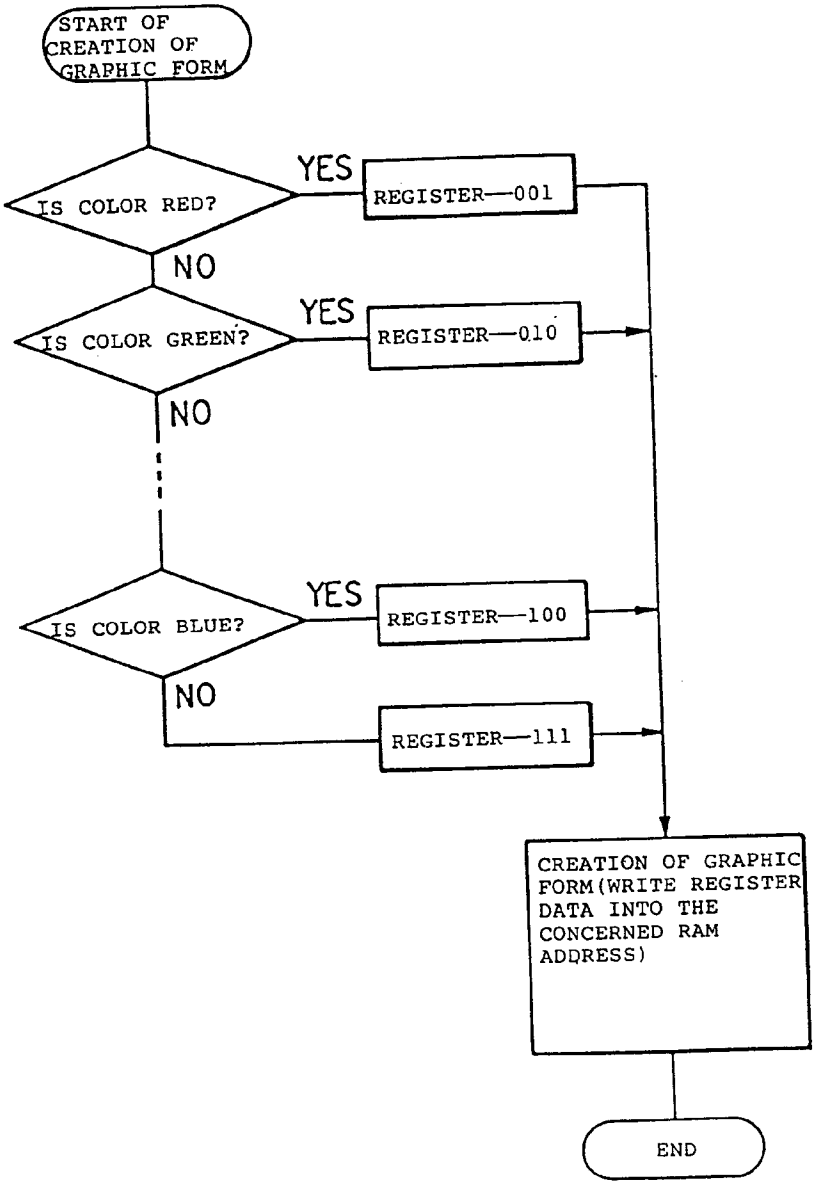
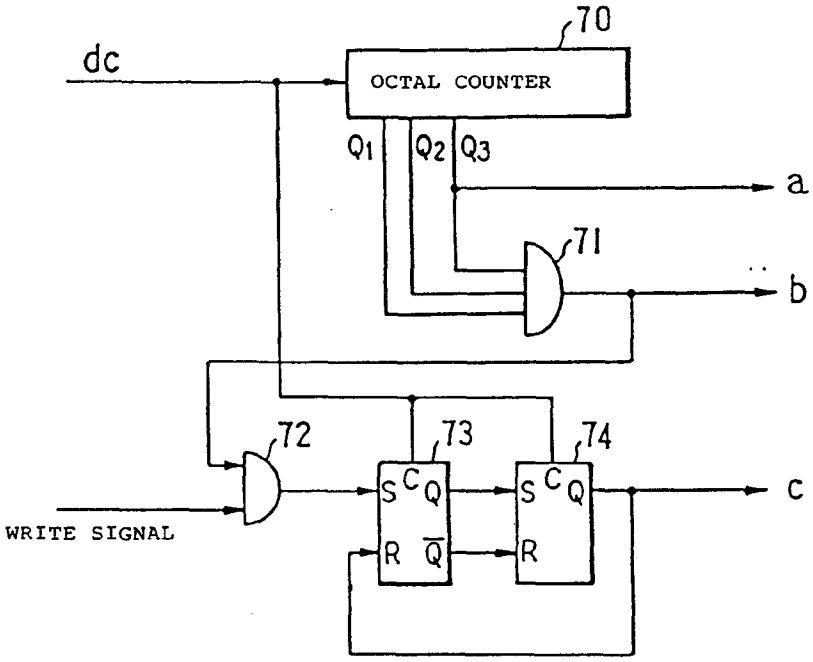

START OF CREATION OF GRAPHIC FORM
IS COLOR RED?
YES
REGISTER—001
NO
IS COLOR GREEN?
YES
REGISTER—010
NO
IS COLOR BLUE?
YES
REGISTER—100
NO
REGISTER—111
CREATION OF GRAPHIC FORM(WRITE REGISTER DATA INTO THE CONCERNED RAM ADDRESS)
END

FIG. 7



# INTERNATIONAL SEARCH REPORT

0161319

International Application No. PCT/JP84/00503

## I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl[3] G09G 1/28, 1/02

## II. FIELDS SEARCHED

Minimum Documentation Searched [4]

| Classification System | Classification Symbols |
|---|---|
| IPC | G09G1/28, 1/02 |

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

## III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

| Category* | Citation of Document, [16] with indication, where appropriate, of the relevant passages [17] | Relevant to Claim No. [18] |
|---|---|---|
| X | JP, A, 53-29033 (Victor Company of Japan, Ltd.), 17 March 1978 (17. 03. 78) | 1 |

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

## IV. CERTIFICATION

| Date of the Actual Completion of the International Search [2] | Date of Mailing of this International Search Report [2] |
|---|---|
| December 17, 1984 (17. 12. 84) | January 14, 1985 (14. 01. 85) |
| **International Searching Authority [1]** | **Signature of Authorized Officer [20]** |
| Japanese Patent Office | |