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(54) Switching circuits and matrix device using same.

(57) The invention relates to switching circuits and matrix device using same and having the form of a flat panel comprising a control device and a smectic liquid crystal display including pixels arranged in a coordinate matrix of 400 rows and 720 columns. The control device includes several driver units located along the four sides of the rectangular matrix and serially interconnected along each side so as to constitute bidirectional shift registers for serial control data and information. Each driver unit controls 30 odd or 30 even numbered lines (rows or columns) and is able to apply to these lines for a predetermined duration DC voltages equal to either -150 Volts, -30 Volts, 0 Volt, +30 Volts or +150 Volts in function of these data and information.

EP 0 162 969 A1

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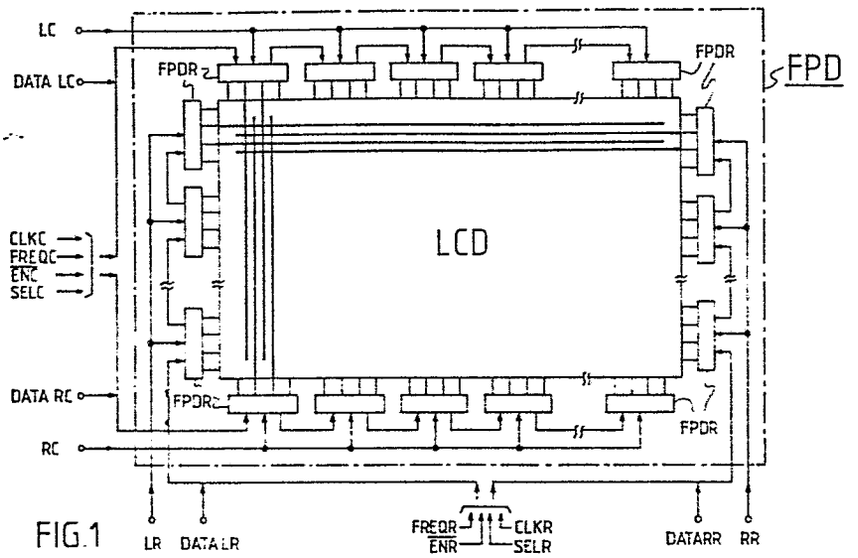
LC
DATA LC
CLKC
FREQC
ENC
SELC
DATA RC
RC
FPDR
FPDR
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LCD
FPDR
FPDR
LR
DATALR
FREQR
ENR
CLKR
SELR
DATARR
RR

FIG.1

Switching circuits and matrix device using same

The present invention relates to a matrix device and an associated control device, said coordinate matrix including a plurality of series of crossing electric lines (rows, columns) defining crosspoints, said control device including a plurality of driver units arranged along different sides of said coordinate matrix and having line output terminals coupled to distinct ones of the lines of at least one of said series, and said control device including also an input signal source coupled to said driver units and adapted to supply input signals to said driver units.

Such a device is already known in the art, e.g. from the UK patent application GB 2 120 440 A. Therein, driver units are on opposite sides of the coordinate matrix thereby benefiting from a spacing between adjacent unit terminals which is twice that between matrix lines. However, the lines on opposite sides are used for distinct functions.

An object of the present invention is to provide a matrix device of the above type but which enables the use of identical driver units having a maximum number of terminals per unit surface and able to be coupled to the signal source by a minimum of equipment.

According to the invention, this object is achieved due to the fact that each of said driver units includes a plurality of driver circuits each having one of said line output terminals and interconnected so as to form a shift register, shift control means to shift said input signals through said shift register, and direction means for controlling the direction of said shift.

Another characteristic of the present invention is that said input signals for said one series of lines being fed from said input signal source to a same side of said matrix device through connector terminals.

By the use of shift registers which are fed from a same side of the matrix, the number of connector terminals required to coupled the signal source to these shift registers is reduced. On the other hand, because these shift registers are bidirectional they can be fed from a same side of the matrix and the driver units can be made identical and arranged with most of their line output terminals facing a side of the matrix. Another advantage of such a driver unit is that, when integrated on a chip, output terminals can be arranged on the four sides thereof.

These advantages will be appreciated from the following considerations.

The driver units could be identical if so arranged that most of their line output terminals would face the matrix and the input signals were fed to the shift registers from opposite sides of this matrix. However, in this case the number of connector terminals required would increase and, moreover, the input signals would have to be shifted through the shift registers in reverse order. Another solution permitting the use of identical driver units would be to connect the line output terminals of the driver units arranged at one side of the matrix to corresponding lines of this matrix by prolonging these lines under these units. However, in this case the side of the chip facing the matrix can not have terminals so that the total number of terminals per unit surface would then be considerably reduced. To be noted that it is particularly important to have a high number of terminals per surface in case the driver unit is integrated on a chip as mentioned above. It is possible to increase this number by increasing the chip dimensions but these are limited by the dimensions of the package wherein the chip may have to be mounted. Moreover, a substantially square chip is preferred

since it has a better mechanical resistance.

It should also be noted that instead of using identical driver units it is possible to use "mirror-image" driver units. Although a single type of driver unit has a more complex design, it has the advantage that it can be manufactured, tested and stocked at less cost than two separate chips, even though the latter can benefit from a partly common design since a mirror symmetry is present.

The present invention relates also to a signal switching circuit enabling controlled complementary couplings between first and second terminals and, alternatively, between third and fourth terminals.

Such a switching circuit is already known in the art and is generally realized by means of two complementary controlled switches or gates used for respective ones of the two couplings.

A further object of the invention is to provide a switching circuit of the above type but which enables the signals transmitted between the first and the second terminals, or between the third and the fourth terminals to be memorized while remaining of a particularly simple structure.

According to the invention this object is achieved due to the fact that said second and fourth terminals are interconnected and coupled through a signal memory circuit to the common terminal of two gates controlled so as to be in complementary conductive states and whose other terminals are respectively coupled to said first and third terminals.

In this way the switching circuit memorizes the above signals and is of a very simple structure due to the use of only one electronic change-over contact formed by the two complementary controlled gates having the common terminal mentioned above, and by the common use of the memory circuit by the two couplings.

The present invention further relates to a switching circuit able to selectively couple one out of at least three

voltages at respective input terminals to a common output terminal.

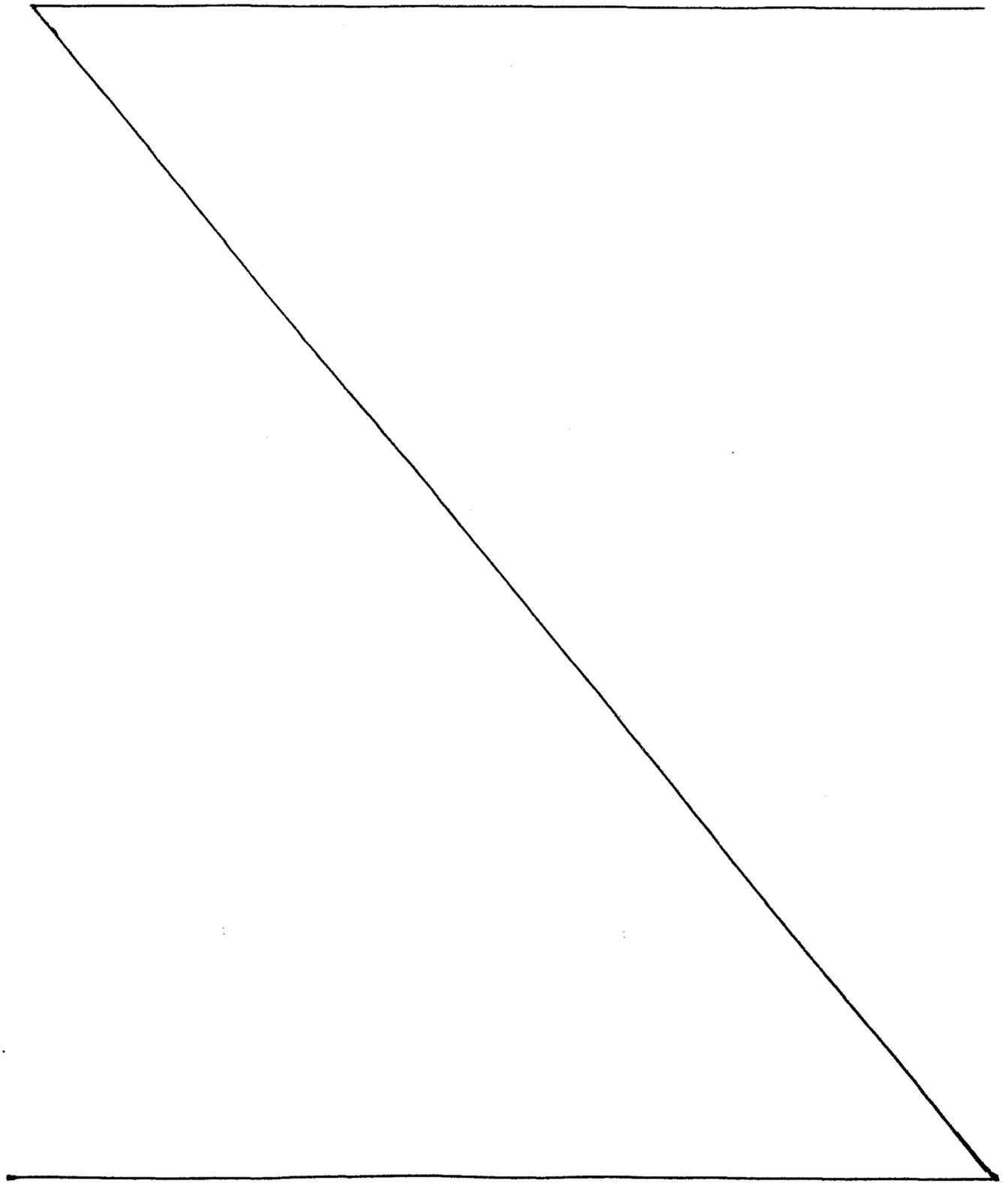
With such a multiple input switching circuit, a further object of the present invention is to realize a connection between one of these input terminals and the common output terminal while avoiding short circuits between the voltages applied to these input terminals, especially when the voltage difference between the terminals is relatively high e.g. 300 Volts.

This object is achieved due to the fact that first and second circuits coupling respectively the first and the second input terminals to said common output terminal include at least one DMOS switch device, and that at least one third circuit coupling the third input terminal to said common output terminal includes two DMOS switch devices coupled in series opposition.

Using the source-drain paths of DMOS transistors as switch devices is appropriate because they can withstand relatively high voltages such as the 300 Volts mentioned above. However, such DMOS transistors have a parasitic diode shunting their drain-to-source path. If the voltage at the first input terminal is the most positive one of the three, the DMOS transistor of the first circuit can then be oriented so that its parasitic diode is always blocked and has no influence on the open or closed state of this transistor. Alternatively, if the voltage at the second input terminal is the most negative one of the three, the DMOS transistor of the second circuit can also be oriented so that its parasitic diode is always blocked, e.g. the source of the DMOS transistor of one circuit is connected to the common output terminal together with the drain of the DMOS transistor of the other circuit.

With the voltage at the third input terminal having a value between the other two, irrespective of its orientation, the corresponding DMOS transistor in the third circuit would always have its parasitic diode conductive when

one of the two other voltages is present at the common output terminal. But two DMOS transistors connected in series with their parasitic diodes back to back solve the problem for this third circuit.



The above mentioned and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings in which :

Fig. 1 is a schematic view of a matrix device or a flat panel display FPD, including several driver units FPDR, according to the invention;

Figs. 2 and 3 represent signals generated by such a driver unit FPDR and some signal waveforms resulting from the combination of these signals;

Fig. 4 is a schematic view of such a driver unit FPDR;

Fig. 5 shows direction control circuit RLC of Fig. 4 in detail;

Fig. 6 is a block diagram of clock circuit CKC of Fig. 4;

Fig. 7 are signal waveforms generated by this clock circuit CKC;

Fig. 8 shows an interface circuit IC of Fig. 4 in detail;

Fig. 9 shows a logical device LD of Fig. 4 in detail;

Fig. 10 shows a high voltage device HVD of Fig. 4 in detail.

The matrix device or flat panel display FPD shown in Fig. 1 includes a liquid crystal display LCD and control circuitry mounted around this display. The latter consists of a thin film of smectic liquid crystal sandwiched between two plates of glass each provided with a set of transparent conductive stripes represented in heavy lines and forming rows and columns of a coordinate matrix respectively. The area of the intersection of two such perpendicular row and column stripes represents one picture element or pixel and the display includes 288,000 such pixels arranged in 400 rows and 720 columns. This is sufficient to display 2000 alpha-

numeric characters each defined by 9 columns and 16 rows.

One major advantage of the smectic liquid crystal used in this display is its ability to rapidly change the state of its pixels. A transparent state is the result of a "clearing" operation and an opaque state is the result of a "scattering" operation. The change of state of a pixel, from opaque to transparent and vice versa, can be derived directly from the drive signals applied to the corresponding crossing row and column stripes. The scatter function (create an opaque pixel) specifically requires one cycle time of a 50 Hertz signal, i.e. 20 milliseconds, and the clear function (create a transparent pixel) requires three cycles of a 1.5 kilohertz signal, i.e. 2 milliseconds. Additional cycles will have no significant effect. Another important characteristic of the smectic liquid crystal material is its voltage threshold, i.e. it will not change state until a certain minimum level of voltage is reached. When this level is exceeded on a particular pixel, that picture element will assume the state indicated by the applied frequency. Near the threshold the liquid crystal material responds rather slowly. However, when the stimulating voltage increases, the response time decreases.

An unbalanced drive signal should never be used to drive a row or column stripe since a long term DC component applied to the liquid crystal material adversely affect performance and life thereof. All these drive waveforms should therefore be well balanced, i.e. they should have equal positive and negative amplitudes and durations.

In order to control the visible information of all the pixels in a row, first this entire row is scattered to effectively eliminate all visible information and afterwards, to display new information, selected pixels are cleared whilst the remaining pixels of that row are left in their scattered state. This means that, the scatter function is performed on at least one row whilst the clear operation is always done one row at a time. However, in that one row, only specific indi-

vidual pixels are selected to be cleared.

The scattering waveforms are shown in Fig. 2. Scatter of a pixel is performed by differentially applying thereto one cycle of a 50 Hertz square waveform PSC having an amplitude of 600 Volts peak-to-peak. There are two modes used for scattering. According to a first mode the entire panel is scattered. This is accomplished by applying square waveforms CSC and RSC which are in phase opposition to all column stripes and to all row stripes during one cycle respectively. These waveforms have a peak-to-peak voltage of 300 Volts. More particularly during the first half cycle time, a voltage of +150 Volts (CSC) is applied to all the column stripes while a voltage of -150 Volts (RSC) is applied to all the row stripes of the display. The resulting differential voltage has an amplitude of 300 Volts (PSC). During the second half cycle time the voltage applied to all the column stripes changes to -150 Volts (CSC) while the voltage applied to all the row stripes changes to + 150 Volts (RSC). This creates a downward voltage step of 300 Volts on the column stripes and an upward voltage step of 300 Volts on the row stripes and thus gives rise to the required differential voltage step of 600 Volts (PSC) on each pixel. This will effect a scatter of all pixels.

According to a second mode of scatter, only selected rows are scattered. In this case, the voltage waveform CSC is applied to all the columns whilst the voltage waveform RSC in phase opposition with respect to CSC is only applied to the row stripes to be scattered. A square voltage waveform RNSC which is the complement of RSC is applied to the other row stripes. The resultant differential voltage PNSC thus applied across all the pixels in these last mentioned rows is zero so that no scattering occurs therein.

The clear function is used to control individual pixels and to thereby display visible information. This operation is performed on selected pixels of a single row

which has previously been set to the scattered state and consists of differentially applying three cycles of a 1.5 kilohertz square voltage signal PCL with an amplitude of 360 Volts peak-to-peak (Fig. 3). The creation of the differential voltage is explained hereinafter.

To the single selected row stripe three cycles of a square "row information" signal called STROBE (Fig. 3) are applied, all other row stripes being connected to the ground voltage. The signal STROBE has a peak-to-peak voltage of 300 Volts. To all column stripes, another square "column information" signal CNC or CC (each 60 Volts peak-to-peak) having same frequency as the signal STROBE is applied during the whole clear operation. The signal CNC is in phase and the signal CC is in phase opposition with respect to the signal STROBE, these waveforms being shown in Fig. 3. The signal CC is applied to the column stripes whose pixels are to be cleared, whilst the signal CNC is applied to the column stripes whose pixels are to be left in the scattered state.

When the signals STROBE and CC are applied to a pixel, these signals add and the pixel experiences, differentially, the required clear signal PCL. Thus, that pixel is cleared within three cycles. Note that this high level signal PCL is applied for only three cycle times to each row in turn, one row at a time.

It should be noted that in a clearing operation the voltage threshold characteristic of the liquid crystal material as well as the duration of the signals applied should be carefully respected. In order to assure proper access of selected pixels only, it is therefore necessary to evaluate the residual voltage applied to other pixels which are not to be cleared. Three situations must be considered wherein pixels must not be cleared. These are :

1) pixels in the same column as the addressed pixel;
2) pixels in the same row as the addressed pixel but not to be cleared;

3) pixels neither in the same column nor row as the addressed pixel.

For the first case, in the same column, pixels are subjected to the signal CC on the column stripe and to ground voltage on the row stripe. This produces a resulting differential signal (60 Volts peak-to-peak) which is identical to the signal CC and which may be applied for a long time, to the pixels without affecting their previous state.

For the second case, in the same row, pixels are subjected to the signal CNC on the column stripe and to the signal STROBE on the row stripe. This combination produces a differential voltage PNCL (Fig. 3) of 240 Volts peak-to-peak across these pixels. This voltage PNCL cannot be held on the pixels for a long period but since no more than three cycles (2 milliseconds) are applied to each row the state of these pixels is not affected.

For the third case, where the pixel is neither in the row nor column of the one being cleared, the signal CNC is applied to the column stripe while the row stripe is at ground. This produces across the pixel a differential voltage equal to CNC which may be applied for an indefinite period to the pixel without affecting its previous state.

To be noted that the frequencies (50 Hertz and 1.5 kilohertz) mentioned above are average values. In fact, temperature sensing means (not shown) are provided on the display to adjust the above frequencies in function of the temperature of the liquid crystal. Typically these frequencies are between 8.3 Hertz and 50 Hertz, and between 1 kilohertz and 2 kilohertz for the "clear" and the "scatter" respectively.

Referring again to Fig. 1, the above mentioned control circuitry includes a plurality of driver units FPDR and each of such unit encompasses 30 drivers which are each coupled to a row or a column stripe. Each driver unit FPDR is realized as a single chip and each driver thereof is able to apply the above mentioned signals CSC, CC, CNC or RSC, RNSC, STROBE to

the associated column or row stripe respectively. The switching between the positive and negative portions of these signals occurs with equal rise and decay times which are less than 30 microseconds. When both a row and a column drivers are operated the pixel at the crossing of the corresponding stripes is brought in an opaque or transparent state wherein it remains until it is again excited in a manner to change its state.

The driver units FPDR are mounted along the sides of the display LCD and those arranged at one side of the LCD control either the even or the odd numbered stripes ending on that side, whilst the driver units situated on the opposite side control the stripes of the other parity . As mentioned above, each driver unit FPDR is able to control 30 stripes and because there are 720 column stripes, 12 driver units FPDR are disposed along both the top and bottom sides of the LCD. Likewise, because there are 400 row stripes, 7 driver units FPDR are provided along the right and left sides of this display LCD. Along each side of the display LCD, the driver units FPDR are connected in cascade so that serial control data and information signals may be shited through these cascade connections. The flat panel display FPD further has only two sets of connector terminals located along two adjacent sides of the FPD respectively and the driver units FPDR are all identical and have their output terminals, connected to the associated stripes, oriented towards these stripes. For these reasons, the serial control data and information signals mentioned above have to be shifted in one direction in the driver units FPDR located along one side of the display LCD while they have to be shifted in the other direction in the driver units FPDR located along the opposite side of the display LCD. The direction of shifting is controlled in each cascade connection of driver units FPDR by the shift direction signals LC, RC, LR and RR which are applied to each driver unit FPDR of the cascade connections at the top of the columns, at the bottom

of the columns, at the left of the rows and at the right of the rows respectively. The serial control data signals applied to the columns stripes are a column clock signal CLKC, a column frequency signal FREQC, a column not enable signal $\overline{ENC}$ and a column select signal SELC. Since the driver units FPDR arranged along the top of the columns are connected to different stripes than those arranged along the bottom of these columns, additional serial information signals DATALC and DATARC are applied to these two cascade connections of driver units FPDR respectively. As will be explained more in detail later, these last mentioned serial information signals DATALC and DATARC associated with the previously mentioned serial control data signals are used to generate the above mentioned signals CSC, CC and CNC applied to the column stripes of the display LCD. Serial control data and information signals similar to those applied to the column stripes are also applied to the row stripes. These control data signals are a row clock signal CLKR, a row frequency signal FREQR, a row not enable signal $\overline{ENR}$ and a row select signal SELR. As for the columns, additional serial information signals DATALR and DATARR are used together with the previous serial control data signals to generate the above mentioned signals RSC, RNSC and STROBE which are applied to the row stripes of the display LCD.

A driver circuit FPDR is shown in detail in Fig. 4. It has control terminal D, terminals I1 to I5 and O1 to O5 and 30 output terminals OUT1/30 and includes 10 interface circuits IC1/10, a clock circuit CKC, a direction control circuit RLC, 30 logical devices LD1/30 and 30 high voltage devices HVD1/30. Control terminal D is coupled through direction control circuit RLC to the internal busses RB and LB which control inputs DA, DB of all the interface circuit IC1/10 as well as inputs RB, LB of all the logic devices LD1/30. Terminals I1 and O1 are connected to terminals AI, BO of LD1 and terminals AO, BI of LD30 via IC1 and IC6 respectively and the pairs of terminals I2, O2; I3, O3; I4, O4 and I5, O5 are connected to the internal busses SB, FB, EB and CKB via IC2,

IC7; IC3, IC8; IC4, IC9 and IC5, IC10 respectively. The busses SB, FB, EB are also connected TO the like named terminals of LD1/30 and the bus CKB is connected to an input of clock circuit CKC whose 4 outputs are connected to 4 corresponding inputs of LD1/30. The latter devices LD1/30 each have three outputs IN1 to IN3 which are connected to like named inputs of HVD1/30 provided with outputs OUT1/30 respectively. These outputs are each connected to a row or column stripe of the display LCD.

The control terminal D of RLC is adapted to receive one of the above direction signals LC, RC, LR or RR indicating the direction in which the serial signals have to be shifted (right or left) into FPDR, as will be explained below. In response to such a signal the RLC then provides 2 complementary output signals R and L which are applied to the busses RB and LB respectively to inform the other circuits of FPDR of the shift direction. When an activated direction signal corresponding to a shift right is applied to terminal D and when a suitable serial information signal DATALC, DATARC, DATALR or DATARR is supplied to terminal I1 from a preceding FPDR, this information signal is transmitted to terminal O1 via the series connection of interface circuit IC1, output terminal OUTI thereof (as will be described later), the above logical circuits LD1/30 and interface circuit IC6 via the input terminal INI thereof. From terminal O1, the information signal is transmitted to the next FPDR. For a shift left, a similar path is followed by the serial information signal but the input terminal of FPDR is then O1 and the output terminal is I1 the information signal being transmitted via output terminal OUTI of IC6 and input terminal INI of IC1. For each of the other interface circuits IC2/5 and IC7/10 of FPDR the input and output terminals INI and OUTI are shorted and connected to the busses SB, FB, EB and CKB respectively.

Referring now to Fig. 5, the direction control circuit RLC is shown therein with more details. This circuit

RLC with input terminal D corresponding to the like named control terminal D of FPDR and output terminals R and L is constituted by a resistor R1 connected to input terminal D and to output terminal L via inverter INV1. To the input of INV1 are also connected two clamping diodes D1 and D2 whose other ends are connected to a voltage supply terminal VDD (+12 Volts) and a ground terminal OV respectively. Moreover, a resistor R2 and output terminal R are also connected to the input of the invertor INV1, the other end of R2 being connected to VDD. The input terminal D is permanently connected either to the ground terminal OV or left open. Resistor R1 limits the possible current flowing through the clamping diodes D1 or/and D2 when an undesirable voltage, e.g. static electricity, is applied to input terminal D. When the input terminal D is connected to ground, output terminals R and L are at logical levels 0 and 1 respectively. On the contrary, when input terminal D is open, output terminal R is pulled up to logical level 1 by supply terminal VDD and resistor R2, whilst output terminal L is then at 0. A logical value 1 at output terminal R indicates a shift right whilst a logical value 1 at output terminal L indicates a shift left. These values are applied to other circuits of the driver unit FPDR via the corresponding internal busses RB and LB, as already mentioned.

Fig. 6 shows the clock circuit CKC having input terminal CKB connected to the like named internal clock bus CKB and having output terminals $\phi 1$, $\overline{\phi 1}$, $\phi 2$ and $\overline{\phi 2}$ providing like named clock signals respectively. CKC includes a NOR gate NOR1 which has its inputs connected to the terminals CKB and $\phi 1$, and another NOR gate NOR2 with its inputs connected to terminal $\phi 2$ and to terminal CKB via an inverter INV2. The output of NOR1 is connected to $\phi 2$ via the series connection of inverters INV3 and INV4 and to $\overline{\phi 2}$ via the series connection of inverters INV5 to INV7. The output of NOR2 is connected to $\phi 1$ via the series connection of inverters INV8 and INV9 and to $\overline{\phi 1}$ via the series connection of inverters INV10 to

INV12.

Fig. 7 shows the input clock signal CKB which is either the column clock signal CLKC or the row clock signal CLKR, as mentioned above, and also shows the output clock signals $\emptyset 1$, $\overline{\emptyset 1}$, $\emptyset 2$ and $\overline{\emptyset 2}$. The input clock signal CKB is a square wave applied to the like named input terminal CKB of clock circuit CKC via the input terminal I5 or O5, the corresponding interface circuit IC5 or IC10 and the internal clock bus CKB. Output signals $\overline{\emptyset 1}$ and $\overline{\emptyset 2}$ are the respective complements of $\emptyset 1$ and $\emptyset 2$. Due to the cascade connections of the inverters of CKC, signals $\emptyset 1$ and $\emptyset 2$ are rectangular waves with positive portions smaller than the negative ones and the positive portions of signal $\emptyset 1$ occur in the middle of the negative portions of signal $\emptyset 2$ and vice versa.

One of the above interface circuits IC1/10 is represented in Fig. 8 and indicated by IC. It has bond pad terminal BP connected to terminals I1/5 or O1/5, input and output terminals INI and OUTI respectively and control terminals DA and DB. The latter terminals DA and DB are controlled by the direction control circuit RLC via the internal busses RB and LB. The circuit IC has also a voltage supply terminal VDD (+12 Volts) and a ground terminal OV. Terminal BP is connected to the junction point of the series connected source-to-drain and drain-to-source path of MOS transistors PM1 and NM1 respectively, the source electrode of PM1 being connected to voltage supply terminal VDD and the source electrode of NM1 being grounded. The gate electrodes of these transistors PM1 and NM1 are respectively connected to the output of a NOR gate NOR3 and to the output of a NAND gate NAND1 each via an inverter INV13 and INV14 respectively. One input of NOR3 is connected to control terminal DA and one input of NAND1 is connected to control terminal DB, whilst input terminal INI is connected to the other inputs of NOR2 and of NAND1 via inverter INV15. Terminal BP is also connected to an input of another NAND gate NAND2 and to an input of another NOR gate NOR4. The

other inputs of NAND2 and of NOR4 are respectively connected to the control terminals DA and DB, whilst the outputs of these gates NAND2 and NOR4 are connected to the gate electrodes of MOS transistors PM2 and NM2 respectively. As for PM1 and NM1, the source-to-drain path of PM2 is connected in series with the drain-to-source path of NM2 and the source electrode of PM2 is connected to supply terminal VDD whilst the source electrode of NM2 is grounded. Moreover, output terminal OUTI is connected to the junction point of PM2 and NM2.

If data have to be shifted from terminal BP to output terminal OUTI, a logical value 1 must be applied to control terminal DA and a logical value 0 must be applied to control terminal DB of IC. This corresponds to a shift right (R = 1, L = 0) for the interface circuits IC1 to IC5 and to a shift left (R = 0, L = 1) for the interface circuits IC6 to IC10. In the above conditions (DA = 1, DB = 0), a logical value 1 is always applied to one input of NOR3 whilst a logical value 0 is always applied to one input of NAND1. This means that the output of NOR3 and NAND1 are at 0 and at 1 respectively so that a logical value 1 is applied to the gate electrode of transistor PM1 and a logical value 0 is applied to the gate electrode of transistor NM1. These latter transistors PM1 and NM1 are then both blocked and input terminal INI is disconnected from terminal BP. Furthermore, in the same conditions as above, a logical value 1 applied to terminal BP provides a 0 at the outputs of NAND2 and NOR4 so that PM2 conducts and that NM2 is blocked. This generates a logical value 1 corresponding to supply voltage VDD at the output terminal OUTI. On the contrary, a logical value 0 applied to terminal BP causes a 1 at the outputs of NAND2 and NOR4 so that PM2 is blocked and NM2 is conductive which results in a logical value 0 or ground being applied to output terminal OUTI. A similar operation occurs when logical values 0 and 1 are applied to the control terminals DA and DB respectively. The transistors PM2 and NM2 are then blocked so that the output

terminal OUTI is disconnected from terminal BP and that the logical value applied to the input terminal INI generates an identical logical value at terminal BP. Owing to the MOS transistors PM1, NM1 and PM2, NM2 the input signals applied to the terminals BP or IN1 of this interface circuit IC are reshaped at the output.

Moreover, due to the large area of bond pad terminal BP and to the connection wires, a large capacitance (not shown) appears between the terminal BP and the ground OV. This capacitance will be charged and discharged through the output resistance (not shown) of the MOS transistors PM1 and NM1 respectively. To reduce the effect of this capacitance, especially at high frequencies, the above mentioned output resistances have to be minimized. To do so, the dimensions of the MOS transistors PM1 and NM1 are increased and as a consequence the gate capacitance of these latter transistors is also increased. For the same reasons as above, the output resistance ---------- (not shown) of the transistors connected to these gates must be reduced. Since an inverter circuit contains less transistors than a logical gate (NAND or NOR), it is easier to realize a small output resistance for an inverter circuit. Therefore, inverters INV13 and INV14 having a small output resistance are placed between the output of the logical gates NOR3 and NAND1 and the gates of the MOS transistors PM1 and NM1 respectively. On the other side of the interface circuit IC, a capacitance (not shown) appears also between the terminal OUTI and the ground OV. However, this latter capacitance has a smaller value than the one at terminal BP. Therefore, the MOS transistors PM2 and NM2 are smaller than the MOS transistors PM1 and NM1, and the output resistances (not shown) coupled to the gate capacitances (not shown) of the transistors PM2 and NM2 are minimized in the logical gates NAND2 and NOR4 respectively so that no invertors are used for this part of the interface circuit IC.

One of the logical devices LD1/30 of Fig. 4 is represented in detail in Fig. 9 and indicated as LD. It has control terminals LB, RB, EB, FB and SB connected to the like named internal busses of the driver unit FPDR respectively and has output terminals IN1, IN2 and IN3 respectively connected to like named input terminals of a high voltage device HVD, as will be described later. Logical device LD is also connected to the clock circuit CKC via terminals $\overline{\emptyset 2}$, $\emptyset 2$ and $\emptyset 1$ and $\overline{\emptyset 1}$ carrying respective like named clock signals. As mentioned above the 30 logical devices LD1/30 of a driver unit FPDR are connected in cascade, each logical device LD having information terminals AI, BO and AO, BI among which the terminals AI and BO of a logical device LD are connected to the terminals AO and BI of the next logical device LD respectively. Logical device LD includes passing gates PG1 to PG7 each constituted by a NMOS transistor and a PMOS transistor (schematically represented with a small circle on its gate electrode) whose source and drain electrodes are interconnected and whose gate electrodes are controlled by complementary control signals as described below.

Terminal AI of a logical device LD is connected to terminal BI of this same logical device LD via the series connection of two oppositely connected passing gates PG1 and P_{G2}, each controlled by complementary direction signals applied to the control terminals LB and RB. The junction point

of these passing gates PG1 and PG2 is connected to both terminals BO and AO of LD via the series connection of passing gate PG3 controlled by the complementary clock signals $\emptyset 1$ and $\overline{\emptyset 1}$, inverter INV16, passing gate PG4 controlled by the complementary clock signals $\emptyset 2$ and $\overline{\emptyset 2}$ and another inverter INV17. Furthermore, an inverter INV18 has its input connected to the output of inverter INV16 and its output connected to the input of inverter INV16 via passing gate PG5 controlled by the clock signals $\emptyset 2$ and $\overline{\emptyset 2}$. The output of PG3 is also connected to one input of a NAND gate NAND3 via passing gate PG6 which is controlled by complementary signals applied to it via control terminal EB directly and through an inverter INV19 respectively. The output of PG6 is also connected to the input of inverter INV20 which is connected in series with inverter INV21 and to the output of passing gate PG7 whose input is connected to the output of inverter INV21 and which is controlled by signals which are the complement of those controlling PG7. The above input of NAND3 which is also the output of passing gate PG6, and control terminal FB are the two inputs of an Exclusive NOR gate XNR. The output of XNR is connected to one input of an AND gate AND1 directly and to one input of another AND gate AND2 via inverter INV22. The other inputs of AND1 and AND2 are both connected to output terminal IN3 which constitutes the output of a AND gate AND3. The two inputs of AND3 are the output of NAND3 and the output of INV19, whilst the second input of NAND3 is connected to the control terminal SB. Output terminal IN1 is constituted by the output of AND2 and output terminal IN2 is constituted by the output of AND1.

A logical value 1 applied to control terminal RB, i.e. in case of a shift right operation, and consequently a logical value 0 applied to control terminal LB, close passing gate PG1 and open PG2. The input terminal for the above mentioned serial information signal DATALC, DATARC, DATALR or DATARR of the logical device LD is then AI and the

output terminal is AO. In this case the input terminal of the driver unit FPDR (Fig. 4) is I1 and its output terminal is O1 so that the serial information signal applied to I1 is thus transmitted to O1 via the series connection of interface circuit IC1, its output terminal OUTI, terminal AI of LD1 to terminal AO of LD30, input terminal INI of IC6 and interface circuit IC6 itself. On the contrary, when a logical value 1 is applied to control terminal LB, i.e. in case of a shift left operation, and consequently a O is applied to control terminal RB, the passing gate PG1 is opened and PG2 is closed. The input terminal of LD for the above serial information signal is then BI and the corresponding output terminal is BO. In the same way as described above, for the driver unit FPDR, the information signal is transmitted through IC6 and IC1 but the input terminal is now O1 whilst the output terminal is I1. In IC6 and IC1 this signal is transmitted via output terminal OUTI and input terminal IN1 respectively. As described above, in case of a shift right operation (RB = 1, LB = O), passing gate PG1 is closed and passing gate PG2 is open so that an information signal applied to input terminal BI cannot be transmitted further into the logical device LD to terminal BO. On the contrary, an information signal applied to the input terminal AI is transmitted to terminal AO. Indeed, it is first applied to the input of inverter INV16 at the first occurrence of a positive pulse of clock signal Ø1. Afterwards, when clock signal Ø2 goes high, so that passing gates PG4 and PG5 are closed, it is shifted to output terminal AO via inverter INV17. This signal is also again applied to inverter INV16 via the feedback inverter INV18 and passing gate PG5. Because of the high output capacitance (not shown) of inverters INV16 and INV18 a latching of the signal takes place therein. Alternatively, for a shift left operation (RB = O, LB = 1), the information signal is handled in the same way but, as mentioned above, the input terminal is then BI and the output terminal is BO.

The values of the output signals IN1, IN2 and IN3 at the respective like named terminals IN1, IN2 and IN3 are dependent on the information signal DATALC/R or DATARC/R (Fig. 1) applied to terminal AI or BI (for the shift right or left) and on the control signals : not enable $\overline{ENC/R}$ (Fig. 1) applied to terminal EB, select SELC/R (Fig. 1) applied to terminal SB and frequency FREQC/R (Fig. 1) applied to terminal FB, as will be described below.

As long as the not enable signal ENC/R is at logical level 1, passing gate PG6 is closed and the serial information signals transmitted between AI and AO or between BI and BO also appear at the output of PG6. However, these signals are not validated by the control signals FB and SB and are thus not generating valid output signals at the output terminals IN1 to IN3. Indeed, because $\overline{ENC/R}$ is on 1 the output of INV19 is at 0 so that the outputs of AND3 and therefore also those of AND1 and AND2 are on 0.

On the negative going edge of the not enable signal $\overline{ENC/R}$, passing gate PG6 opens and passing gate PG7 closes and the last information signal at the output of PG6 is latched in the circuit comprising inverters INV20 and INV21 and passing gate PG7, due to the high output capacitances (not shown) of these inverters. In this case the output signal IN3 is at 0 only when the select signal SELC/R at terminal SB and the information signal latched in INV20 and INV21 are both at logical value 1.

For the other values of the signal SELC/R and the information signal, the values of the signals IN1 and IN2 may be represented by the following Boolean functions :

$IN1 = IN3.(DATA.\overline{FREQC/R} + \overline{DATA}.FREQC/R)$

and $IN2 = IN3.(DATA.FREQC/R + \overline{DATA}.\overline{FREQC/R})$

where DATA is either one of the information signals DATALC/R or DATARC/R. Consequently the signals IN1 and IN2 are both at 0 when IN3 is at 0. Alternatively, when IN3 is at 1, the signals IN1 and IN2 are only dependent of the above signals DATA and FREQC/R and of their respective complements.

The values of the signals IN1, IN2 and IN3 in function of $\overline{ENC/R}$, SELC/R, FREQC/R and DATA are summarized in the following table :

$\overline{ENC/R}$	SELC/R	DATA	IN1	IN2	IN3
1	X	X	0	0	0
0	1	1	0	0	0
0	0	0	FREQC/R	$\overline{FREQC/R}$	1
0	0	1	$\overline{FREQC/R}$	FREQC/R	1
0	1	0	FREQC/R	$\overline{FREQC/R}$	1

where X means "don't care".

The meaning of the values indicated in the previous table will become clear from the following description of a high voltage device HVD wherefore reference is made to Fig. 10. This high voltage device HVD represents either one of the 30 high voltage devices HVD1/30 of FPDR represented in Fig. 4. It has input terminals IN1, IN2 and IN3 connected to the like named output terminals of the logical device LD respectively as well as voltage supply terminals VDD (+12 Volts), +V1, -V2, +V3 and ground terminal OV. HVD also has output terminal OUT connected to a like named terminal of a stripe (row or column) of the display LCD. The voltages applied to the terminals +V1, -V2 and +V3 are +150 Volts, -150 Volts and +170 Volts or +30 Volts, -30 Volts and +50 Volts depending on the kind of stripe (row or column) connected to terminal OUT and on the operation (scatter or clear) to be performed on that stripe, as described previously. A stripe connected to HVD is represented in Fig. 10 by its equivalent circuit LCDE which comprises the series connection between the HVD terminal OUT and ground OV, of a resistor R3 and a resistor R4 in parallel with a capacitor C1.

The high voltage device HVD comprises three circuits HV1, HV2 and HV3 among which HV1 and HV2 are identical. Therefore, only HV1 and HV3 will be described in detail hereinafter.

Circuit HV1 has an input terminal TI and further terminals T1, T2, T3 and T4. It includes a high voltage PNP transistor P1 whose base electrode is connected to the junction point of resistors R5 and R6 which are branched in series between VDD and input terminal TI. The emitter electrode of transistor P1 is directly connected to VDD and its collector electrode is connected to the gate electrode of a high voltage NMOS transistor NM3 as well as to terminal T1 via resistor R7. Furthermore, the source electrode of transistor NM3 is directly connected to supply terminal -V2, whilst its drain electrode is connected to terminal T2 via resistor R8 and to the gate electrode of a second high voltage NMOS output transistor NM4. The drain electrode of the latter transistor NM4 is directly connected to terminal T3 and its source electrode is connected to terminal T4. For the circuit HV1, input terminal TI is connected to input terminal IN1 of HVD, terminal T3 is connected to supply terminal +V1 and terminal T4 is connected to output terminal OUT of HVD. Alternatively, the input terminal TI of circuit HV2 is connected to input terminal IN2 of HVD and the terminals T3 and T4 of HV2 are connected to output terminal OUT and supply terminal -V2 respectively. Moreover, the terminals T1 and T2 of the two circuits HV1 and HV2 are connected to respective like named terminals T1 and T2 of circuit HVD3 described below.

The circuit HV3 has input terminal IN3 corresponding to the like named input terminal of HVD. HV3 includes a NMOS transistor NM5 whose gate electrode is directly connected to terminal IN3, whose source electrode is connected to terminal OV and which has its drain electrode connected to the base electrode of a high voltage PNP transistor P2 via resistor R9. The emitter electrode of transistor P2 is connected to terminal +V3 and to its own base electrode via biasing resistor R10. The collector electrode of transistor P2 is connected to the gate electrode of a high voltage NMOS transistor NM6 and to terminal T2. The source electrode of transistor NM6 is connected

to terminal -V2, whilst terminal T1 is connected to the drain electrode of NM6 via a clamping diode D3. Terminal +V1 is also connected via resistor R11 to the junction point of the drain electrode of transistor NM6, the cathode of diode D3 and to the gate electrodes of a pair of high voltage NMOS output transistors NM7 and NM8 whose source electrodes are interconnected . The drain electrode of output transistor NM7 is connected to terminal OV and the drain electrode of output transistor NM8 is connected to terminal OUT of HVD.

The functionning of the high voltage device HVD will be described hereinafter. As mentioned above, the purpose of this device is to provide at its output terminal OUT signals such as CSC, CC, CNC, RSC, RNSC or STROBE depending on the kind of stripe (row or column) to which terminal OUT is connected and also in function of the required operation (scatter or clear). The voltages +V1 and -V2 may be applied to terminal OUT via the output transistors NM4 of the circuits HV1 and HV2, whilst the ground voltage OV may be applied to this output terminal OUT via the pair of output transistors NM7 and NM8, as will be explained below. The selection of the supply voltage which has to be applied to the output terminal OUT is a result of the logical values applied to the input terminals IN1 to IN3. Of course, transient short circuits between these supply voltages must necessarily be avoided, e.g. the two output transistors NM4 of the respective circuits HV1 and HV2 may never be both conductive since otherwise the voltages +V1 and -V2 would be shorted. The same is true for the combination of the pair of output transistors NM7, NM8 with each of the above output transistors NM4. To avoid such short circuits, the circuits HV1/3 are designed to block the output transistors NM4; NM7, NM8 faster than to make them conductive. To achieve this, the NMOS transistors NM4; NM7 and NM8 of the high voltage device HVD have a high gate capacitance (not shown) and to make them conductive their gate electrode is connected to a respective supply terminal +V3; +V1 via a high ohmic resistor R8; R11

(R8 = R11 = 40 megohms). More particularly, each of these NMOS transistors are slowly made conductive by charging its high gate capacitance towards a positive voltage via the associated high ohmic resistor. On the contrary, the blocking of each of these NMOS transistors NM4; NM7 and NM8 is produced more rapidly by the connection of its gate electrode to the supply terminal -V2 via the drain-to-source path of transistor NM3; NM6 which is then made conductive.

The three possible states of the high voltage device HVD indicated by the voltages at its output terminal OUT and corresponding respectively to various combinations of logical values applied to the input terminals IN1 to IN3 are analyzed in detail hereinafter. In the two first states a logical value 1 is applied to input terminal IN3 and logical values 1 and 0 are applied to input terminals IN1/2 and IN2/1 respectively. In a third state the logical value at the input terminal IN3 is equal to zero and, consequently, also the other input terminals IN1 and IN2 are at zero.

Logical values 0 at all the input terminals IN1 to IN3 cause the output transistor NM4 of circuits HV1 and HV2 to be blocked and the pair of output transistor NM7, NM8 to be conductive so that the ground voltage 0V is then applied to the output terminal OUT. Alternatively, a logical value 1 applied to one of the input terminals IN1 or IN2 causes the operation of the corresponding output transistor NM4. Since in these conditions, input terminal IN3 must be at logical value 1 as described before, the pair of output transistors NM7, NM8 is blocked so that the ground voltage is disconnected from the output terminal OUT. As a result, the supply voltage +V1 or -V2 from the like named supply terminal, to which the above operating output transistor NM4 is connected, is applied to the output terminal OUT. A scenario comprising the succession of the following logical values 1, 0, 1 and 0, 1, 1 at the respective input terminals IN1, IN2, IN3 will provide at the output terminal OUT of HVD the succession of voltages +V1 and

-V2 respectively. The latter succession of output voltages corresponds to one cycle of a signal such as CSC, CC, CNC, RSC, RNSC or STROBE mentioned above, as follows from Figs. 2 and 3.

The above mentioned two first states of the high voltage device HVD correspond always to a logical value 1 applied to input terminal IN3 and to complementary logical values applied to the input terminals IN1 and IN2 respectively. A logical value 1 at input terminal IN1 and a logical value 0 at input terminal IN2 cause the voltage +V1 to be applied to output terminal OUT whilst the logical values 0 and 1 applied to the input terminals IN1 and IN2 respectively cause the voltage -V2 to be applied to output terminal OUT. These two combinations of input signals are symmetrical due to the fact that the circuits HV1 and HV2 are identical. Therefore, only one of them, say IN1 at 1 and IN2 at 0 will be explained in detail hereinafter.

Since a logical value 1 corresponding to the supply voltage VDD, i.e. +12 Volts, is applied to input terminal IN3, transistor NM5 of circuit HV3 conducts so that transistor P2 also conducts. As a result, the positive voltage +V3 is applied to the gate electrode of transistor NM6 and to terminal T2 via the emitter-to-collector path of conductive transistor P2 so that transistor NM6 also becomes conductive. Afterwards, the negative voltage -V2 is applied to terminal T1 via diode D3 and the drain-to-source path of conductive transistor NM6 and this voltage -V2 is also applied to the gate electrodes of the pair of output transistors NM7 and NM8 in order to block them.

To be noted that, because transistors NM7 and NM8 are DMOS transistors, a parasitic diode (not shown) is coupled across their source and drain electrodes, this diode being inherent to the construction of these transistors. Such a parasitic diode has its cathode electrode connected to the drain electrode of the DMOS transistor whilst the anode electrode of

the diode is connected to the source electrode of the transistor. Since either a positive voltage up to +150 Volts or a negative voltage down to -150 Volts may be applied to the output terminal OUT by the circuits HV1 and HV2, these voltages also appear at the drain electrode of transistor NM8 since this electrode is connected to terminal OUT. Considering only transistor NM8 instead of the pair of transistors NM7, NM8, e.g. by shorting the source electrode of transistor NM8 to ground terminal OV, a negative voltage at the drain electrode of this transistor NM8 (e.g. -150 Volts) will be grounded via then conductive parasitic diode of this transistor NM8. This happens independently of the state (conductive or blocked) of transistor NM8. For the same reasons, if transistor NM7 is considered alone, e.g. by shorting the drain-to-source path of transistor NM8, a positive voltage at the terminal OUT (e.g. + 150 Volts) will be grounded via the parasitic diode of this transistor NM7. From the above it follows that the transistors NM7 and NM8 have to be coupled in series opposition to effectively disconnect the output terminal OUT from the ground terminal OV when a negative voltage is applied to the gate electrodes of this pair of transistors NM7, NM8 in order to block them.

In the circuit HV2, transistor P1 conducts due to the logical value 0 applied to input terminal IN2. Supply voltage VDD is thus applied to the gate electrode of transistor NM3 via the emitter-to-collector path of conductive transistor P1. Since the source electrode of transistor NM3 is connected to terminal -V2 and its drain electrode is connected to terminal +V3 via the emitter-to-collector path of transistor P2, terminal T2 and resistor R8, transistor NM3 becomes conductive. The negative voltage -V2 is then applied to the gate electrode of output transistor NM4 of circuit HV2 via the drain-to-source path of conductive transistor NM3. As a consequence transistor NM4 of circuit HV2 blocks immediately, thus disconnecting terminal T4 which is also the supply terminal -V2 from output terminal OUT.

Input terminal IN1 being at logical value 1, i.e. +12 Volts, transistor P1 of circuit HV1 is blocked so that the gate electrode of NMOS transistor NM3 of circuit HV1 is disconnected from supply terminal VDD to which it was previously connected via the emitter-to-collector path of transistor P1. Because transistor NM3 has a high gate capacitance, the latter discharges slowly to the voltage -V2 via high ohmic resistor R7 until this transistor NM3 blocks. At that moment the gate electrode of output transistor NM4 is disconnected from supply terminal -V2 and the high gate capacitance of this transistor NM4 is slowly charged to the positive voltage +V3 supplied thereto via the emitter-to-collector path of transistor P2, terminal T2 and resistor R8. After a while, output transistor NM4 of circuit HV1 becomes conductive and applies the supply voltage +V1 to the output terminal OUT via its drain-to-source path.

To be noted that the voltage +V3 is always equal to the voltage +V1 increased by about 20 Volts and for this reason the voltage +V3 at the gate electrode of conductive output transistor NM4 of circuit HV1 is always higher than the voltage +V1 at its source electrode so that transistor NM4 remains conductive.

In the third state of HVD, i.e. when the three input signals IN1 to IN3 all have logical value 0, transistor NM5 of circuit HV3 is blocked, thereby preventing any current flow through resistors R9 and R10 so that transistor P2 blocks. As a consequence and due to the fact that transistor NM6 has also a high gate capacitance, the voltage at the gate electrode of this transistor NM6 which was previously connected to supply terminal +V3 via transistor P2 decreases slowly. Before transistor NM6 is blocked, terminal T1 is connected to terminal -V2 via diode D3 and the drain-to-source path of this transistor NM6 in series, whilst the positive voltage +V3 is available at the terminal T2 because of the previous charge of the gate capacitance of transistor NM6.

In both the circuits HV1 and HV2 the 0 Volt at their terminal TI causes transistor P1 to conduct so that the gate electrode of transistor NM3 is brought at the positive voltage VDD via the emitter-to-collector path of transistor P1. As a result, transistor NM3 conducts immediately, providing via its drain-to-source path the negative voltage -V2 at the gate electrode of output transistor NM4. The latter output transistor NM4 therefore blocks immediately. The previous supply voltage +V1 or -V2 which was applied to the output terminal OUT via the drain-to-source path of transistor NM4 of either HV1 or HV2 is then disconnected from this output terminal OUT. Moreover, the voltage -V2 is also applied to the gate electrodes of the pair of output DMOS transistors NM7, NM8 via the drain-to-source path of transistor NM6. This negative voltage (-V2) blocks NM7, NM8 and the above mentioned parasitic diodes associated to these transistors and coupled in series opposition inhibit any flow of current in both directions between the output terminal OUT and the ground terminal OV.

At this moment, output terminal OUT is temporarily disconnected from any of the supply terminal +V1, -V2 and ground terminal OV. Since the gate electrode of transistor NM6 is disconnected from terminal +V3 due to the blocked transistor P2, the voltage at this gate electrode decreases slowly until transistor NM6 blocks. The voltage at the drain electrode of blocked transistor NM6, disconnected from terminal -V2, becomes slowly equal to +V1 due to the charging of the gate capacitances of the output transistors NM7 and NM8 via resistor R11. This voltage +V1 is not applied to terminal T1 because of the blocking diode D3. The output terminal OUT is then connected to ground terminal OV. Indeed, if the positive voltage +V1 was previously applied to terminal OUT, the latter is shorted to ground terminal OV via the drain-to-source path of conducting transistor NM8 in series with the operating parasitic diode of transistor NM7. On the

contrary, if the negative voltage -V2 was previously present at terminal OUT, the latter is shorted to terminal OV via the drain-to-source path of transistor NM7 in series with the parasitic diode of transistor NM8.

Because of the above mentioned disconnection of terminal T1 from a supply terminal, due to the blocking diode D3, transistors P1 of both the circuits HV1 and HV2 block. Furthermore, terminal T2 being also disconnected from its supply terminal +V3 because transistor P2 is blocked, no current flows through transistor NM3 of both the circuits HV1 and HV2, while transistor NM4 remains blocked. Excluding the leakage currents in the transistors in this state, the only currents in the high voltage device HVD flow from supply terminal VDD to input terminals IN1 and IN2 through high ohmic resistors R5 and R6 of both the circuits HV1 and HV2. So, the power consumption in the high voltage device HVD at rest, i.e. when IN1 = IN2 = IN3 = 0, is reduced to a minimum and the ground voltage OV is applied to the output terminal OUT.

As mentioned above, all the signals : CSC, RSC, RNSC (300 Volts peak-to-peak, 50 Hertz); CC, CNC (60 Volts peak-to-peak, 1.5 kilohertz) and STROBE (300 Volts peak-to-peak, 1.5 kilohertz) applied to corresponding line stripes (columns or rows) are supplied thereto by the output terminals OUT of the driver units FPDR. The voltages +150 Volts, +30 Volts and -150 Volts, -30 Volts at the output terminals OUT are supplied by the voltage supply terminals +V1 and -V2 respectively of each high voltage device HVD of the driver units FPDR. These voltages are applied to the output terminal OUT of each HVD under the control of the logical values IN1 to IN3 of the signals at the like named input terminals IN1 to IN3 applied thereto via the output terminals IN1 to IN3 of logical device LD. These logical values IN1 to IN3 are themselves controlled by the frequency signal FREQC or FREQR, the selection signal SELC or SELR and the serial information signal DATALC/R or DATARC/R latched by the inverters INV20 and INV21 in the

logical device LD when the corresponding not enable signal $\overline{ENC}$ or $\overline{ENR}$ is low.

The operations of the display LCD are summarized in the following table :

SELR	DATAR	SELC	DATAC	OPERATION	PIXEL SIGNAL
0	0	0	1	scattering	PSC
0	1	0	1	no scattering	PNSC
1	0	0	0	no clearing	PNCL
1	0	0	1	clearing	PCL
1	1	0	0	row not addressed	CNC
1	1	0	1	row not addressed	CC
0	X	0	0	not used	—
X	X	1	X	not used	—

where DATAR is either DATALR or DATARR, DATAC is either DATALC or DATARC and where X means "don't care".

In the previous table it is assumed that the not enable signals $\overline{ENC}$ and $\overline{ENR}$ are at logical value zero and that suitable frequency signals FREQC/R of 50 Hertz and 1.5 kilohertz are used for the scattering and the clearing respectively. Furthermore it is obvious that suitable supply voltages are applied to the supply terminals +V1, -V2 and +V3 of the high voltage devices HVD. It appears clearly from this table that the scatter operation is a result of a logical value 1 applied as information signal DATAC to the column stripes and of a logical value 0 used as selection signal for both SELC and SELR. Since the scatter operation may be performed for the complete display or for only selected rows, the rows to be scattered have a logical value 0 as information signal DATAR while the rows which are not to be scattered have a logical value 1 as information signal DATAR, the resulting signal at the corresponding pixels being PSC and PNSC respectively.

For the clear operation, the row selection signal SELR is always at logical value 1 while the column selection signal SELC is still at 0. The clearing being performed one row at a time, the selected row has its information signal DATAR at logical value 0 and the associated columns are either at 0 or at 1 corresponding to the not clearing PNCL or to the clearing PCL of the pixel respectively. The remaining rows i.e. those which are not addressed receive a logical value 1 as information signal DATAR. As mentioned above, the signals on the pixels of these rows (not addressed) are CNC or CC in function of the information signal DATAC on the corresponding column. The other possible combinations of signals are not used in the present embodiment. To be noted also that an active operation such as scattering or clearing is only performed when a logical value 0 is applied to a row stripe as information signal DATAR together with a logical value 1 applied to a column stripe as information signal DATAC.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention.

CLAIMS

1. Matrix device (FPD) with a coordinate matrix (LCD) and an associated control device, said coordinate matrix including a plurality of series of crossing electrical lines (rows, columns) defining crosspoints, said control device including a plurality of driver units (FPDR) arranged along different sides of said coordinate matrix and having line output terminals (OUT1/30) coupled to distinct ones of the lines of at least one of said series, and said control device including also an input signal source coupled to said driver units and adapted to supply input signals (DATALC/R, DATARC/R, CLKC/R, FREQC/R, $\overline{\text{ENC/R}}$, SELC/R) to said driver units, characterized in that each of said driver units (FPDR) includes a plurality of driver circuits (LD, HVD) each having one of said line output terminals (OUT1/30) and interconnected so as to form a shift register, shift control means (CKC) to shift said input signals (DATALC/R, DATARC/R) through said shift register, and direction control means (RLC) for controlling the direction of said shift.

2. Matrix device according to claim 1, characterized in that said input signals (DATALC/R, DATARC/R, CLKC/R, FREQC/R, $\overline{\text{ENC/R}}$, SELC/R) for said one series of lines being fed from said input signal source to a same side of said matrix device (FPD) through connector terminals.

3. Matrix device according to claim 1, characterized in that said line output terminals (OUT1/30) coupled to two immediately adjacent lines of at least one of said series are connected at different sides of said coordinate matrix (LCD) respectively.

4. Matrix device according to claim 1, characterized in that said matrix device is a flat panel (FPD) carrying a smectic liquid crystal flat panel display (LCD) which constitutes said coordinate matrix, and said driver units (FPDR) which are disposed around said display, cells of said display being located at said crosspoints.

5. Matrix device according to claim 1, characterized in that each of said driver circuits (LD, HVD) has logical means (LD1/30) including a signal switching circuit (PG1/5, INV16/18) controlled by said direction control means (RLC) and enabling complementary couplings between first (AI) and second (AO) terminals and, alternatively between third (BI) and fourth (BO) terminals.

6. Signal switching circuit (PG1/5, INV16/18) enabling controlled complementary couplings between first (AI) and second (AO) terminals and, alternatively between third (BI) and fourth (BO) terminals, characterized in that said second (AO) and fourth (BO) terminals are interconnected and coupled through a signal memory circuit (INV16, INV18, PG5) to the common terminal of two gates (PG1/2) controlled so as to be in complementary conductive states and whose other terminals are respectively coupled to said first (AI) and third (BI) terminals.

7. Plurality of signal switching circuits as in claim 5, characterized in that said circuits are cascaded with the first (AI) and fourth (BO) terminals of one circuit respectively coupled to the second (AO) and third (BI) terminals of the next circuit.

8. Plurality of signal switching circuits as in claim 7, characterized in that the two terminals (AI, BO; AO, BI) at an end of said cascade are coupled through a controlled interface circuit (IC1/10) to a bidirectional line (BP).

9. Plurality of signal switching circuits as in claim 8, characterized in that said controlled interface circuit (IC1/10) includes first means (NAND2, NOR4, PM2, NM2)

to regenerate and allow transmission of signals between said bidirectional line (BP) and one (AI; BI) of said two terminals (AI, BO; AO, BI) while transmission between the other (AO; BO) of these terminals and said bidirectional line is inhibited, and includes second means (INV13/15, NAND1, NOR3, PM1, NM1), to regenerate and allow transmission of signals between said other terminal (AO; BO) and said bidirectional line while transmission between said one terminal (AI; BI) and said bidirectional line is inhibited.

10. Matrix device according to claim 5, characterized in that said signal switching circuit (PG1/5, INV16/18) is realized as per claim 6.

11. Matrix device according to claim 10, characterized in that said shift register formed by said driver circuits (LD, HVD) is realized by the cascade connection of the signal switching circuits (PG1/5, INV16/18) as per claim 7.

12. Matrix device according to claim 11, characterized in that each of said driver units (FPDR) has a plurality of control terminals (I1/5, O1/5) to which said input signals (DATALC/R, DATRC/R, CLKC/R, FREQC/R, $\overline{\text{ENC/R}}$, SELC/R) may be applied, and among which at least one is coupled to a controlled interface circuit (IC1/10) as per any of the claims 8 or 9 via said bidirectional line (BP), said interface circuit being controlled by said direction control means (RLC).

13. Matrix device according to claim 12, characterized in that a plurality of driver units (FPDR) connected in series via said control terminals (I1/5, O1/5) are located along at least one side of said coordinate ----------

matrix (LCD).

14. Matrix device according to claim 10, characterized in that said logical means (LD1/30) further include combination means (PG6/7, XNR, NAND3, AND1/3, INV19/22) coupled to said signal memory circuit (INV16, INV18, PG5) and adapted to translate said input signals (DATALC/R, DATARC/R, CLKC/R, FREQC/R, $\overline{\text{ENC/R}}$, SELC/R) into a number of codes comprising a plurality of elements (IN1/3) controlling distinct one of a like plurality of circuits (HV1/3) forming a switching circuit (HVD) also included in said driver circuit (LD, HVD) and having said one line output terminal (OUT1/30) to which said output circuits are able to apply output signals (CSC, CC, CNC; RSC, RNSC, STROBE) defining the electrical state of the coupled line.

15. Matrix device according to claim 14, characterized in that said combination means (PG6/7, XNR, NAND3, AND1/3, INV19/22) are provided with latching means (PG7, INV20/21) for latching some of said input signals (DATALC/R, DATARC/R) under the control of other of said input signals ($\overline{\text{ENC/R}}$).

16. Switching circuit (HVD) able to selectively couple one out of at least three voltages at respective input terminals (+V1, -V2, OV) to a common output terminal (OUT), characterized in that first (HV1) and second (HV2) circuits coupling respectively the first (+V1) and the second (-V2) input terminals to said common output terminal (OUT) include at least one DMOS switch device (NM4), and that at least one third circuit (HV3) coupling the third input terminal (OV) to said common output terminal includes two DMOS switch devices (NM7/8) coupled in series opposition.

17. Switching circuit according to claim 16, characterized in that each of said circuits (HV1/3) further includes operating means (R8, NM3; R11, NM6) associated to the respective DMOS switch device(s) (NM4; NM7/8) and able to open said DMOS switch device(s) more rapidly than closing

it/them.

18. Switching circuit according to claim 16, characterized in that said circuits (HV1/3) are interconnected (T1, T2) and coupled to logical means (LD1/30) controlled by input signals (FREQC/R, SELC/R, $\overline{\text{ENC/R}}$) and able to generate a number of codes comprising three elements (IN1/3) each controlling a distinct one of said circuits.

19. Switching circuit according to claims 17 and 18, characterized in that each of said circuits (HV1/3) further includes a level translator (R5/6, P1; R9/10, P2) including an active device (P1; P2) coupled between said logical means (LD) and said operating means (R8, NM3; R11, NM6), and adapted to transform, together with said operating means, said elements (IN1/3) of said codes into control signals for said DMOS switch devices (NM4; NM7/8).

20. Switching circuit according to claim 19, characterized in that current flow through said DMOS switch devices (NM4; NM7/8), said operating means (R8, NM3; R11, NM6) and said active devices (P1; P2) of said level translators (R5/6, P1; R9/10, P2) is inhibited when said three elements (IN1/3) of said codes are such that the voltage at the third input terminal (OV) is applied to said common output terminal (OUT).

21. Switching circuit according to claim 19, characterized in that said first (HV1) and said second (HV2) circuits are identical and have their level translator (R5/6, P1) coupled to said said operating means (R11, NM6) of said third circuit (HV3) via first interconnection means (R7; R1, D3), the operating means (R8, NM3) of said first and second circuits being coupled to said level translator (R9/10, P2) of said third circuit via second interconnection means (T2), and that said third circuit controls said operating means of said first and second circuits via said first and second interconnection means.

22. Switching circuit according to claim 17,

characterized in that said DMOS switch devices are DMOS transistors (NM4; NM7/8) of same conductivity type (N-channel) and that said operating means (R8, NM3; R11, NM6) including a transistor (NM3; NM6) and a resistor (R8; R11) are able to make said associated DMOS transistor(s) (NM4; NM7/8) slowly conductive by charging its/their intrinsic gate capacitance towards a positive voltage (+V3; +V1) through said resistor and to rapidly block said DMOS transistor(s) by applying a negative voltage (-V2) to its/their gate electrode via the drain-to-source path of said transistor.

23. Switching circuit according to claims 21 and 22, characterized in that said negative voltage (-V2) is permanently applied to the source electrode of said transistor (NM3; NM6) of each of said operating means (R8, NM3; R11, NM6), that said transistor (NM3) included in said first (HV1) and second (HV2) circuits is controlled by a respective one of said level translators (R5/6, P1) and by said operating means (R11, NM6) of said third circuit (HV3) via said first interconnection means (R7; T1, D3), said transistor (NM6) of said third circuit being only controlled by said coupled level translator (R9/10, P2), and that said positive voltage (+V3; +V1) is permanently applied to one end of said resistor (R11) of said operating means (R11, NM6) included in said third circuit, and is applied to one end of said resistor (R8) of said operating means (R8, NM3) included in said first and second circuits by said level translator (R9/10, P2) of said third circuit via said second interconnection means (T2).

24. Matrix device according to claim 14, characterized in that said switching circuit (HVD) is realized as per any of the claims 16 to 23, each of said line output terminals (OUT1/30) being said common output terminal (OUT).

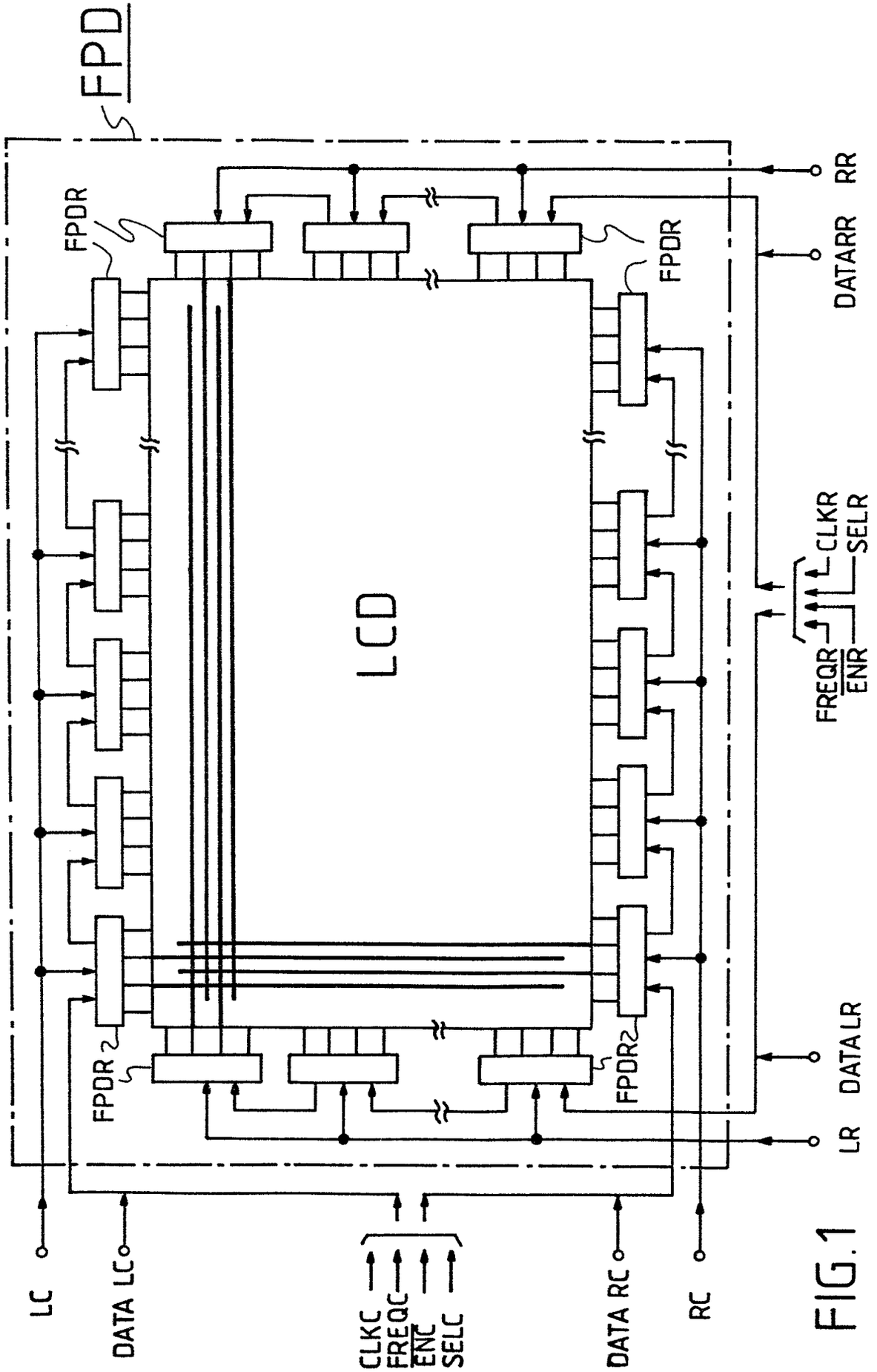

FPD
FPDR
FPDR
FPDR2
FPDR2
LCD
RR
DATARR
CLKR
SELR
FREQR
ENR
LR
DATALR
LC
DATA LC
CLKC
FREQC
ENC
SELC
DATA RC
RC

FIG.1

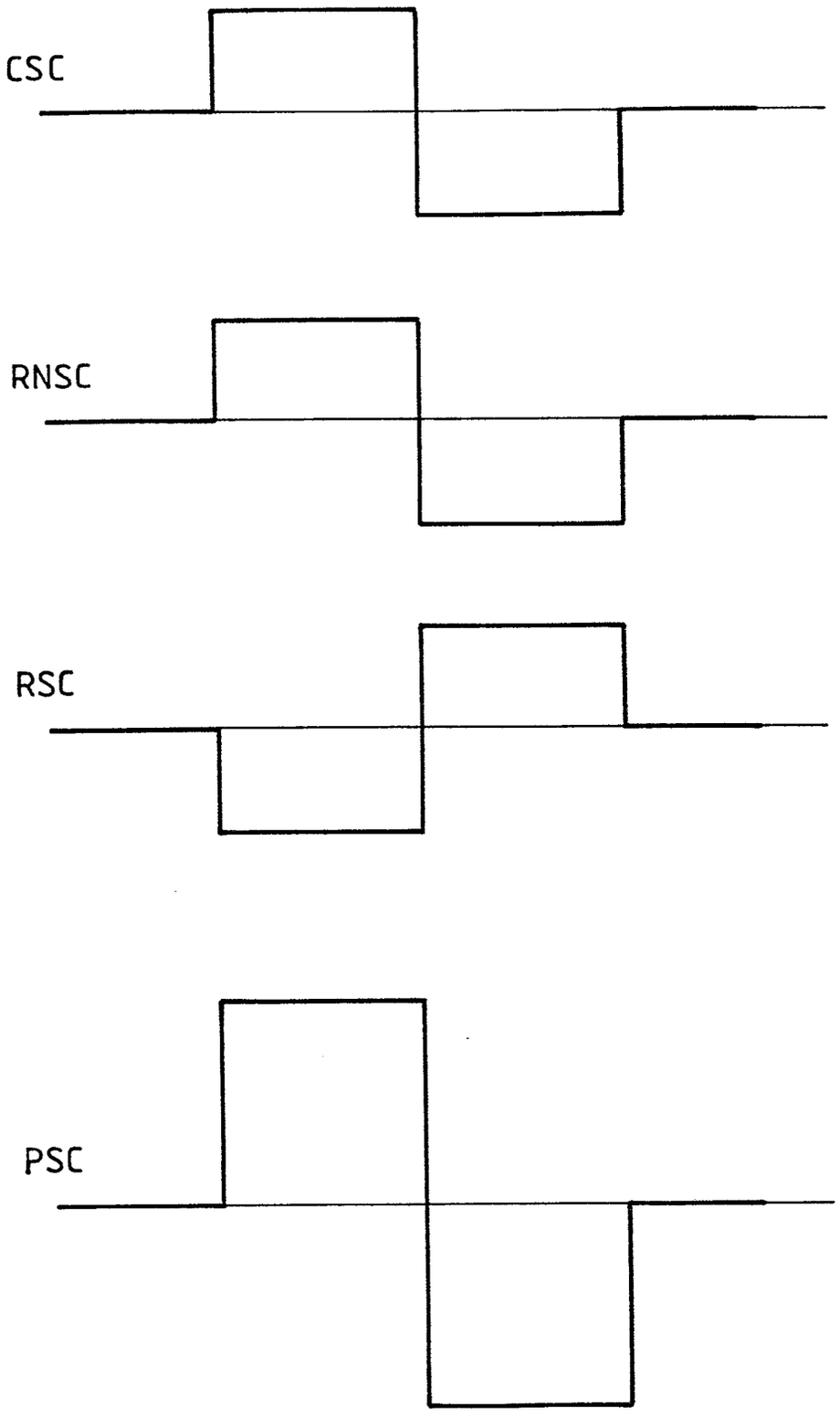


FIG. 2

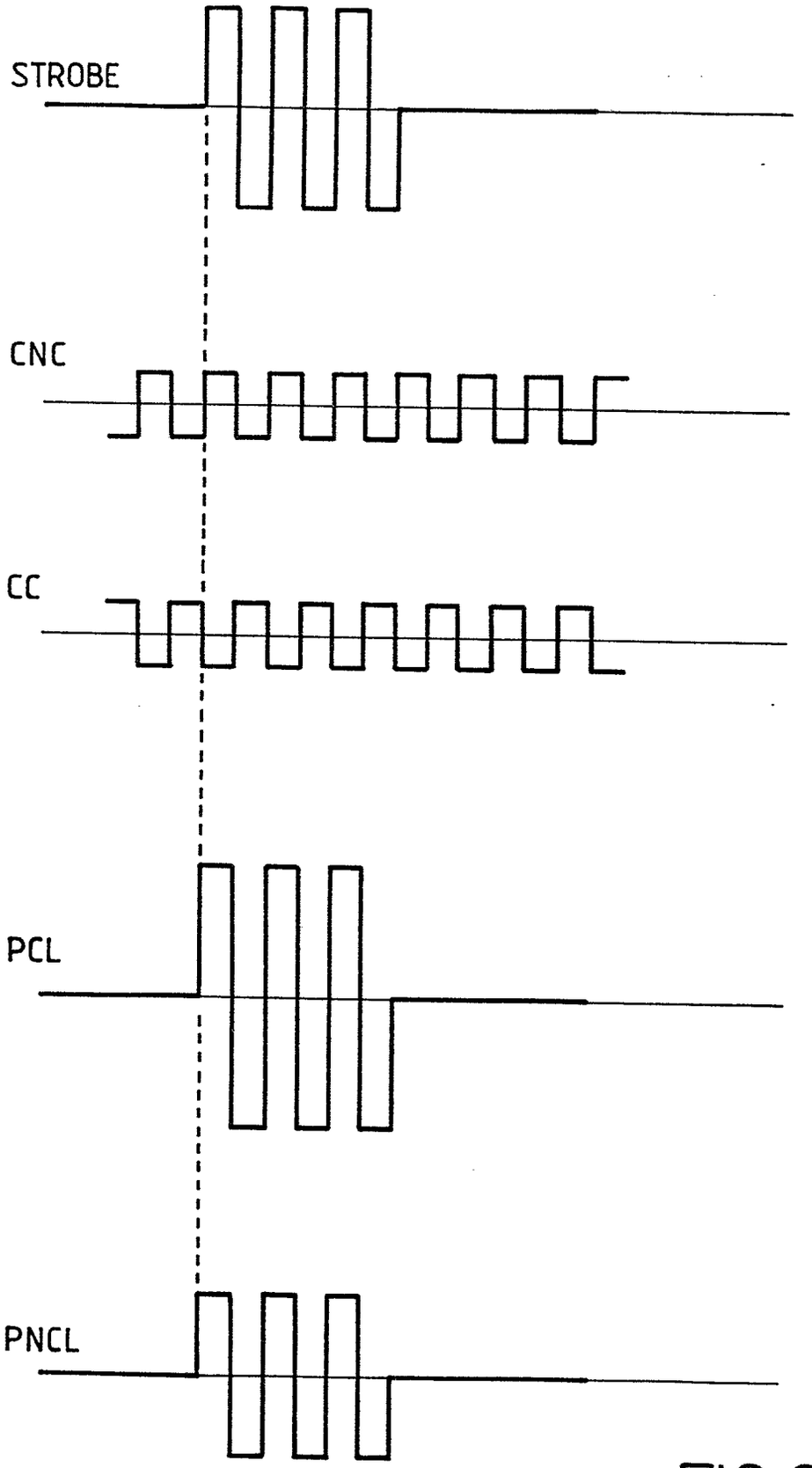


FIG.3

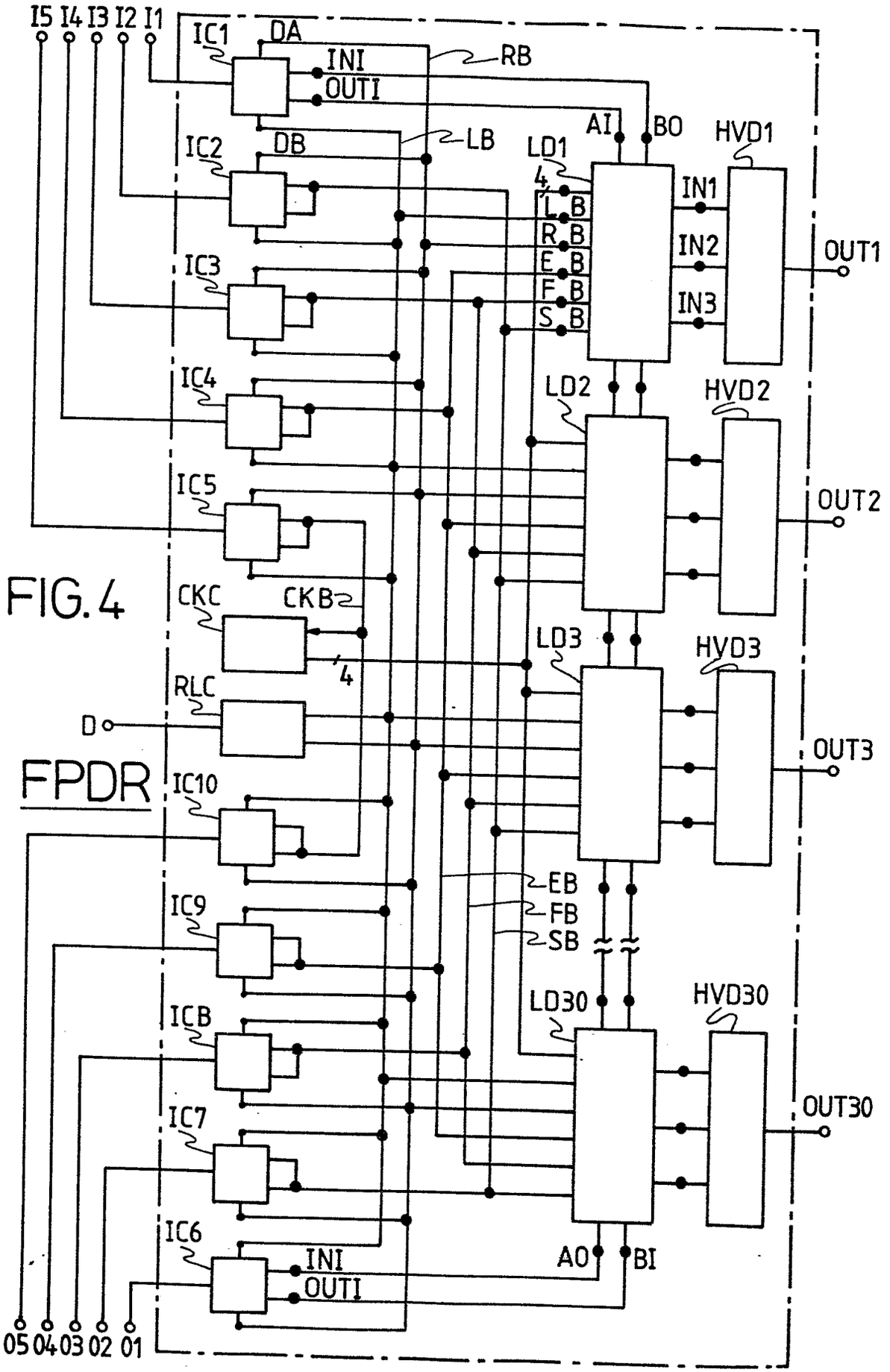

I5 I4 I3 I2 I1
IC1
DA
INI
OUTI
RB
AI
BO
HVD1
IC2
DB
LB
LD1
4
LB
RB
EB
FB
SB
IN1
IN2
IN3
OUT1
IC3
IC4
LD2
HVD2
IC5
OUT2
CKC
CKB
4
LD3
HVD3
RLC
D
OUT3
IC10
EB
FB
SB
IC9
LD30
HVD30
ICB
OUT30
IC7
IC6
INI
OUTI
AO
BI
05 04 03 02 01

FIG. 4

FPDR

RLC

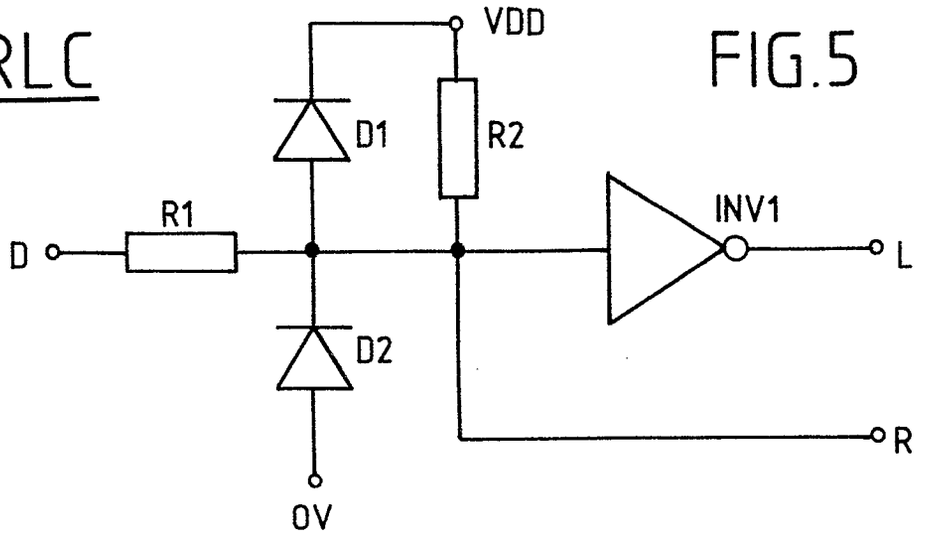


FIG.5

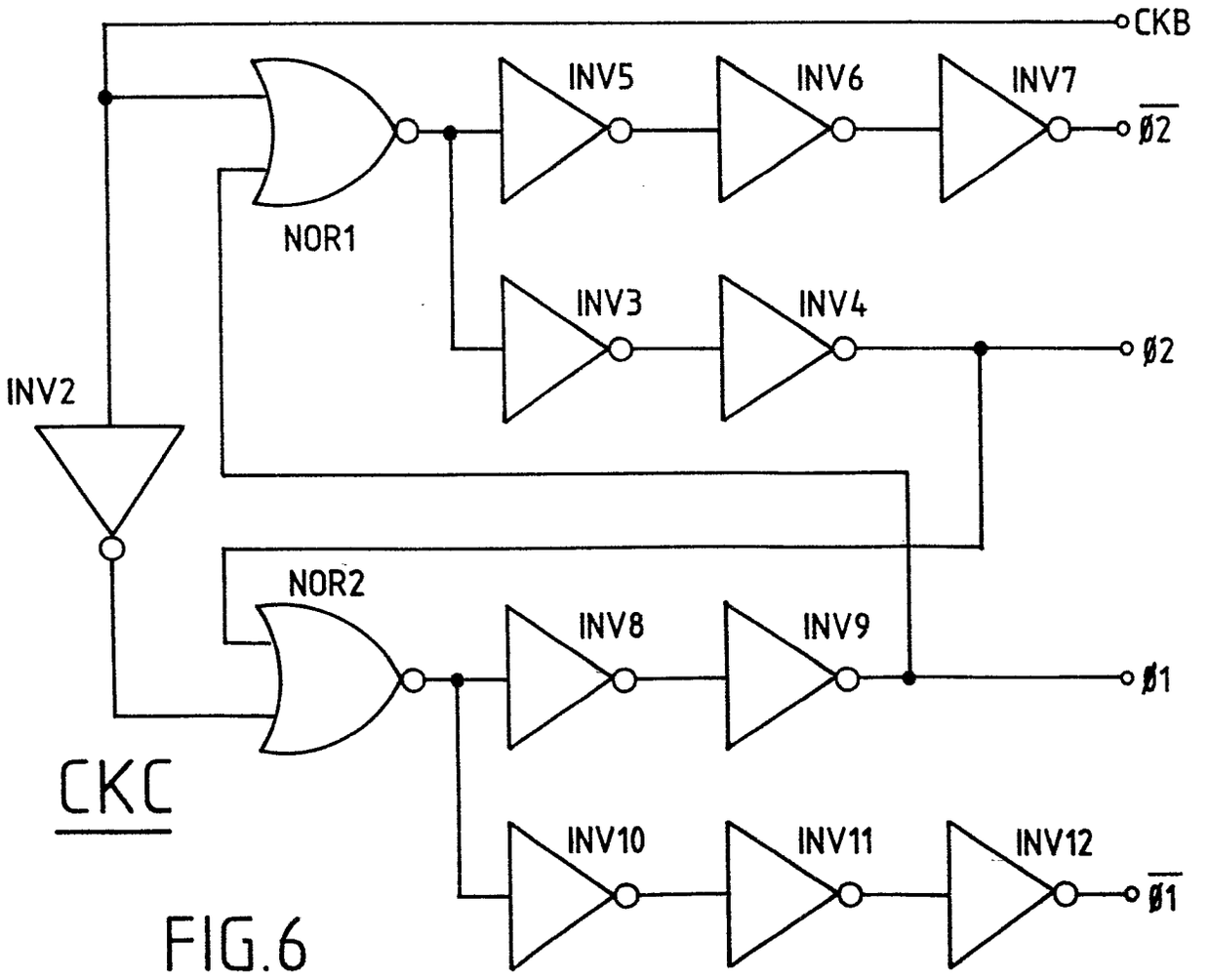
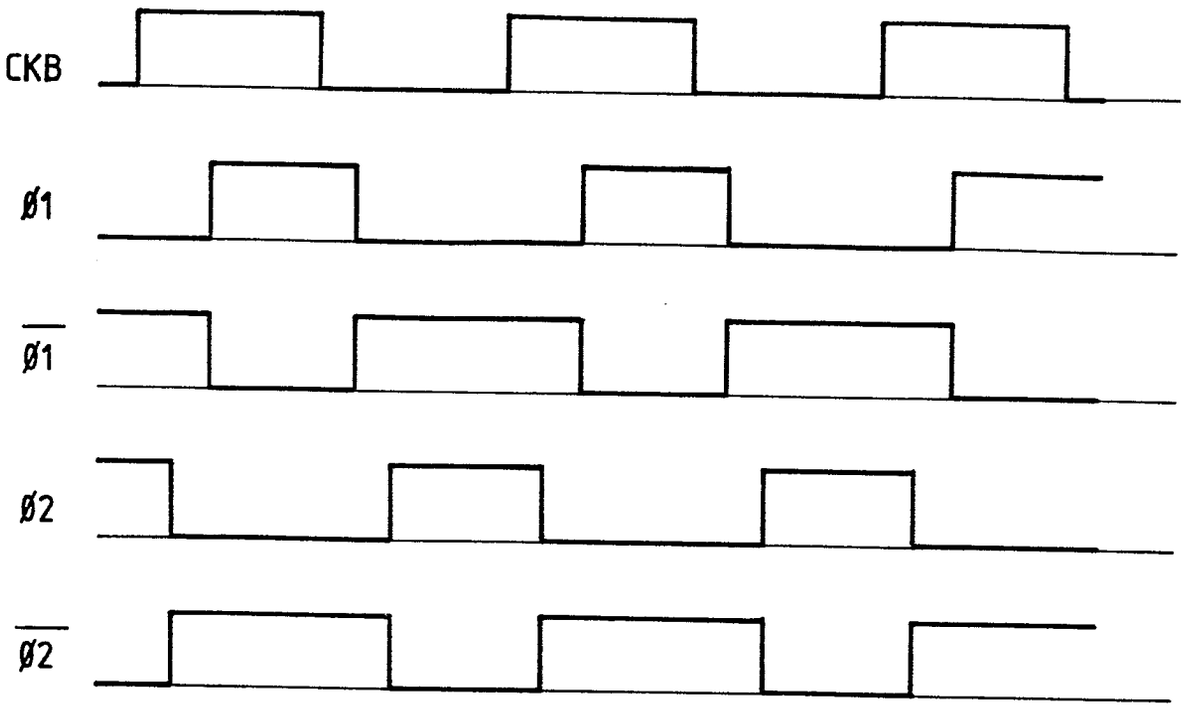
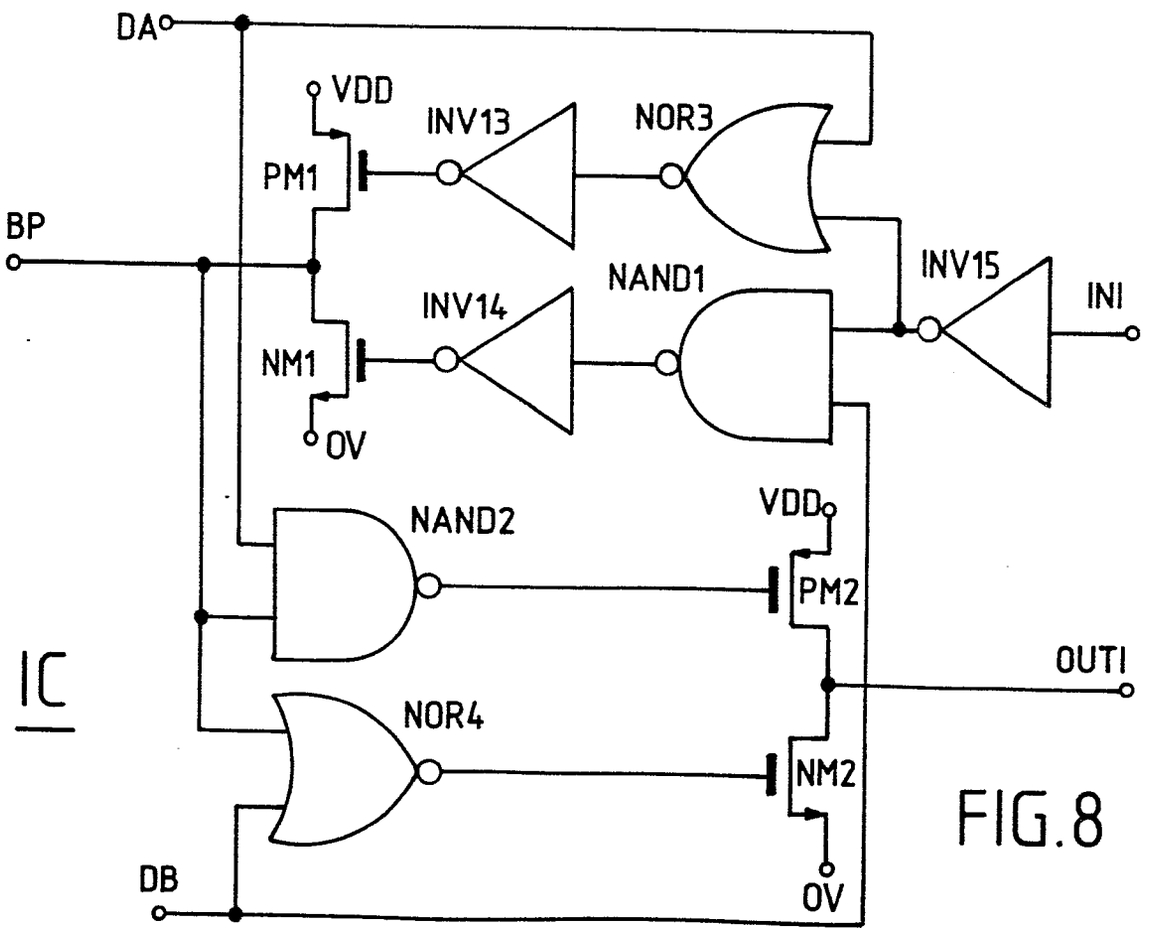


FIG.6

FIG.7


CKB
ø1
ø1
ø2
ø2


DA
VDD
INV13
NOR3
PM1
BP
INV15
NAND1
INV14
INI
NM1
OV
NAND2
VDD
PM2
OUTI
NOR4
NM2
DB
OV

IC

FIG.8

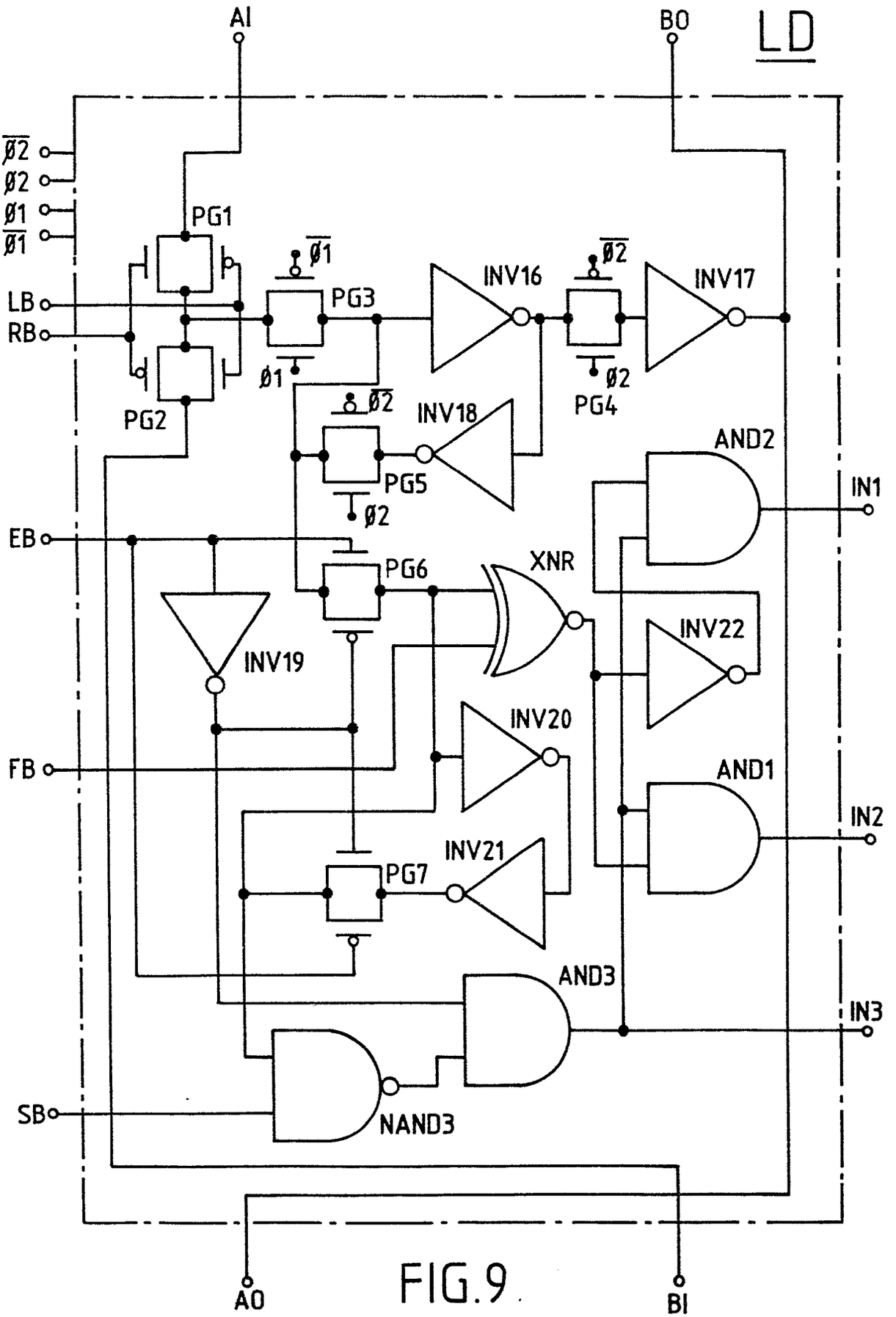
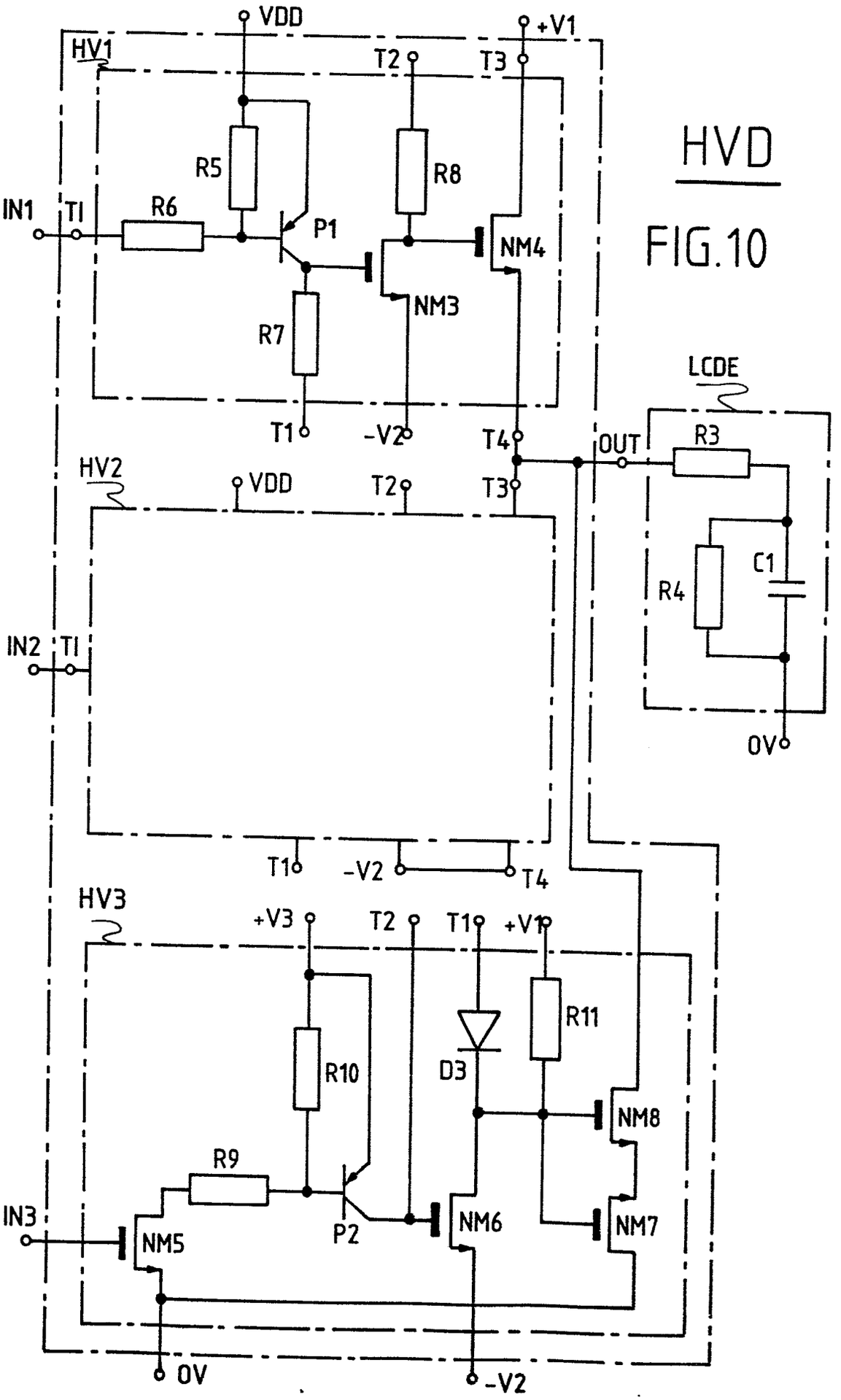

AI
BO
LD
Ø2
Ø2
Ø1
Ø1
PG1
LB
RB
PG3
INV16
INV17
PG2
PG4
INV18
AND2
PG5
IN1
EB
PG6
XNR
INV19
INV22
INV20
FB
AND1
IN2
INV21
PG7
AND3
IN3
SB
NAND3
AO
BI

FIG.9


VDD
+V1
HV1
T2
T3
R5
R8
IN1
TI
R6
P1
NM4
NM3
R7
T1
-V2
T4
OUT
LCDE
R3
HV2
VDD
T2
T3
C1
R4
IN2
TI
0V
T1
-V2
T4
HV3
+V3
T2
T1
+V1
R11
R10
D3
NM8
R9
IN3
NM5
P2
NM6
NM7
0V
-V2

HVD

FIG.10

0162969

European Patent Office

EUROPEAN SEARCH REPORT

Application number

EP 84 20 0778

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int Cl.4)
X	EP-A-0 078 402 (TOKYO SHIBAURA DENKI K.K.) * Figures 1-4; abstract; page 2, lines 13-27, page 3, line 22 - page 7, line 27 *	1,3,4	G 09 G 3/36

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

G 09 G 3/36

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18-04-1985	VAN ROOST L.L.A.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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