(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 163 875**
A1

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **85104679.7**

(22) Date of filing: **19.04.85**

(51) Int. Cl.⁴: **G 06 F 1/04**

(30) Priority: **08.06.84 US 618798**

(43) Date of publication of application: **11.12.85 Bulletin 85/50**

(84) Designated Contracting States: **DE FR GB**

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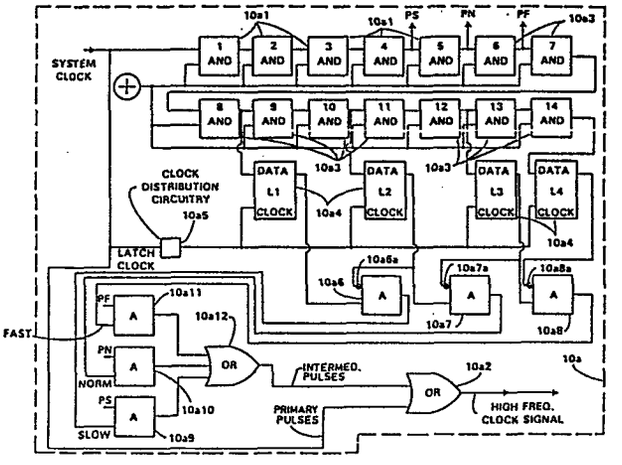
(54) Apparatus and method for stabilizing the frequency of a clock signal generated by an on-chip clock generator.

(57) For generating from a system clock a high frequency clock signal, the pulse generator has two consecutive delay lines (10a1, 10a3) and additional evaluating circuitry (10a4...10a12) to obtain the intermediate pulses in correct timing relationship with respect to the oroginal system clock pulses. Each of the consecutive system clock pulses propagates through the first (10a1) and into the second (10a3) delay line whose tap outputs are latched (11...L4) as delay indications when the next system clock pulse occurs. From tap outputs of the first delay line (PS, PN, PF) each system pulse can be obtained in several different time positions. The latched delay indications are evaluated in AND gates (10a6, 10a7, 10a8) to obtain three delay indicator signals (SLOW, NORM, FAST) of which only one is active. The delay indicator signals and the tap output signals of the first delay line are combined (10a9...10a12) to obtain an intermediate pulse that has a time position exactly between two consecutive system clock pulses.



APPARATUS AND METHOD FOR STABILIZING THE FREQUENCY OF A CLOCK SIGNAL GENERATED BY AN ON-CHIP CLOCK GENERATOR

The present invention pertains to improved on-chip clock signal generation, and more particularly, to clock signal generator circuitry for stabilizing the frequency of the generated clock signal, and to a method for generating a stabilized clock signal.

Some integrated circuit chips used in association with modern day computing systems include a clock signal generator circuit for generating a high frequency clock signal in response to a system clock signal generated from a source disposed external to the chip. The high frequency clock signal is used to coordinate the functioning of various circuits disposed on the chip, such as a processor circuit. The clock signal generator generates a primary output pulse from each pulse of the system clock that is received. However, the clock signal generator also generates an intermediate pulse disposed between each pair of primary pulses that are directly derived from the system clock pulses.

Due to the particular characteristics of the clock signal generator circuit, the frequency of the high frequency clock signal is not fixed. The position of the intermediate pulses within the high frequency clock signal varies. The position of the primary pulses within the high frequency clock signal does not vary since these pulses are generated in response to the system clock.

Computing systems of the prior art are not as fast, in terms of operating speed, as are modern day computing systems. Consequently, the non-fixed frequency of the

high frequency clock signal did not detrimentally affect the performance of the prior art computing systems. However, due to their faster operating speeds, the non-fixed frequency of the high frequency clock signal does detrimentally affect the performance of modern-day computing systems. In particular, the operational performance of the various circuits on the chip, such as the processor circuit, is detrimentally affected. Accordingly, an apparatus within the clock signal generator circuit is needed to stabilize the frequency of the high frequency clock signal generated from the clock signal generator.

Accordingly, it is a primary object of the present invention to provide an on-chip clock signal generator which includes circuitry for stabilizing the frequency of a clock signal generated by the clock signal generator.

It is a further object of the present invention to provide an on-chip clock signal generator which includes circuitry for stabilizing the frequency of the clock signal generated, the circuitry stabilizing the frequency of the clock signal by minimizing the variation in the position of intermediate pulses comprised in the clock signal.

These and other objects of the present invention are accomplished by a clock signal generator and a clock signal generation method as defined in the claims.

Further scope of applicability of the present invention will become apparent from the detailed description presented hereinafter. It should be understood, however, that the detailed description and the specific examples, while representing a preferred embodiment of the inven-

tion, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become obvious to one skilled in the art from a reading of the following detailed description.

A full understanding of the present invention will be obtained from the detailed description of the preferred embodiment presented hereinbelow, and the accompanying drawings, which are given by way of illustration only and are not intended to be limitative of the present invention, and wherein:

Figure 1 illustrates an integrated circuit chip including a high frequency clock signal generator and a processor circuit connected to the high frequency clock signal generator;

Figures 2a and 2b illustrate a system clock signal and a high frequency clock signal generated by the high frequency clock generator of Figure 1, respectively;

Figure 3 illustrates a prior art high frequency clock generator;

Figure 4 illustrates the high frequency clock generator in accordance with the present invention; and

Figure 5 illustrates the clock distribution circuitry of Figure 4.

Referring to Figure 1, an integrated circuit chip 10 is illustrated. The chip 10 includes a high frequency

clock generator 10a and a processor circuit 10b connected to the output of the high frequency clock generator 10a. The high frequency clock generator 10a receives a system clock signal from a source external to the chip 10 and generates a high frequency clock signal in response to the system clock. The processor 10b receives the high frequency clock signal and utilizes this signal to perform its intended function.

Referring to Figure 2a, a typical system clock signal 12 is illustrated. Referring to Figure 2b, a typical high frequency clock signal 14 is also illustrated. The system clock of Figure 2a includes a first pulse 12a, a second pulse 12b, and a third pulse 12c. The high frequency clock signal of Figure 2b also includes a first pulse 14a, a second pulse 14b, and a third pulse 14c. However, the high frequency clock signal further includes an intermediate pulse 14d.

The high frequency clock generator 10a of the prior art, as shown in Figure 1, generated a high frequency clock signal with a varying frequency. The frequency varied because the position of the intermediate pulse 14d within the high frequency clock signal 14 would not remain fixed. The intermediate pulse 14d would move from its intended mid-point to a point located either to the left or to the right of the mid-point, as indicated by the arrows 14d1 and 14d2. Consequently, the functioning of the processor 10b on chip 10 was detrimentally affected.

Referring to Figure 3, a detailed construction of a high frequency clock generator 10a of the prior art is illustrated. The high frequency clock generator 10a of

Figure 3 generates the high frequency clock signal 14 shown in Figure 2b, including the moving intermediate pulse 14d which causes the frequency of the high frequency clock signal 14 to vary. In Figure 3, the high frequency clock generator comprises a plurality of AND gates 10a1 connected together. The first AND gate 10a1 receives the system clock signal 12 at one of its input terminals and a high (binary 1) signal at its other input terminal. The high (binary 1) signal is tied to the other input terminal of each of the other AND gates 10a1 shown in Figure 3. The output terminal of the first AND gate 10a1 is connected to the one input terminal of the second AND gate 10a1; the output terminal of the second AND gate 10a1 is connected to the one input terminal of the third AND gate 10a1; the output terminal of the third and fourth AND gates 10a1 are connected to the one input terminal of the fourth and fifth AND gates 10a1, respectively. The output terminal of the fifth AND gate 10a1 is connected to one input terminal of an OR gate 10a2. The other input terminal of the OR gate 10a2 is connected directly to the system clock. The output signal generated by the OR gate 10a2 represents the high frequency clock signal 14 shown in Figure 2b.

In operation, the high frequency clock generator 10a of the prior art shown in Figure 3, functions in the following manner.

Each of the AND gates 10a1 represents a delay element in that each AND gate 10a1 includes an inherent amount of delay. However, the amount of delay inherent in an AND gate 10a1 depends upon a variety of factors peculiar to the AND gate. Suffice it to say, however, that the amount

of delay for each AND gate 10a1 varies, from one point in time to another.

When the first pulse 12a of the system clock is generated, the first pulse 12a is received by the other input terminal of OR gate 10a2 and is propagated directly therethrough thereby generating the first pulse 14a of the high frequency clock signal. However, at the same time, the first pulse 12a of the system clock is propagated through the plurality of AND gates 10a1 to the one input terminal of the OR gate 10a2. Since the amount of delay inherent in the AND gates 10a1 varies, the first pulse 12a may be received by the one input terminal of the OR gate 10a2 at a nominal point in time or at an earlier point in time or at a later point in time. Therefore, when an intermediate pulse is generated, it may or may not be generated by the OR gate 10a2 at a point mid-way between the first pulse 14a and the second pulse 14b of the high frequency clock signal. Utilizing second and third pulses 12b, 14b, 12c, 14c of Figure 2a and 2b, intermediate pulse 14d may be generated at a nominal point in time or at an earlier point in time or at a later pint in time, as indicated by arrows 14d1 and 14d2. When the second and third pulses 12b and 12c of the system clock are received by the high frequency clock generator 10a, they are propagated directly through the OR gate 10a2 to the output of the high frequency clock generator 10a yielding pulses 14b and 14c, that is, since the other input terminal of the OR gate 10a2 is connected directly to the source of the system clock, the second and third pulses 14b and 14c of the high frequency clock signal will be generated immediately in response to the second and third pulses 12b and 12c of the system clock. However, since the generation of the intermediate pulses

14d of the high frequency clock signal is dependant upon the characteristics of the delay elements (AND gates 10a1) shown in Figure 3, the intermediate pulse 14d may or may not be generated at a point which is mid-way between the second pulse 14b and the third pulse 14c of the high frequency clock signal 14. Therefore, the frequency of the high frequency clock signal 14 is not fixed with respect to the embodiment of the high frequency clock generator 10a shown in Figure 3. Therefore, the functioning of the processor circuit 10b shown in Figure 1 may be detrimentally affected. In order to remedy this deficiency, another embodiment of the high frequency clock generator 10a shown in Figure 1 is required.

Referring to Figure 4, a high frequency clock signal generator 10a, in accordance with the present invention, is illustrated. In Figure 4, the plurality of AND gates 10a1, as shown in Figure 3, is again illustrated. However, a second plurality of AND gates 10a3 is serially connected to the output of the original plurality of AND gates 10a1. The original plurality of AND gates 10a1 may be alternatively referred to as a preliminary delay line and the second plurality of AND gates 10a3 may be alternatively referred to as an additional delay line. For convenience of description, the AND gates 10a1 and 10a3 have been numbered sequentially from 1 to 14. In Figure 4, AND gates 1 through 14 are connected serially together. One output terminal is disposed between AND gates 4 and 5 and is labelled PS. Another output terminal is disposed between AND gates 5 and 6 and is labelled PN. Another output terminal is disposed between AND gates 6 and 7 and is labelled PF. With the exception of AND gate 14, the output terminal of each AND gate is connected to one

input terminal of the next sequentially connected AND gate. The one input terminal of AND gate 1 is connected to the system clock. The other input terminal of each AND gate (1-14) is connected to a high (binary 1) input signal source.

A plurality of latch circuits 10a4, consisting of latches L1, L2, L3, and L4, are connected to the output terminals of AND gates 8, 10, 12, and 14, respectively. For example, the data terminal of a latch circuit L1 is connected to the output terminal of AND gate 8. The data terminal of a latch circuit L2 is connected to the output terminal of AND gate 10. The data terminal of a latch circuit L3 is connected to the output terminal of AND gate 12. The data terminal of a latch circuit L4 is connected to the output terminal of AND gate 14. The clock terminals of latches L1, L2, L3, and L4 are connected to the system clock 12 via a clock distribution circuit 10a5. The output terminal of latch circuit L2 is connected to one input terminal of an AND gate 10a6 via an inverter 10a6(a). The output terminal of latch circuit L1 is connected to the other input terminal of AND gate 10a6. The output terminal of latch circuit L3 is connected to one input terminal of an AND gate 10a7 via an inverter 10a7(a). The other input terminal of AND gate 10a7 is connected to the output terminal of latch circuit L2. The output terminal of latch circuit L4 is connected to one input terminal of an AND gate 10a8 via an inverter 10a8(a). The other input terminal of AND gate 10a8 is connected to the output terminal of latch circuit L3. An AND gate 10a9 includes one input terminal connected to the PS output terminal and another input terminal connected to the output terminal of AND gate 10a6. An AND gate 10a10 includes one input terminal connected to the PN

output terminal and another input terminal connected to the output terminal of AND gate 10a7. An AND gate 10a11 includes one input terminal connected to the PF output terminal and another input terminal connected to the output terminal of AND gate 10a8. The output terminals of AND gates 10a9, 10a10, and 10a11 are connected to respective input terminals of an OR gate 10a12. The output terminal of OR gate 10a12 is connected to one input terminal of OR gate 10a2. The other input terminal of OR gate 10a2 is connected directly to the system clock. The output terminal of OR gate 10a2 provides the high frequency clock signal shown in Figure 2b; however, the position of the intermediate pulses 14d in this clock signal is more nearly fixed. Therefore, its frequency is also more nearly fixed.

The clock distribution circuit 10a5 of Figure 4 is illustrated again in Figure 5 of the drawings. The clock distribution circuit 10a5 receives a system clock pulse and generates a plurality of pulses in response thereto, each of which is approximately identical to the system clock pulse which energized the clock distribution circuit.

The functional operation of the high frequency clock signal generator 10a, according to the present invention, will be described in the paragraphs below with reference to Figure 4 of the drawings.

In Figure 4, pulses 12a, 12b, and 12c of the system clock are allowed to propagate through the chain of delay elements consisting of a plurality of AND gates 10a1 and 10a3. As previously mentioned, each AND gate 10a1 and

10a3 possesses a certain delay so that a signal propagating therethrough will be delayed by an amount corresponding to the certain delay. However, the amount of delay associated with each AND gate varies from one point in time to another depending upon a variety of factors. In Figure 4, it is assumed that the total delay associated with the plurality of AND gates 10a1 and 10a3 is greater than the cycle time (i.e. - the period) of the system clock. For the purposes of this discussion, a half-cycle delay is desired, that is, it is desired that the intermediate pulses of the high frequency clock signal be disposed at a mid-point between adjacent pulses of the high frequency clock signal.

When the first pulse 12a of the system clock is generated, the other input terminal of OR gate 10a2 is energized and the first pulse 12a is propagated through OR gate 10a2 representing the first pulse 14a of the high frequency clock signal. When the second pulse 12b of the system clock is generated, the other input terminal of OR gate 10a2 is energized and the second pulse 12b is propagated through OR gate 10a2 representing the second pulse 14b of the high frequency clock signal.

Assume that the AND gates 10a1 and 10a3 are operating slowly, that is, a significant amount of delay is attributable to each AND gate. The first pulse 12a of the system clock begins to propagate through the chain of AND gates 10a1 and 10a3. At some point in time during the propagation of the first pulse 12a through the chain of AND gates, the second pulse 12b of the system clock begins to propagate through the chain of AND gates 10a1 and 10a3.

Utilizing the assumption that the AND gates 10a1 and 10a3 are operating slowly, the first pulse 12a of the system clock may not yet have sufficiently propagated through the chain of AND gates 10a3, but nevertheless if may have energized already the data terminal of latch L1 of latches 10a4 simultaneously with the energization of the clock terminal of latch L1 by the second pulse 12b of the system clock. When this occurs, the output of latch L1 will be high (binary 1). However, if the first pulse 12a of the system clock which is propagating through AND gates 10a3 has not yet energized the data terminal of latches L2, L3, and L4, the output of latches L2, L3, and L4 is low (binary 0). Since the output of latch L1 is high and the output of latch L2 is low, due to the functioning of inverter 10a6(a), the output of AND gate 10a6 will be high but the outputs of AND gates 10a7 and 10a8 will be low. Consequently, the input terminal to AND gate 10a9 marked "SLOW" will be high, but the input terminals to AND gates 10a10 and 10a11 marked "NORM" and "FAST" will be low. When the second pulse 12b of the system clock, propagating through the chain of AND gates 10a1, arrives at the output of AND gate 4 of AND gates 10a1, the PS output terminal goes high (binary 1). Therefore, the input terminal to AND gate 10a9 marked "PS" will also be high. Because the input terminal to AND gate 10a9 marked "SLOW" is also high, AND gate 10a9 will develop an output signal; however, AND gates 10a10 and 10a11 will not be developing output signals. The output signal from AND gate 10a9 will propagate through OR gates 10a12 and 10a2 representing an intermediate pulse 14d, this intermediate pulse being disposed approximately mid-way between the second pulse 12b of the system clock and a third pulse 12c of the system clock. Even though the AND gates 10a1 and 10a3 are operating slowly, causing

an appreciable amount of delay for the intermediate pulse as it propagates through the chain of AND gates 10a1 and 10a3, the position of latch circuit L1 near the front end of AND gates 10a3 coupled with the early receipt of output signal PS by AND gate 10a9 will cause the intermediate pulse 14d to be disposed near a mid-point between the second pulse 12b and a third pulse 12c of the system clock.

Assume that the AND gates 10a1 and 10a3 are operating fast, that is, a small amount of delay is attributable to each AND gate. The first pulse 12a of the system clock begins to propagate rapidly through the chain of AND gates 10a1 and 10a3. At some point in time during the propagation of the first pulse 12a through the chain of AND gates, the second pulse 12b of the system clock begins to propagate rapidly through the chain of AND gates 10a1 and 10a3.

Utilizing the assumption that the AND gates 10a1 and 10a3 are operating fast, the first pulse 12a of the system clock may have propagated through the greater portion of the chain of AND gates 10a3, and thus may have energized the data terminals of latches L1, L2, and L3 simultaneously with the energization of the clock terminals of latches L1, L2, and L3, respectively, by the second pulse 12b of the system clock, causing the outputs of latches L1, L2, and L3 to go high (binary 1). If the first pulse 12a has not yet propagated far enough through the chain of AND gates 10a3 to energize the data terminal of latch L4, the output of latches L1, L2, and L3 will be high (binary 1) but the output of latch L4 will be low (binary 0). Since the output of latches L1, L2, and L3 are high and the output of latch L4 is low, due to the

functioning of inverter 10a8(a), the output of AND gate 10a8 will be high but the outputs of AND gates 10a6 and 10a7 will be low.

Consequently, the input terminal to AND gate 10a11 marked "FAST" will be high, but the input terminals to AND gates 10a9 and 10a10 marked "SLOW" and "NORM" will be low. Since the AND gates 10a1 are operating fast, the output terminal "PF" will be high when the input terminal to AND gate 10a11 marked "FAST" is also high. Therefore, AND gate 10a11 will develop an output signal; however, AND gates 10a9 and 10a10 will not be developing output signals. The output signal from AND gate 10a11 will propagate through OR gates 10a12 and 10a2 representing an intermediate pulse 14d, this intermediate pulse being disposed between the second pulse 12b of the system clock and a third pulse 12c of the system clock. Even though the AND gates 10a1 and 10a3 are operating fast, causing a small amount of delay for the intermediate pulse as it propagates through the chain of AND gates 10a1 and 10a3, the position of latch circuit L4 near the back end of AND gates 10a3 coupled with the late receipt of output signal PF by AND gate 10a11 will cause the intermediate pulse 14d to be disposed near a mid-point between the second pulse 12b and a third pulse 12c of the system clock.

This process will repeat itself with respect to the intermediate pulse of the high frequency clock signal disposed between the third and fourth pulses of the system clock, with respect to the intermediate pulse disposed between the fourth and fifth pulses of the system clock, et cetera. Since the intermediate pulses of the high frequency clock signal are disposed near a mid-point between the adjacent pulses of the system clock, the frequency of the high frequency clock signal

is more nearly fixed. The functioning of the processor circuit 10b and other circuits on the chip are not detrimentally affected. Higher speed computing systems, using this high frequency clock signal, will perform effectively due to the fixed frequency of the clock signal.

C L A I M S

1. A clock signal generator for developing a clock signal (14) in response to a system clock signal (12) received from a system clock generating means, the system clock signal including consecutive pulses (12a, 12b, 12c), characterized by

preliminary delay line means (10a1) responsive to the pulses of the system clock signal for developing output signals (PS, PN, PF) indicative of the position of each pulse in the preliminary delay line; and

means (10a3...10a12) connected to the preliminary delay line means (10a1) and responsive to the output signals (PS, PN, PF) developed therefrom for stabilizing the frequency of the clock signal (14) generated by the clock signal generator.

2. The clock signal generator of claim 1 characterized in that

the clock signal (14) comprises a plurality of primary pulses (14a, 14b, 14c) generated immediately in responsive to the pulses (12a, 12b, 12c) of the system clock (12) and a plurality of additional intermediate pulses (14d) disposed, respectively, between adjacent ones of the plurality of primary pulses; and that

the means for stabilizing (10a3...10a12) minimizes the variation in the position of the intermediate pulses (14d) disposed intermediate adjacent primary pulses (14b, 14c) of the clock signal.

3. The clock signal generator of claim 2, characterized in that the means for stabilizing (10a3...10a12) comprises:

additional delay line means (10a3) connected serially to said preliminary delay line means (10a1),

position determining means (10a4...10a8) connected to said additional delay line means for determining the position, within the additional delay line means, of the first pulse (12a) of each triple of system clock pulses (12a, 12b, 12c) and for generating output signals indicative of said position,

intermediate pulse generating means (10a9...10a12) responsive to the output signals from the preliminary delay line means (10a1), which output signals are indicative of the position, within the preliminary delay line means, of the second pulse (12b) of each triple of system clock pulses (12a, 12b, 12c), and to the output signals from the position determining means, for generating an intermediate pulse (14e) in response thereto, the intermediate pulse being generated at a point in time approximately mid-way between the second (12b) and the third (12c) of each triple system clock pulses.

4. The clock signal generator of claim 3, further characterized by

receiving means (10a2) connected to the intermediate pulse generating (10a9...10a12) means and to the system clock generating means for receiving the pulses (12a, 12b, 12c) of the system clock from the system clock

generating means and for generating primary pulses (14a, 14b, 14c) of the clock signal in response thereto, the receiving means receiving each intermediate pulse from the intermediate pulse generating means and generating intermediate pulses of the clock signal in response thereto,

whereby each intermediate pulse of the clock signal is positioned approximately mid-way between the primary pulses of the clock signal thereby fixing the frequency of the clock signal being generated by the clock signal generator.

5. Method for generating a stabilized clock signal from a system clock signal by inserting intermediate pulses between the original system clock signal pulses, characterized by the steps of:

- feeding the original system clock signal pulses to a two-part delay chain;

- deriving from tap output signals of the second part of the delay chain signals (SLOW, NORM, FAST) indicative of the relative delay of a first pulse (12a) of each pair (12a, 12b) of consecutive system clock signal pulses;

- obtaining as tap output signals of the first part of the delay chain auxiliary signals (PS, PN, PF) representing, in various delayed time positions, a second pulse (12b) of each pair of system clock pulses;

- selecting one of the auxiliary signals (PS, PN, PF) in response to the indicative signals as an intermediate clock signal; and

- combining the original system clock signal pulses and the generated intermediate clock signal pulses to obtain the desired stabilized clock signal.

6. The method of claim 5, further characterized in that the step of deriving indicative signals (SLOW, NORM, FAST) comprises the steps of:

- latching selected tap output signals of the second part of the delay chain in response to the occurrence of each original pulse (12b) of the system clock signal to obtain an indication of how far a preceding system clock signal pulse (12a) has propagated through the delay chain; and

- evaluating the latched signals to obtain the signals (SLOW, NORM, FAST) indicative of the relative delay of said preceding pulse (12a) in the delay chain.

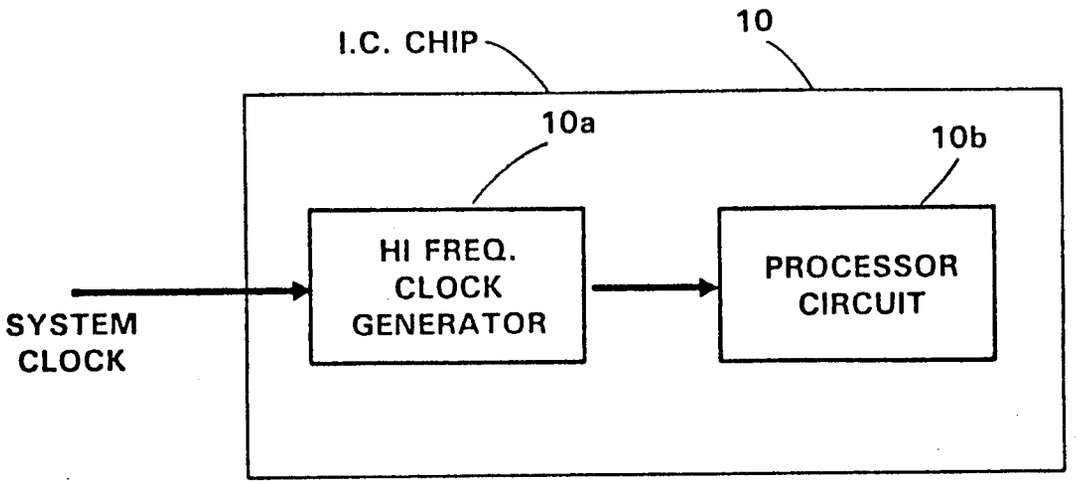


FIGURE 1

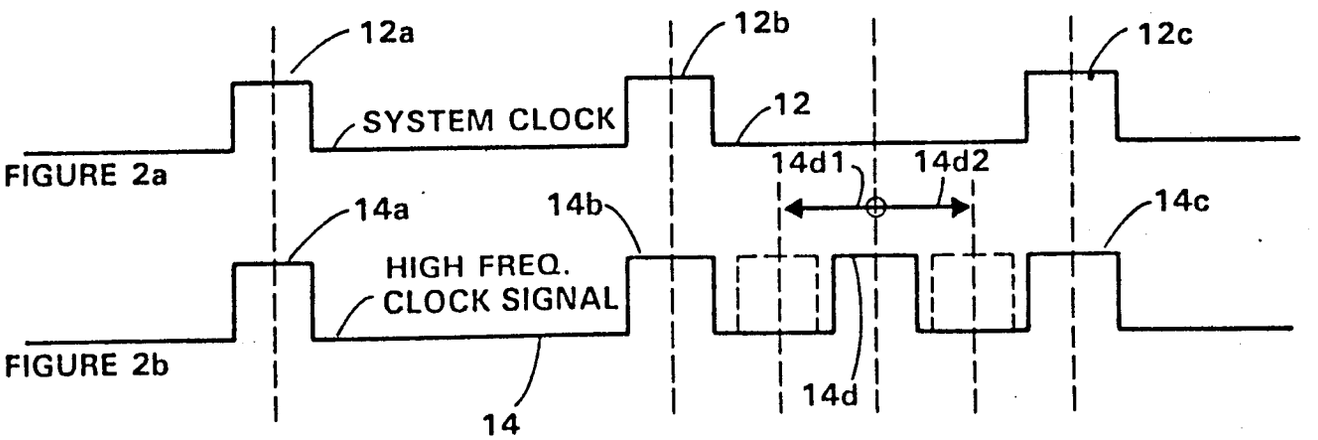


FIGURE 2a

FIGURE 2b

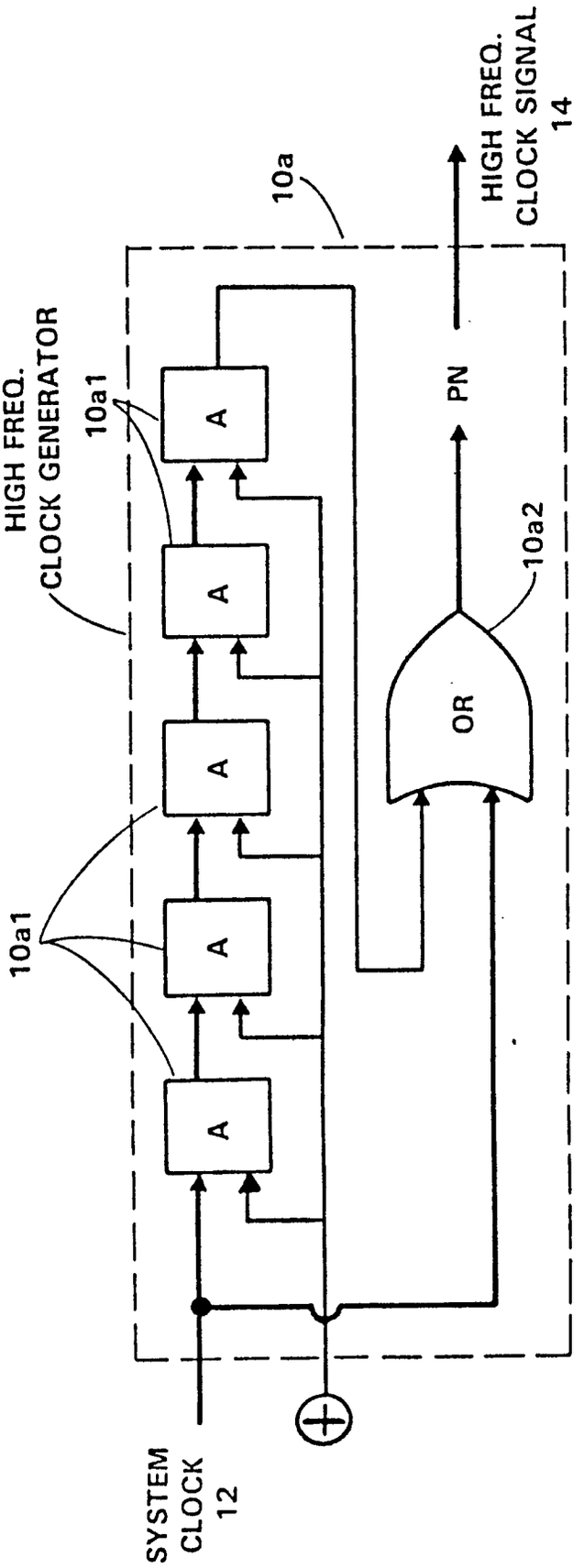


FIGURE 3
PRIOR ART

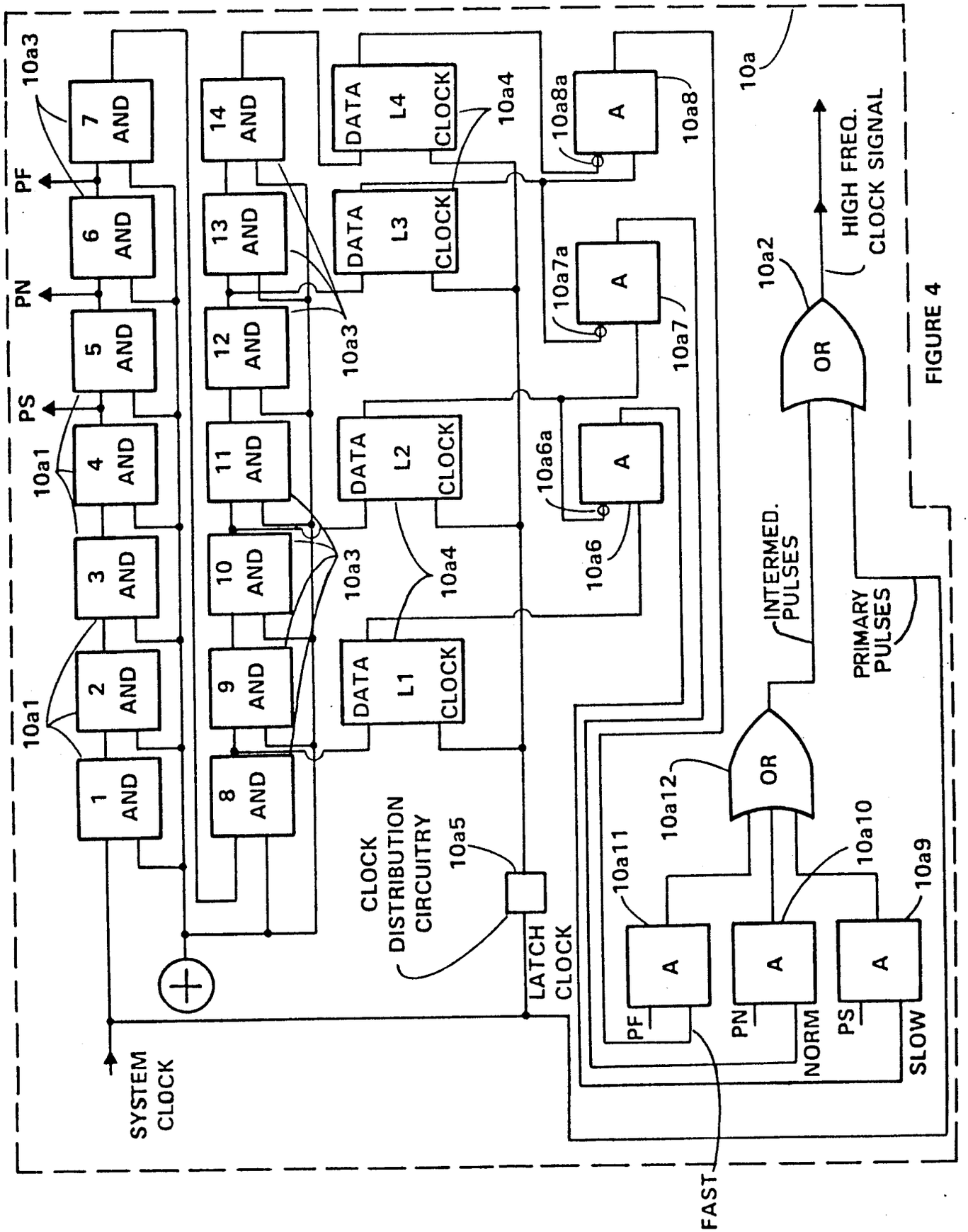

10a
10a3
7 AND
6 AND
5 AND
4 AND
3 AND
2 AND
1 AND
14 AND
13 AND
12 AND
11 AND
10 AND
9 AND
8 AND
PF
PN
PS
10a1
DATA L4 CLOCK
DATA L3 CLOCK
DATA L2 CLOCK
DATA L1 CLOCK
10a4
10a8a
A
10a8
10a7a
10a7
10a6a
10a6
10a2
OR
HIGH FREQ. CLOCK SIGNAL
INTERMED. PULSES
PRIMARY PULSES
CLOCK DISTRIBUTION CIRCUITRY
10a5
LATCH CLOCK
SYSTEM CLOCK
10a12
10a11
10a10
10a9
PF
PN
PS
NORM
SLOW
FAST

FIGURE 4

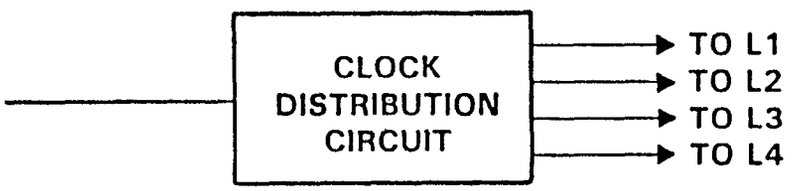


FIGURE 5

European Patent Office

EUROPEAN SEARCH REPORT

0163875
Application number

EP 85 10 4679

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X,Y	US-A-3 027 468 (GENERAL PRECISION INC., HILL et al.) * Column 1, lines 55-61; column 2, lines 48-63; column 10, lines 7-15,28-32,38-46,54-58; column 12, lines 36-48 *	1,5	G 06 F 1/04
A		2	

Y	US-A-3 593 158 (CONTROL DATA CO., DAY et al.) * Figure 1 *	5	

Y	PATENTS ABSTRACTS OF JAPAN, vol. 8, no. 51(P-259)[1488], 8th March 1984; & JP - A - 58 201 123 (TOKYO SHIBAURA DENKI) 22-11-1983 * Abstract; figure 1 *	5	TECHNICAL FIELDS SEARCHED (Int. Cl.4)
A	Idem	1-4	G 06 F H 03 K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26-07-1985	GORDON M.

CATEGORY OF CITED DOCUMENTS

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