(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 165 539**
A3

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **85107136.5**

(22) Date of filing: **11.06.85**

(51) Int. Cl.⁴: **G 06 F 15/347**

(30) Priority: **22.06.84 US 623602**

(43) Date of publication of application: **27.12.85 Bulletin 85/52**

(84) Designated Contracting States: **AT DE FR GB**

(88) Date of deferred publication of search report: **27.07.88 Bulletin 88/30**

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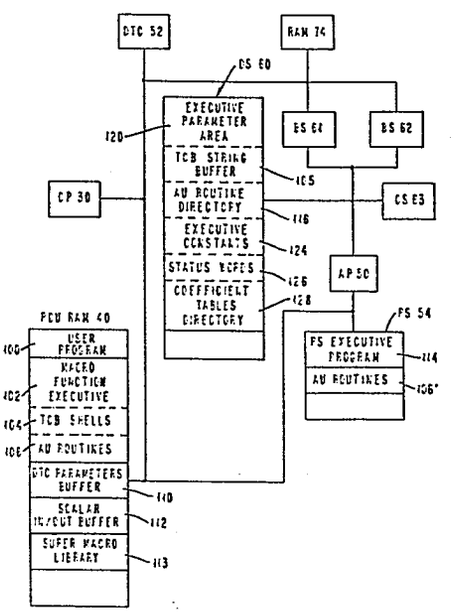
(54) Virtual vector registers for vector processing system.

(57) A working or buffer store (61, 62) is connected between a main or bulk store (74) and a vector processing unit (50). The buffer store contains one or more virtual vector registers operable under user control in register-to-register (RR) vector operations. A user instruction specifies the length of a vector operand to be processed, the type of operation to be performed, and which vector registers will be used. Vector processing is controlled by a series of programs (106) defined at the code level of the processing unit where for a given function or operation, the same program is used for both register-to-register and storage-to-storage processing. The latter processing is controlled by passing predetermined parameters to the program whereas register-to-register processing is controlled by passing parameters generated in response to user program instructions.



EP 0 165 539 A3

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EUROPEAN SEARCH REPORT

0165539

Application Number

EP 85 10 7136

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	K. HWANG et al.: "Computer Architecture and Parallel Processing", section 4.4.5, 1984, pages 293-297, McGraw-Hill Book Co., New York, US * Page 295, lines 8-18 *	1-3	G 06 F 15/347 G 06 F 15/06
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 23, no. 4, September 1980, pages 1720-1724, New York, US; J. HUANG et al.: "Vector mode computation" * Page 1721, line 11 - page 1723, line 8 *	1,4	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 22, no. 6, November 1979, pages 2317-2318, New York, US; P.G. CASPERS et al.: "Cache-resident processor registers" * Whole article *	1	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 26, no. 2, July 1983, pages 511-514, New York, US; T.K.M. AGERWALA et al.: "Register renaming for vector processors" * Page 511, lines 1-20 *	1	TECHNICAL FIELDS SEARCHED (Int. Cl.4) G 06 F 15/06 G 06 F 9/38 G 06 F 12/08
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 23, no. 7B, December 1980, pages 3480-3483, New York, US; J.W. HUANG et al.: "Dynamically reconfigurable vectors" * Whole article *	1	
E	EP-A-0 114 304 (IBM) * Page 2, line 30 - page 5, line 25 *	1,4	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	20-04-1988	QUESSON C.J.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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