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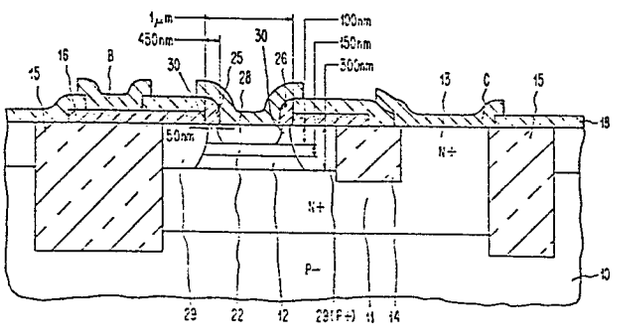
(54) High performance bipolar transistor having a lightly doped guard ring disposed between the emitter and the extrinsic base region.

(57) The present invention relates to a novel semiconductor device, such for example, an NPN bipolar transistor including a standard highly doped N^+ emitter (28) separated on its sidewalls from the P^+ extrinsic base region (29) (base contact reach through) by a guard ring shaped region (30) having a significantly lower impurity concentration than the emitter (e.g. N^-). Said region (30) is located beneath an insulating spacer (25).

The initial steps of the process are basically standard. The extrinsic base (29) is formed from a boron doped polysilicon contact region (16). The N^+ emitter region (28) is self aligned with the P^+ polysilicon contact region (16), and remains separated thereof by said N^- region (30). The N^+ emitter (28) is formed either using ion implantation techniques or a doped emitter polysilicon contact region. However, according to the teachings of the present invention, the intrinsic base (22) of the transistor is formed in situ, by a low dose low energy P type ion implantation through a mask, made with its concentration peak below the device surface. Subsequently, an intermediate N^- region is formed by implanting N type impurities through the same mask just to convert superficially the conductivity of the top surface above the P intrinsic base into N^- type. The N^+ emitter may be then formed in such a way it is separated from the extrinsic base by a guard ring shaped portion (30) of said lightly doped intermediate N^- region. The transistor thus formed will have a controllable narrow base width and optimized concentration, and will exhibit desired low external resistance through the extrinsic base region. Both factors are essential to provide high speed and low power devices.

In addition, this transistor has a significantly high β factor (in the range of 150) with a limited modulation of said gain factor; it has also good Emitter-Base breakdown voltages (in the range of 6V).

Lastly, it presents increased inverse β which is a highly desirable factor for Merged Transistor Logic (MTL) applications.



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EUROPEAN SEARCH REPORT

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Application number

EP 85 10 5728

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X	PATENT ABSTRACTS OF JAPAN, vol. 6, no. 12 (E-91)[[890], 23rd January 1982; & JP-A-56 135 965 (NIPPON DENKI K.K.) 23-10-1981 * Abstract; figures *	1,2	H 01 L 29/08 H 01 L 29/72 H 01 L 29/06
A	Idem	3	
D,A	US-A-4 252 582 (IBM) * Abstract; figure 9 *	1-3	
A	FR-A-2 267 641 (SONY CORP.) * Figure 3 * & US-A-4 000 506 (Cat. D,A)	1,2	
D,A	US-A-4 381 953 (IBM) * Whole document *	1,3,6, 8	TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30-06-1987	BAILLET B.J.R.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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