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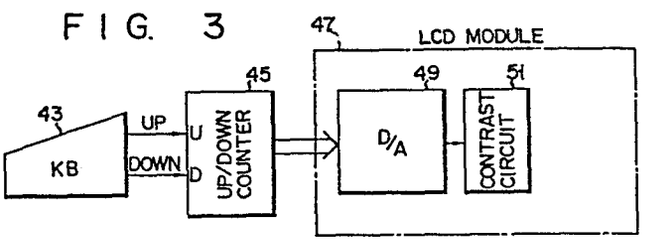
(54) **Digital contrast control circuit for display unit.**

(57) A digital contrast control circuit for a display unit according to the present invention has an up/down counter (45) for performing up- or down-count operations in response to a contrast control key signal supplied from a contrast control key arranged on a keyboard (43). A digital contrast output from the up/down counter is supplied to a D/A converter (49) arranged within a liquid crystal display unit (47). The D/A converter converts the digital contrast output to an analog contrast signal.

FIG. 3



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Digital contrast control circuit for display unit

The present invention relates to a digital contrast control circuit for a display unit.

Recent developments in microcomputers are rapid. Along with this, extensive studies on hand-held computers have been made. In a hand-held computer of this type, as shown in Fig. 1, a central processing unit (CPU) 9, a direct memory access controller 13 for performing high-speed data transfer, a main memory 15, a keyboard controller 19 for controlling a keyboard unit 17, a floppy disk controller 23 for controlling a micro floppy disk unit 21, a communication controller 33 for controlling a modem 31, and a display controller (LCDC) 37 for controlling a display unit (LCD module) 35 are connected through an address bus 1, a data bus 3 and a control bus 5.

The display unit 35 conventionally comprises a low-power liquid crystal display. In order to control the contrast of the conventional liquid crystal display unit 35, a contrast control line 41 of the liquid crystal display unit 35 is connected to the slider of a potentiometer 39 to change the voltage on the contrast control line 41 as shown in Fig. 2.

In this conventional method, however, noise tends to occur considerably to degrade the reliability of such a display unit, resulting in inconvenience. In

addition, since the user frequently adjusts contrast, demands has arisen for a highly reliable contrast control.

An object of the present invention is to provide a simple, highly reliable digital contrast control circuit for a display unit.

To achieve the above object, a digital contrast control circuit for a display unit according to the present invention comprises:

key input means, having at least first and second keys, for generating an increment signal when said first key is depressed and a decrement signal when said second key is depressed;

counting means for receiving the increment and decrement signals from said key input means, incrementing a count in response to the increment signal and decrementing the count in response to the decrement signal; and

a D/A converter for converting a digital output generated by said counting means to an analog signal.

A more complete understanding of the advantages, structure and operation of the present invention may be had by referring to the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing an example of hand-held computer to which the display contrast control circuit for display unit of the present invention applies;

Fig. 2 is a schematic view of a prior art display contrast control circuit; and

Fig. 3 is a block diagram showing an embodiment of the present invention.

Fig. 3 is a block diagram of a digital contrast control circuit for a display unit according to an embodiment of the present invention. Referring to Fig. 3, a keyboard 43 has two keys (not shown) for

controlling the contrast. The first contrast key serves to emphasize the contrast. When the first key is continuously depressed, the contrast is continuously increased. The second contrast key serves to deemphasize the contrast. When the second contrast key is continuously depressed, the contrast is continuously decreased. An up signal generated upon depression of the first contrast key or a down signal generated upon depression of the second contrast key is supplied to an up or down input terminal, respectively, of an up/down counter 45. The up/down counter 45 performs an up- or down-count operation upon reception of the up or down signal, respectively, from the keyboard 43. A digital count output from the up/down counter 45 is supplied to a D/A converter 49. The D/A converter 49 converts the digital count output from the up/down counter 45 to an analog signal. The analog signal from the D/A converter 49 is supplied to a contrast circuit 51 in a liquid crystal display module (LCD module) 47, thereby performing contrast control.

In the above embodiment, the up/down counter comprises a hardware counter. However, the up/down counter may comprise a software counter in place of the hardware counter. That is, in Fig. 1, the CPU 9 may count the increment and decrement signals supplied from said key input means and stores the counted value into the main memory 15.

In the embodiment described above, the display contrast control circuit of the present invention is applied to a display unit in a hard-held computer. However, the present invention may be applied to any display unit in any device.

While the display contrast control circuit for display unit has been described in reference to a particular embodiment, and as being used to a certain computer, it is to be understood that further modifications, alterations, and manipulations may be

made and practiced by those having ordinary skill in the art without departing from the spirit and scope of the present invention.

Claims:

1. A digital contrast control circuit for a display unit, comprising:

key input means (43), having at least first and second keys, for generating an increment signal when said first key is depressed and a decrement signal when said second key is depressed;

counting means (45) for receiving the increment and decrement signals from said key input means, incrementing a count in response to the increment signal and decrementing the count in response to the decrement signal; and

a D/A converter (49) for converting a digital output generated by said counting means to an analog signal.

2. A circuit according to claim 1, characterized in that said counting means comprises:

a central processing element (9) for counting the increment and decrement signals supplied from said key input means (43); and

storage means (15) for storing the count.

3. A circuit according to claim 1, characterized in that said counting means (45) comprises an up/down counter.

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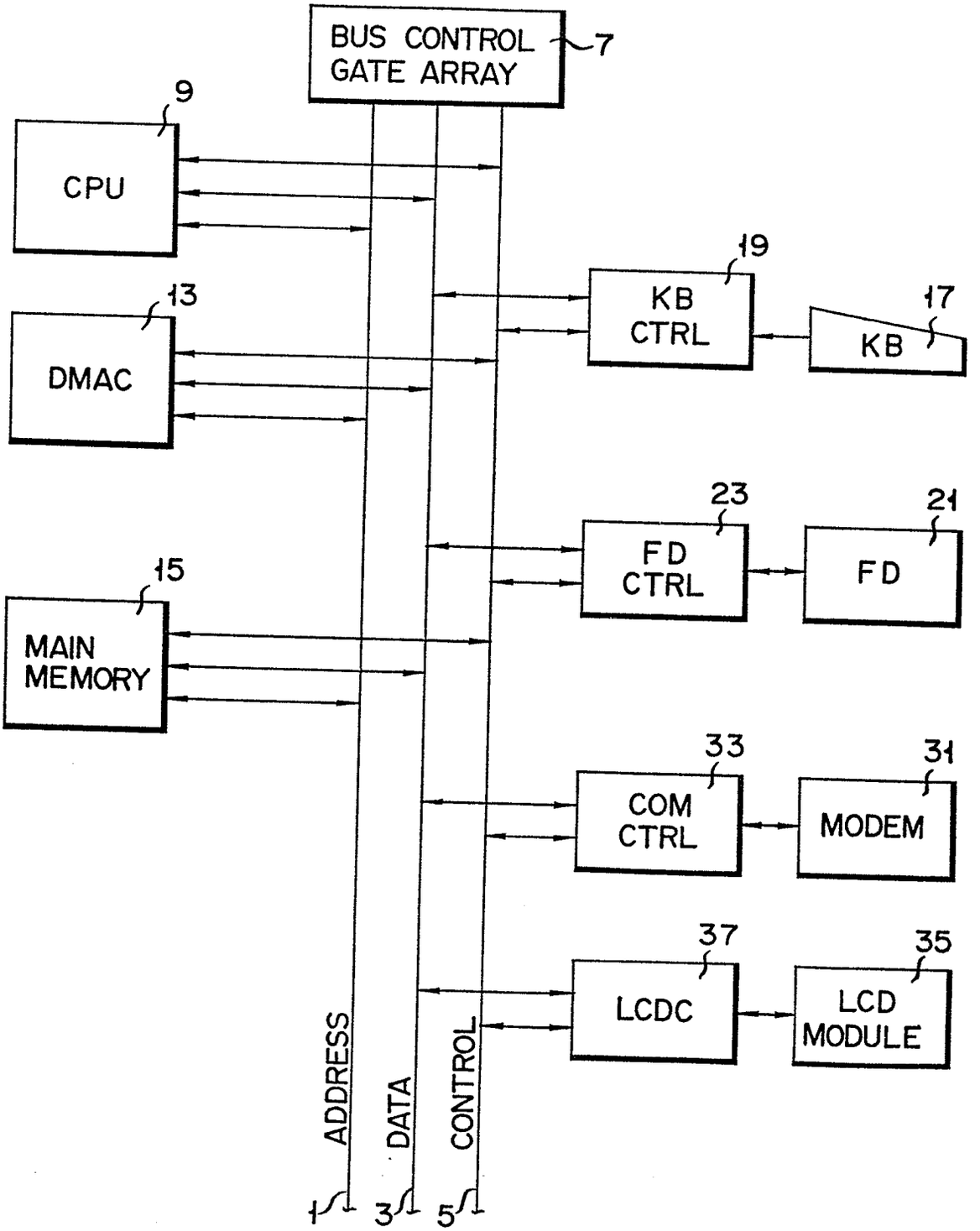
FIG. 1


BUS CONTROL GATE ARRAY
7
9
CPU
13
DMAC
15
MAIN MEMORY
19
KB CTRL
17
KB
23
FD CTRL
21
FD
33
COM CTRL
31
MODEM
37
LCDC
35
LCD MODULE
ADDRESS
DATA
CONTROL
1
3
5

2/2

FIG. 2

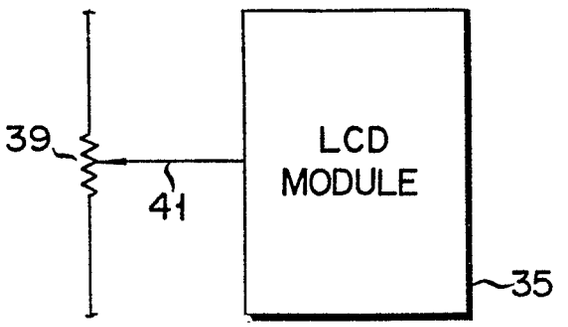
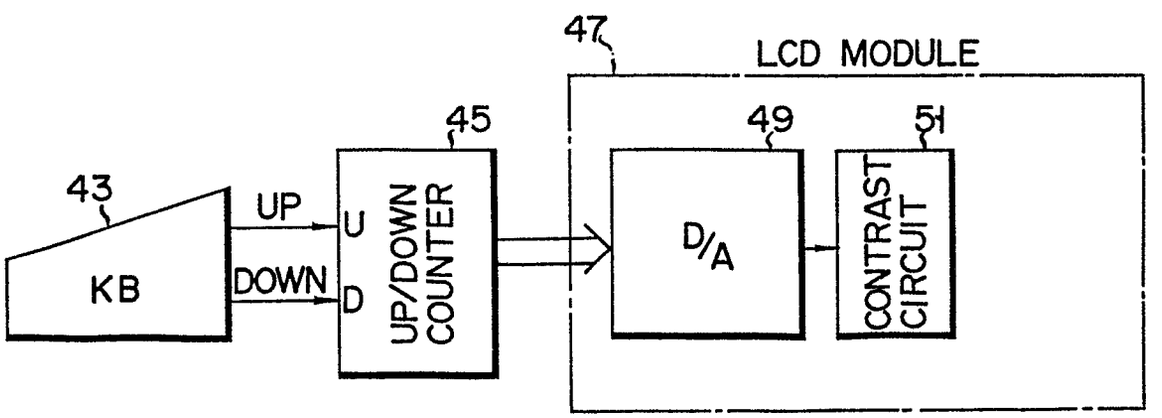

39
41
LCD
MODULE
35

FIG. 3


47
LCD MODULE
45
49
51
43
UP
DOWN
U
D
KB
UP/DOWN
COUNTER
D/A
CONTRAST
CIRCUIT