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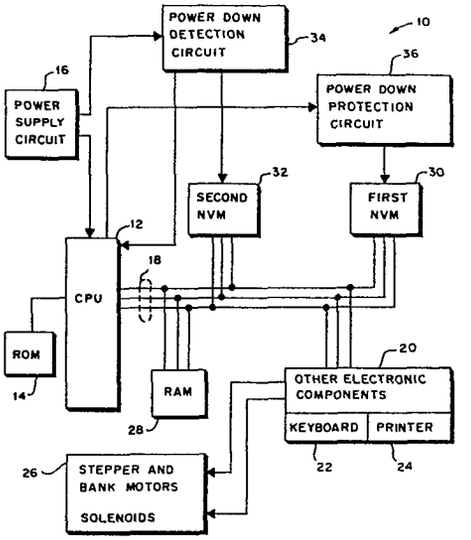
(54) Non-volatile memory system with real time and power down data storage capability for an electronic postage meter.

(57) A method and associated apparatus is provided for increasing the reliability of the stored accounting data which reflects the transactions of an electronic postage meter, including the steps of an associated apparatus for providing a first non-volatile memory (30) capable of storing accounting data which represents the postage meter transactions; updating the first non-volatile memory (30) in real time for each postage transaction to provide a current record of the accounting data for each postage transaction on-the-fly; providing a second non-volatile memory (32) capable of storing accounting data representing the postage meter transactions during a power down cycle of the postage meter; providing a volatile memory (28) capable of storing accounting data which represents the postage meter transactions; updating the volatile memory (28), in real time for each postage transaction to provide a current record of the accounting data for each postage transaction; and transferring the accounting data from the volatile memory (28) to the second non-volatile memory (32) during the power down cycle of the postage meter.



Non-Volatile Memory System with Real Time and Power Down Data Storage Capability for an Electronic Postage Meter

The present invention relates to electronic postage meters, and to methods and systems for increasing reliability of stored accounting data which reflects the transactions of an electronic postage meter.

Various electronic postage meter systems have been developed, as for example, the systems disclosed in United States Patent 3,978,457 for Microcomputerized Electronic Postage Meter Systems, United States Patent 3,938,095 for Computer Responsive Postage Meter, European Patent Application 80400603.9, filed May 5, 1980, for Electronic Postage Meter Having Improved Security and Fault Tolerance Features, United States Patent 4,301,507, for Electronic Postage Meter Having Plural Computing Systems, and co-pending European Patent Application No. 83 112 364.1, filed December 8, 1983, for Stand-Alone Electronic Mailing Machine.

Generally elecronic postage meters include some form of non-volatile memory capability to store critical postage accounting information. This information includes, for example, the amount of postage remaining in the meter for subsequent printing and the total amount of postage already printed by the meter. Other types of accounting or operating data may also be stored in the non-volatile memory, as desired.

However, conditions can occur in electronic postage meters where information stored in non-volatile memory may be lost. A total line power failure or fluctuation in voltage conditions can cause the microprocessor associated with the meter to operate erratically and either

cause erasure of data or the writing of spurious data in the non-volatile memory. The erasure of data or the writing of spurious data in the non-volatile memory may result in a loss of critical accounting information. Since the accounting data changes with the printing of postage and is not permanently stored elsewhere, there is no way to recapture or reconstruct the lost accounting information. Under such circumstances, it is possible that a user may suffer a loss of postage funds.

To minimize the likelihood of a loss of information stored in the non-volatile memory, various approaches have been adopted to ensure the high reliability of electronic postage meters. It is known from aforementioned United States Patent 3,978,457 and aforementioned co-pending European Patent Application No. 83 112 364.1 to provide a microprocessor controlled electronic postage meter having memory architecture which includes a temporary storage memory for storing accounting data reflecting each meter transaction and a non-volatile memory to which the accounting data is transferred during the power down cycle of the meter.

Another approach for preserving the stored accounting data has been the use of redundant non-volatile memories. One such redundant memory system is disclosed in European Patent Application No. 83 100 639.0, filed January 25, 1983.

With such redundant memory system the two redundant non-volatile memories are interconnected with a microprocessor by way of completely separate data and address lines to eliminate error conditions. The data may be applied to the memories simultaneously or sequentially at different times. Such a system minimizes

the possibility of non-detectable and/or non-correctable errors resulting from transients.

Another redundant memory system is disclosed in the aforementioned European Patent Application 80400603.9. In this patent application, accounting data is written into each of the two non-volatile memories, designated BAMs, twice during each postage meter transaction, once in temporary form and once in permanent form to minimize the loss of accounting data during microcomputer failure.

The aforementioned redundant memory systems may help to eliminate certain errors in the accounting data due to microcomputer failure or the presence of transcients. However, since writing into these memories occurs during each transaction or trip cycle of the meter, critical accounting data is written into the non-volatile memories during the noisiest cycle of meter operation when the presence of transients or spurious signals is probably greatest.

It is an object of the present invention to provide a non-volatile memory system for an electronic positive meter which minimizes errors in the stored accounting data.

It is a further object of the present invention to provide a non-volatile memory system for an electronic postage meter in which accounting data is written into different NVMs during two different cycles of postage meter operation.

It is a further object of the present invention to provide a non-volatile memory system with real time and power down data storage capability for an electronic postage meter to minimize the possibility of errors in the stored accounting data.

Briefly, in accordance with the present invention, a method and associated apparatus is provided for increasing the reliability of the stored accounting data which reflects the transactions of an electronic postage meter, including the steps of and associated apparatus for providing a first non-volatile memory capable of storing accounting data which represents the postage meter transactions; updating the first non-volatile memory in real time for each postage transaction to provide a current record of the accounting data for each postage transaction on-the-fly; providing a second non-volatile memory capable of storing accounting data representing the postage meter transactions during a power down cycle of the postage meter; providing a volatile memory capable of storing accounting data which represents the postage meter transactions; updating the volatile memory in real time for each postage transaction to provide a current record of the accounting data for each postage transaction; and transferring the accounting data from the volatile memory to the second non-volatile memory during the power down cycle of the postage meter.

Other objects, aspects and advantages of the present invention will be apparent from the following detailed description of an exemplary embodiment of the invention considered in conjunction with the drawings, in which:

FIGURE 1 is a block diagram of one embodiment for the non-volatile memory system of the present invention; and

FIGURE 2 is a flowchart illustrating the operation of the non-volatile memory system of the present invention.

Referring to Fig. 1, a non-volatile memory system for an electronic postage meter in accordance with the present invention is generally illustrated at 10. Preferably, the general architecture of the electronic postage meter is similar to that disclosed in the aforementioned co-pending patent application No. 83 112 364.1, modified as disclosed in Fig, 1. Specifically, a central processing unit 12, in the form of a microprocessor, e.g., a Model 8085A microprocessor, is operated under program control in accordance with the programs stored in a ROM 14. The microprocessor 12 is energized by the output of a power supply circuit 16 during a power up cycle to place the meter in an operative condition. The microprocessor 12 transmits and receives signals over a data bus 18 coupled to the various meter components.

Generally, the microprocessor 12 transmits signals to and receives signals from the other electronic components 20, the keyboard 22 and the printer 24 for the actuation of stepper and bank motors and solenoids 26 to accomplish the printing of postage on a document. Each such postage operation or printing transaction is referred to as a trip cycle.

During each trip cycle, a certain amount of postage is used. A volatile random access memory 28, such as model 8155 with the appropriate input and output and timing circuits, contains an ascending register (AR), a descending register (DR) and appropriate cyclic redundancy codes (CRCs) and control sums. During each trip cycle, and under control of the microprocessor 12, the descending register is decremented the appropriate amount for the postage used during the trip and the ascending register is incremented the appropriate amount for the postage used during the trip. Thus, the AR provides a running or current total of the amount of postage that has been used through completion of the last trip cycle and the DR provides a running or current total of the amount of postage remaining in the meter for subsequent use.

Also coupled to the data bus 18 to receive accounting data from the microprocessor 12 is a first NVM 30. Preferably, the NVM 30 is a SEEQ 5516A electrically erasable read only memory (EEROM) having an endurance of 1 million write cycles. However, it should be understood that other NVMs which have high endurances may also be utilized, such as a battery backed CMOS integrated circuit chip or other similar integrated circuit chips. Under control of the microprocessor 12 the accounting data for each meter postal transaction, i.e., AR and DR, and other accounting data, as desired, is written into the NVM 30, as well as the volatile RAM 28. Thus, a

permanent updated record of the accounting data is maintained on-the-fly in real time in the NVM 30.

A second NVM 32, such as an ER 3400 MNOS integrated circuit chip, is also electrically coupled to the data bus 18. Under control of the microprocessor 12, accounting data which is temporarily stored in the RAM 28 during each meter transaction is transferred from the RAM 28 and written into the second NVM 32 upon detection of a power down signal indicating commencement of a power down cycle.

During normal operation of the postage meter, the second NVM 32 is held in a non-write condition by the output signals from the microprocessor 12 over data bus 18. However, during a power failure (power down cycle), the microprocessor 12 initiates a power down cycle routine in which the accounting data which has been temporarily stored in the volatile RAM 28 is transferred or written into the first NVM 32. Upon completion of the transfer of accounting data into the second NVM 32, the second NVM 32 is disabled by a power down detection circuit 34 to prevent further writing therein by the microprocessor 12.

Advantageously, the power supply circuit 16 and the power down detection circuit 34 may be of the type disclosed in United States Patent 4,445,198, issued April 24, 1984, entitled Memory Protection Circuit For An Electronic Postage Meter. Upon receiving a first low power signal from the power supply circuit 16, the power down detection circuit 34 applies predetermined bias signals to the second NVM

32 to allow the transfer of accounting data thereto from the RAM 28 under control of the microprocessor 12. Thereafter, the bias voltages are removed from the second NVM 32 to disable the same and prevent any further writing of data therein from the microprocessor 12. Alternatively, the power supply circuit 16 and the power down detection circuit 34 may be of the type disclosed in co-pending European Patent Application No. 84 104 709.5, filed April 26, 1984.

Output signals from the microprocessor 12 are also electrically coupled to a power down protection circuit 36 such as disclosed in co-pending U.S. Patent Application Serial No. _____, entitled "Data Protection System for Electronic Postage Meters Having Multiple NVMs", a copy of which is filed together with this application for reference. The power down protection circuit 36 inhibits any further writing in the first NVM 30 upon detection of a power down condition by the microprocessor 12.

A flowchart for the operation of the memory system of the present invention is illustrated in Fig. 2 at 50. Considering this flowchart 50 and the apparatus 10 illustrated in Fig, 1, after power up of the postage meter, prior to undertaking a transaction or commencing a trip cycle, the meter is in its quiescent or steady state condition. In this condition, if the microprocessor 12 senses a power down condition, i.e., power failure, the microprocessor 12 immediately transfers all the accounting data from the RAM 28 to the second NVM 32 by writing it into the second NVM 32. Thereafter, the power down detection circuit 34 dis-

ables the second NVM 32 to preclude any further writing of spurious data therein by erratic operation of the microprocessor 12 during the remainder of the power down cycle. After the transfer of accounting data from the RAM 28 to the second NVM 32, the first NVM 30 is disabled by the power down protection circuit 36 to prevent any further writing of spurious data therein by erratic operation of the microprocessor 12 during the remainder of the power down cycle when the voltages applied to the various circuit elements are degrading towards zero volts through unspecified and undefined bias conditions.

If no power down condition is present, the microprocessor 12 waits for a trip signal indicating that a trip cycle is being commenced. When a trip is present, the accounting data in the RAM 28 is updated to reflect the results of the most recent postage transaction or trip cycle. Additionally, the accounting data for the postage transaction is written into the first NVM 30.

After writing the accounting data for the most recent transaction in RAM and the first NVM 30, the microprocessor 12 looks for a power down condition. If such a condition is present, the previously described operation is undertaken to transfer accounting data from the RAM 28 into the second NVM 32 while at the same time preventing any further writing of data into the first NVM 30. If a power down condition is not present, the microprocessor 12 looks for a trip completion signal after writing the accounting data in the RAM 28 and first NVM 30. Upon detection of a trip completion signal, the meter returns to its steady state condition where the aforementioned process may be repeated.

From the foregoing description, it should be apparent that "permanent" storage of accounting data

is provided on-the-fly in real time on a transaction by transaction basis to provide a first accounting data file during one cycle of meter operation, i.e., during the trip cycle, and that "permanent" storage of accounting data is also provided during the power down cycle by transferring accounting data from temporary storage to "permanent" storage to provide a second accounting data file during another cycle of meter operation, i.e., during the power down cycle. Advantageously, the second accounting data file is permanently constructed during a period of the meter operation, i.e., the power down cycle, when spurious signals are at a minimum.

It should be understood for the purpose of the present application that the term postage meter refers to the general class of devices for the imprinting of a defined unit value for governmental or private carrier delivery of parcels, envelopes or other like applications for unit value printing. Thus, although the term postage meter is utilized, it is both known and employed in the trade as a general term for devices utilized in conjunction with services other than those exclusively employed by governmental postage and tax services. For example, private, parcel and freight services purchase and employ such meters as a means to provide unit value printing and accounting for individual parcels.

Further, it will be apparent to those skilled in the art that various modifications may be made in the present invention without departing from the spirit and scope thereof as described in the specification and defined in the appended claims.

The disclosure of copending European Patent Applications No. and No. (Our Refs: 42 513 and 42 514)

Claims:

1. A method of increasing the reliability of the stored accounting data which reflects the transactions of an electronic postage meter, characterised by the steps of:

providing a first non-volatile memory (30) capable of storing accounting data which represents the postage meter transactions;

updating the first non-volatile memory (30) in real time for each postage transaction to provide a current record of the accounting data for each postage transaction on-the-fly;

providing a second non-volatile memory (32) capable of storing accounting data representing the postage meter transactions during a power down cycle of the postage meter;

providing a volatile memory (28) capable of storing accounting data which represents the postage meter transactions;

updating the volatile memory (28) in real time for each postage transaction to provide a current record of the accounting data for each postage transaction; and

transferring the accounting data from the volatile memory (28) to the second non-volatile memory (32) during the power down cycle of the postage meter.

2. A method according to Claim 1, wherein:

the first non-volatile memory (30) is updated during each trip cycle of the meter.

3. A method according to Claim 1 or 2, wherein:

the first non-volatile memory (30) has a greater endurance for data storage than the second non-volatile memory (32).

4. A method according to any one of claims 1 to 3 including the steps of:

updating the first non-volatile memory (30) under control of a microprocessor (12); and

transferring data to the second non-volatile memory (32) during the power down cycle under control of the microprocessor (12).

5. A method for increasing the reliability of the stored accounting data which reflects the transactions of an electronic postage meter, characterised by the steps of:

providing a first non-volatile memory (30) capable of storing accounting data representing the transactions of the postage meter;

updating the first non-volatile memory (30) during each trip cycle of the postage meter to write the accounting data resulting from each trip cycle therein;

providing a second non-volatile memory (32) capable of storing accounting data representing the transactions of the postage meter; and

writing accounting data into the second non-volatile memory (32) only during the power down cycle of the postage meter.

6. A method for increasing the reliability of the stored accounting data which reflects the transactions of an electronic postage meter, characterised by the steps of:

providing a first non-volatile memory (30) capable of storing accounting data reflecting the transactions of the meter;

writing accounting data into the first non-volatile memory (30) during each transaction of the postage meter to provide a current record of the accounting data

providing a volatile memory (28) capable of storing accounting data which reflects the postage meter transactions;

writing accounting data into the volatile memory (28) during each transaction of the postage meter to provide a current record of the accounting data for each postage transaction;

enabling a second non-volatile memory (32) for the writing of accounting data therein upon the detection of a power down signal; and

transferring the accounting data present in the volatile memory (28) to the second non-volatile memory (32) upon detection of the power down signal to provide two records of accounting data reflecting the transactions of the meter which are written into non-volatile memory during two different cycles of operation of the postage meter.

7. A system for increasing the reliability of the stored accounting data which reflects the transactions of an electronic postage meter, characterised by:

first non-volatile memory means (30) for storing accounting data reflecting the transactions of the postage meter;

volatile memory means (28) for storing accounting data reflecting the transactions of the postage meter;

second non-volatile memory means (32) for storing accounting data reflecting the transactions of the postage meter; and

microprocessor means (12) electrically connected to said first and second non-volatile memory means (30, 32) and said volatile memory means (28) for writing accounting data into said first non-volatile memory means (30) and said volatile

memory means (28) in real time during each trip cycle of the postage meter and transferring the accounting data stored in said volatile memory means (28) to said second non-volatile memory means (32) only during a power down cycle of the meter.

8. A system according to Claim 7, wherein:

said first non-volatile memory (30) is updated under control of said microprocessor means (12) to reflect each transaction of the postage meter.

9. A system according to Claim 7 or 8, wherein:

said first non-volatile memory (30) has a greater endurance for data storage than said second non-volatile memory (32).

10. A system according to any one of Claims 7 to 9, wherein:

said first non-volatile memory means (30) is an EEROM.

11. A system for increasing the reliability of the stored accounting data which reflects the transactions of an electronic postage meter, characterised by:

first non-volatile memory means (30) for storing accounting data representing the transactions of the postage meter;

second non-volatile memory means (32) for storing accounting data representing the transactions of the postage meter;

microprocessor means (12) electrically connected to said first and second non-volatile memory means (30, 32) for writing accounting data into said first non-volatile memory means (30) in real time during each trip cycle of the postage meter to provide a current record of accounting data on-the-fly and for writing accounting data into said second non-volatile memory means only during the power down cycle of the postage meter.

12. A system for increasing the reliability of the stored accounting data which reflects the transactions of an electronic postage meter, characterised by:

first non-volatile memory means (30) for storing accounting data reflecting the transactions of the postage meter;

microprocessor means (12) for writing accounting data into said first non-volatile memory means (30) in real time during each transaction of the postage meter;

volatile memory means (28) for storing accounting data reflecting the transactions of the postage meter;

said microprocessor means (12) writing accounting data into said volatile memory means (28) during each transaction of the postage meter to provide a current record of the accounting data for each postage transaction;

second non-volatile memory means (32) for storing accounting data reflecting the transactions of the postage meter;

means for detecting a power down condition to enable said second non-volatile memory means (32) for the writing of accounting data therein during the power down cycle;

said microprocessor means (12) transferring the accounting data present in said volatile memory means (28) to said second non-volatile memory means (32) during the power down cycle of the postage meter to provide two records of accounting data reflecting the transactions of the meter which are written into said non-volatile memory means (28) during two different cycles of operation of the postage meter.

13. A system according to Claim 12, wherein:

said first non-volatile memory means (30) is an EEROM.

14. A system according to Claim 12 or 13, wherein:

said first non-volatile memory means (30) is an EEROM; and

said second non-volatile memory means (32) is an MNOS memory.

15. An electronic postage meter operable according to any one of claims 1 to 6 or comprising the system of any one of Claims 7 to 14.

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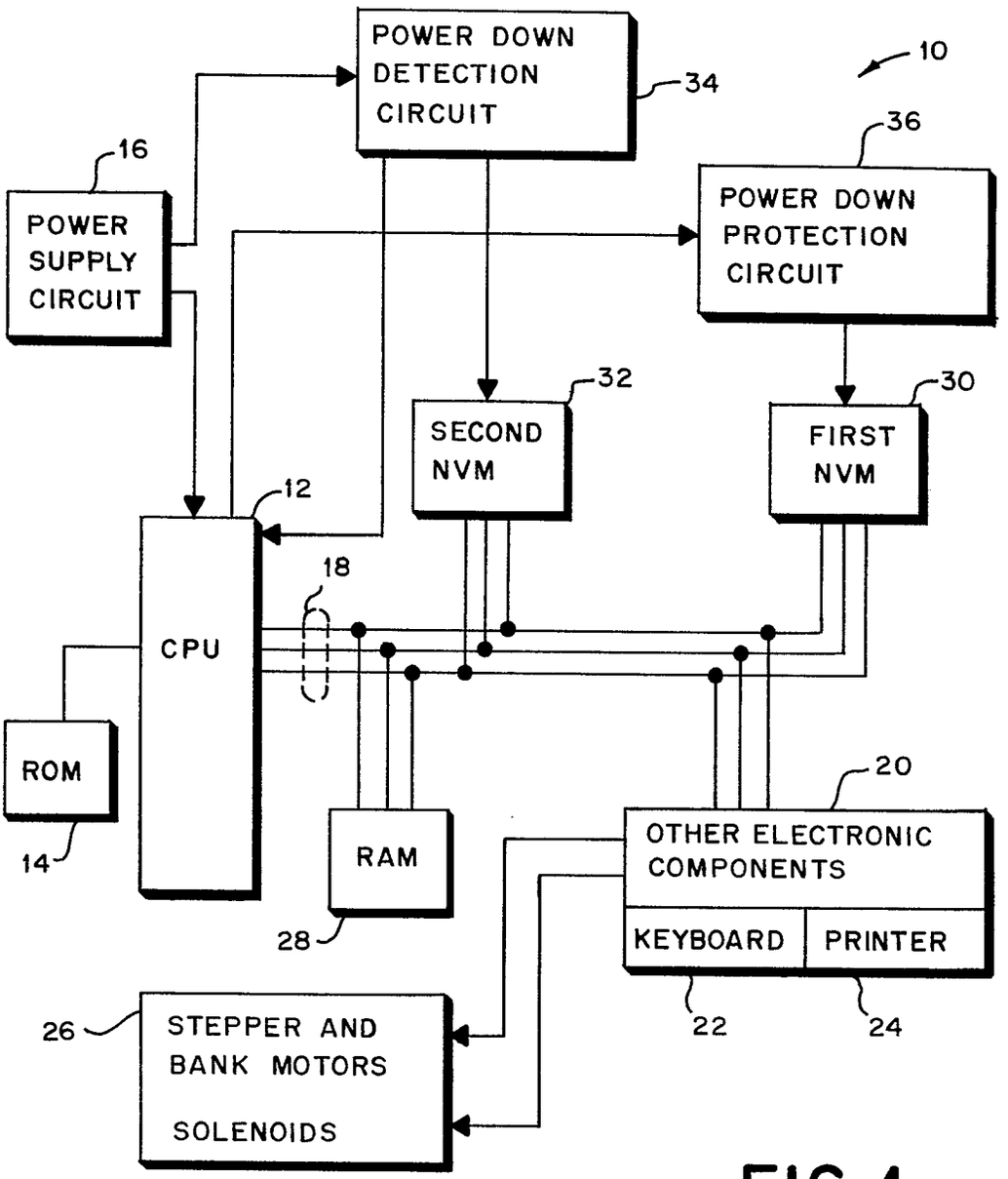

FIG. 1

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FIG. 2