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(54) CATHODE RAY TUBE DISPLAY SYSTEM.

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EP-A-0 105 725
US-A-4 357 604

Fernseh & Kino Technik, volume 37, nr. 9, September 1983, Berlin (DE), pages 375/384 Werner Rudolf:"Elektronische Zeichenerzeugung bei Rastersichtgeräten", see page 376, left-hand column, line 23 - right-hand column, line 8

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Description

Technical Field

This invention relates to cathode ray tube display systems of the kind including: a cathode ray tube adapted to display images on the screen thereof; memory means adapted to the store data to be displayed; processing means adapted to access said memory means; a cathode ray tube controller adapted to access said memory means to refresh images displayed on said screen; and multiplexing means connected to receive address signals from said processing means and from said cathode ray tube controller and having an output coupled to said memory means, said multiplexing means being responsive to a switching signal to provide address signals from said processing means to said output, and said signal generating means being responsive to an inhibit signal to inhibit the provision of said video signal for a predetermined period of time.

Background Art

In a conventional cathode ray tube (CRT) display device, it is generally known that it is necessary to repeatedly refresh the screen on the CRT, normally on the order of 50-60 times per second, in order to maintain the displayed state and in the manner wherein a controller sequentially reads out all addresses in a refresh memory. In addition, it is also necessary to access the refresh memory from a central processing unit (CPU) for any modification of the screen-displayed content and for other purposes.

A cathode ray tube display system of the kind specified is known from U.S. Patent Specification US-A-4,379,293. The known system includes a CRT controller connected to a processor and having a refresh address generator to refresh the display on the cathode ray tube, an update address generator to update information in the refresh memory, and a control circuit for connecting the update address generator and the refresh address generator to address the memory so that only one of the generators has control of the refresh memory at a time. The known system has the disadvantage of being complex in construction and hence expensive to manufacture.

From EP-A-0 105 725 there is known a cathode ray tube display system wherein data to be displayed on a cathode ray tube (CRT) is formed by a microcomputer during a display period and is stored in a work memory. A CRT controller supplies a vertical. synchronizing signal to the CRT, which signal also serves as an interrupt signal for the microcomputer whereby an address supplied by the microcomputer is effective to access a display memory, such that data is transferred from the work memory to the display memory during the vertical blanking period of the picture being displayed on the CRT. When the amount of data to be transferred is large, the data transfer is continued beyond the vertical blanking period and during the data transfer the display on the CRT is inhibited, whereby a visual impression is created as if the picture disappeared for a short period of time.

Disclosure of the Invention

According to the present invention, a cathode ray tube display system of the kind specified is characterized by control means coupled to said processing means, said multiplying means and said video signal generating means by first data bus means connected to said memory and to latching means which are connected to said signal generating means; and by second bus means connected to said processing means and to gating means connected to said first bus and responsive to a gating signal provided by said control means to connect said first bus means to said second bus means; whereby, in response to a request signal applied from said processing means to said control means, said control means is effective to provide said switching signal to said multiplexing means, to provide said gating signal to said gating means and to provide said inhibit signal to said signal generating means.

It will be appreciated that a cathode ray tube display system according to the invention has the advantage of being relatively simple in construction. A further advantage is that the system has the capability of obviating any flashing or flickering on the screen which could occur during processor access to the refresh memory. Still another advantage is that timing difficulties are alleviated. For example, synchronization between reference clocks for the processor and the cathode ray tube controller and any consequent need for high speed circuit elements is avoided.

In brief summary of a preferred embodiment of the invention, the preferred embodiment utilizes a cathode ray tube having a long persistence light emission time.and constructed in such a manner that the CRT controller monopolizes the refresh memory to sequentially read out addresses therefrom unless access to the memory is requested by the central processing unit (CPU). Data which is read out from the refresh memory by the CRT controller is stored in a latch circuit and a character generator produces a display pattern signal which is based on such data. The display pattern signal is converted into serial data by a parallel-to-serial converter and is sent to the long persisting CRT as a video signal for controlling electron beams.

The control unit in the system of the preferred embodiment is constructed so as to generate and send out various control signals such as a select signal for switching an appropriate address bus when the access to the memory is requested by the CPU, a gate control signal for connecting and switching a data bus, and a video ir hibit signal. When the CPU requests access to the refresh memory, the control unit sends the select signal to a multiplexer to switch the address bus from the CRT controller to the CPU and also sends the gate control signal to the gate to connect a data line of the memory with the data bus of the CPU. At the same time, the control unit sends a read or

write signal to the refresh memory to permit the access to the memory from the CPU. The data stored in the latch when the CPU accesses the memory is not the data to be displayed on the CRT at that time, but is the data based on the access from the CPU so that sending a video signal which is generated in form as based on this data to the long persisting CRT would cause a flash to appear on the CRT screen. In order to avoid the flashing, the control unit sends the video inhibit signal for a predetermined period of time after the access is requested by the CPU to inhibit the video signal from being sent out from the parallel-to-serial converter. Thus, a portion of the screen will not flicker owing to the visual persistence effect of the long persisting CRT even though the sending out of the video signal is inhibited for the predetermined period of time.

Brief Description of the Drawings

One embodiment of the present invention will now be described by way of example with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram illustrating the diagrammatic structure of a system according to the present invention;

Fig. 2 is a logic diagram of the control unit of Fig. 1 and showing the relationship between the control unit and the peripheral elements thereof;

Fig. 3 is a logic diagram of a modification in which the sending time of the display inhibit signal is prolonged; and

Fig. 4 is a timing diagram showing the various operation timings of the embodiment of Fig. 2.

Best Mode for Carrying out the Invention

Fig. 1 is a block diagram illustrating the diagrammatic structure of an embodiment of the present invention wherein 10 is a central processing unit or CPU using an SCLK as the reference clock signal, 12 is a cathode ray tube or CRT controller using a CCLK as the reference clock signal, 14 is a CRT refresh memory for storing data required for the CRT screen display and 16 is a multiplexer for switching an address bus 18 from the CPU 10 and an address bus 20 from the controller 12 so as to connect either one of the buses to the memory 14. A latch circuit 22 is controlled by the reference clock CCLK to latch the data on a data line of the memory 14. A character generator CG 24 sends a pattern signal of a character to be displayed in accordance with the data in the latch circuit 22, and a parallel-to-serial converter 26 converts the parallel display pattern signal sent from the character generator 24 into a serial signal to send it to a CRT 30 as the video signal. A long persisting CRT 30 uses fluorescent paint such as P-39 or the like to provide a CRT screen of long persistence time. A control unit 32 sends various control signals such as a select signal 33, a gate control signal 35, and a video inhibit signal DISPLAY INHIBIT according to the request from the CPU 10 to access the memory 14. A gate circuit 34 is provided between and connects a data bus 36 of the CPU and a data bus 38 of the memory 14.

The CRT controller 12 sequentially reads out the content of the refresh memory 14 while always counting up addresses one by one in accordance with the reference clock CCLK to refresh the display on the screen of the CRT 30. In the case wherein an access to the memory 14 is requested by the CPU 10, the control unit 32 sends the select signal to the multiplexer 16 to switch the address line to the address bus 18, sends the gate control signal to the gate circuit 34 to connect the data bus 36 and the data line 38 together and to access the memory 14 simultaneously therewith. The data on the data line 38 which is sent at that particular time is a read data in response to the request of the CPU 10 or is a write data sent from the CPU and is not the data intended for the CRT 30 display. However, the latch circuit 22 unconditionally latches the data on the data line 38 in accordance with the reference clock CCLK and the character generator 24 produces a display pattern signal based on the latch data in the latch and sends it to the parallel-to-serial converter 26. Then, if the converter 26 converts the display pattern signal into a serial signal and sends it to the CRT 30 as the video signal, a character which should not be displayed will be instantaneously displayed and thereby cause the flash to generate or appear on the CRT screen.

The DISPLAY INHIBIT signal is adapted to inhibit the sending out of the video signal for the predetermined period of time until a correct display pattern signal comes out, thereby preventing flashing on the screen. In the present invention, the long persisting CRT 30 is used so that a preferable display state can be maintained without flicker on the screen, owing to the visual persistence effect of the long persisting CRT, even though the sending out of the video signal is stopped or delayed for the predetermined period of time.

The control unit 32 is now described in detail with reference to Fig. 2 which is a diagrammatic block diagram illustrating the relationship between the control unit and the associated peripheral circuit elements. As seen in Fig. 2, a memory request signal $\overline{\text{MREQ}}$ and a read signal $\overline{\text{RD}}$ or a write signal WR, the latter two signals being inverted through a gate 42, are input into an AND gate 44, the output of which is connected to a flip-flop 46, to the gate circuit 34, and to the multiplexer 16. The read signal $\overline{\text{RD}}$ is input into the gate circuit 34 and is inverted by an inverter 48 to be input into a NOR gate 50 together with the output from the AND gate 44 and then to be supplied to the refresh memory 14. The write signal $\overline{\text{WR}}$ is directly supplied to the refresh memory 14.

The output of the flip-flop 46 is connected to the input of a flip-flop 52 through an AND gate 54, and the output of the flip-flop 52 is connected to the parallel-to-serial converter 26 as a DISPLAY INHIBIT signal. The reference clock CCLK signal of the controller 12 is input through an inverter 56 to

the clock inputs of the flip-flops 46 and 52. The reference clock signal CCLK is also provided to the latch circuit 22 through an inverter 58.

When the CPU 10 requests to access the refresh memory 14, that is, when signals $\overline{\text{MREQ}}$ and $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signals go to the low level, the output from the gate 44 also goes to the low level which output is then sent to the multiplexer 16 and the gate circuit 34 as means for generating the select signal 33 and the gate control signal 35, whereby the switching of the address buses 18 and 20 and the connection between the data buses 36 and 38 are accomplished. Additionally, the $\overline{\text{RD}}$ signal is also being input into the gate 34 by which its connecting direction is switched in such a manner that the data from the memory 14 is sent to the CPU 10 in the read mode while the data from the CPU is written into the memory 14 in the write mode. At the same time, the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal is sent to the refresh memory 14 thereby to read the data from or write the data into the memory.

When the output from the AND gate 44 is at the low level, the flip-flop 46 is directly reset by reason of which the flip-flop 52 is also reset at the next fall of the reference clock signal CCLK. When the flip-flop 52 is reset, the low output is sent to the parallel-to-serial converter 26 as the DISPLAY INHIBIT or video inhibit signal to inhibit the video signal from being sent to the CRT 30. The flip-flops 46 and 52 are sequentially set at each falling of the CCLK signal after the output from the AND gate 44 goes to the high level. In other words, the flip-flop 52 is set at the second falling edge of the CCLK signal after the output from the AND gate 44 goes to the high level and, hence, the video inhibit signal is not sent out.

Although in this embodiment, the duration of the DISPLAY INHIBIT signal corresponds to that of two reference clock CCLK signals, the duration and the time of sending the video inhibit signal can be freely changed depending on the access time of the character generator 24 and the parallel-to-serial converter 26 and the necessity or requirement of the Chinese or like character display. For example, in order to display one Chinese character, it is necessary to continuously access the refresh memory 14 two times and, in relation thereto, it is necessary to send the video inhibit signal for a relatively longer time. Accordingly, and as illustrated in Fig. 3, it is also possible to send the video inhibit signal for a period of time corresponding to the period required for sending out four reference clock CCLK signals; for example, by additionally providing two flip-flops 62 and 64 along with associated AND gates 66 and 68 at the front stage of the AND gate 54 and of the flip-flop 52.

Fig. 4 is a timing diagram illustrating various operation timings of the embodiment in Fig. 2. The controller 12 accesses the refresh memory 14 by sequentially counting up addresses in accordance with the reference clock CCLK signal. As shown in Fig. 4, when the memory request $\overline{\text{MREQ}}$ signal (d) and then the read $\overline{\text{RD}}$ signal or write $\overline{\text{WR}}$ signal (e) are sent from the CPU 10, the select signal (g) is immediately sent to the multiplexer 16 to switch the address buses 18 and 20. Since the address data is already sent on the address bus 18 of the CPU 10 as shown by Fig. 4(c), the memory read or memory write signal (f) is immediately sent out. In Fig. 4 (h) is shown the access address of the refresh memory 14 and (i) is the address of the data to be latched into the latch circuit 22. Since the data on the data line 38 is latched into the latch circuit 22 at the next falling of the CCLK signal, the latched data of the latch circuit and the now-existing access data on the data line 38 are offset from each other for one cycle. Since the display pattern signal that is produced is based on the latched data of the latch circuit 22, the video signal is sent to the long persisting CRT 30, delayed by one cycle after the CPU 10 has accessed the memory. As shown by (h), the access from the CPU 10 is performed or accomplished in a manner that is unrelated to the reference clock CCLK signal so that incomplete memory access [see addresses 2 and 3 in Fig. 4(h)] is performed or accomplished before and after the access address (the shaded portion) of the CPU 10. Since the access time of the data read out by this incomplete access is short, the data of the next read-out address 3 in Fig. 4(i) is latched to the latch circuit 22 in spite of whether or not the data is correctly read out. Thus, as shown by Fig. 4(j), the video inhibit signal is being sent out during the time of access of data of the CPU 10 and during the time that data of the address 3 are being latched into the latch circuit 22, thereby inhibiting the sending out of the video signal from the parallel-to-serial converter 26 during that time.

It is seen in previous arrangements that, in order to process the access request of the CPU 10 without delay, the high and low periods of the reference clock corresponding to the CCLK signal as shown in Fig. 4(a) were respectively assigned as the access periods from the CPU 10 and the CRT controller 12 so that it was necessary to access at a half cycle of the CCLK signal and, hence, the high-speed elements were needed.

In the present embodiment, the CRT controller 12 reads out the addresses from the refresh memory 14 in a monopolizing manner when the access to the memory is not requested by the CPU 10, and the controller gives a priority to the CPU when the access is requested by the CPU and sends the video inhibit signal during that time whereby the full one cycle of the reference clock CCLK signal is assigned as the access time of the memory so that the present invention can provide the CRT display device in an arrangement capable of processing the access request of the CPU without delay even when elements of relatively low speed are used. Additionally, the flashing on the screen due to the generation of an incorrect video signal can be avoided and a preferable display state can be maintained by generating the video inhibit signal for inhibiting the sending out of the video signal based on the access data of the CPU 10 and by utilizing the visual persistence

effect of the long persisting CRT 30. Further, it is not necessary to synchronize the reference clock SCLK signal of the CPU 10 with the reference clock CCLK signal of the CRT controller 12 so that the CRT 30 display device of a simpler construction can be provided. Moreover, the CRT 30 display device is composed of a simpler structure by using low speed elements so that a lower priced CRT display device can be provided.

Claims

1. A cathode ray tube display system, including: a cathode ray tube (30) adapted to display images on the screen thereof; memory means (14) adapted to store data to be displayed; processing means (10) adapted to access said memory means (14); a cathode ray tube controller (12) adapted to access said memory means (14) to refresh images displayed on said screen; and multiplexing means (16) connected to receive address signals from said processing means (10) and from said cathode ray tube controller (12) and having an output coupled to said memory means (14), said multiplexing means (16) being responsive to a switching signal to provide address signals from said processing means (10) to said output, and said signal generating means (24, 26) being responsive to an inhibit signal to inhibit the provision of said video signal for a predetermined period of time, characterized by control means (32) coupled to said processing means (10), said multiplexing means (16) and said video signal generating means (24, 26); by first data bus means (38) connected to said memory means (14) and to latching means (22) which are connected to said signal generating means (24, 26); and by second bus means (36) connected to said processing means (10) and to gating means (34) connected to said first bus means (38) and responsive to a gating signal provided by said control means (32) to connect said first bus means (38) to said second bus means (36); whereby in response to a request signal applied from said processing means (10) to said control means (32), said control means (32) is effective to provide said switching signal to said multiplexing means (16) to provide said gating signal to said gating means (34) and to provide said inhibit signal to said signal generating means (24, 26).

2. A display system according to claim 1, characterized in that said cathode ray tube (30) has a persistence time sufficiently long, in dependence on said predetermined period of time, as to prevent flashing or flickering of the display on said screen.

3. A display system according to claim 2, characterized in that said signal generating means (24, 26) includes a character generator (24) coupled to parallel-to-serial converting means (26) adapted to provide said video signal and arranged to receive said inhibit signal.

4. A display system according to claim 1, characterized in that said processing means includes a microprocessor (10).

Patentansprüche

1. Kathodenstrahlenröhren-Anzeigesystem mit: einer Kathodenstrahlenröhre (30), die geeignet ist, Bilder auf ihrem Schirm anzuzeigen; einer Speichervorrichtung (14), die geeignet ist, anzuzeigende Daten zu speichern; einer Verarbeitungsvorrichtung (10), die geeignet ist, auf die Speichervorrichtung (14) zuzugreifen; einer Kathodenstrahlenröhrensteuerung (12), die geeigent ist, auf die Speichervorrichtung (14) zuzugreifen, um auf dem Schirm angezeigte Bilder aufzufrischen und einer Multiplexervorrichtung (16), die zum Empfang von Adressensignalen von der Verarbeitungsvorrichtung (10) und von der Kathodenstrahlröhrensteuerung (12) geschaltet und mit einem Ausgang versehen ist, der mit der Speichervorrichtung (14) gekoppelt ist, wobei die Multiplexervorrichtung (16) auf ein Schaltsignal anspricht, um Adressensignale von der Verarbeitungsvorrichtung (10) an den Ausgang zu legen und die Signalerzeugungsvorrichtung (24, 26) auf ein Blockiersignal anspricht, um die Abgabe des Videosignals für eine vorbestimmte Zeitperiode zu blockieren, gekennzeichnet durch eine Steuervorrichtung (32), die mit der Verarbeitungsvorrichtung (10), der Multiplexervorrichtung (16) und der Videosignal-Erzeugungsvorrichtung (24, 26) gekoppelt ist; durch eine erste Datensammelleitungsvorrichtung (38), die mit der Speichervorrichtung (14) und einer Haltevorrichtung (22) gekoppelt ist, die mit der Signalerzeugungsvorrichtung (24, 26) verbunden sind; und durch eine zweite Sammelleitungsvorrichtung (36), die mit der Verarbeitungsvorrichtung (10) und einer mit der ersten Sammelleitungsvorrichtung (38) verbundenen Torvorrichtung (34) verbunden ist, die auf ein von der Steuervorrichtung (32) abgegebenes Torsignal anspricht, um die erste Sammelleitungsvorrichtung (38) mit der zweiten Sammelleitungsvorrichtung (36) zu verbinden; wodurch unter Ansprechen auf ein von der Verarbeitungsvorrichtung (10) an die Steuervorrichtung (32) angelegtes Anforderungssignal die Steuervorrichtung (32) wirksam wird, um das Schaltsignal an die Multiplexervorrichtung (16) zu legen, um das Torsignal an die Torvorrichtung (34) abzugeben und das Blockiersignal an die Signalerzeugungsvorrichtung (24, 26) zu legen.

2. Anzeigesystem nach Anspruch 1, dadurch gekennzeichnet, daß die Kathodenstrahlröhre (30) eine genügend lange Nachleuchtdauer abhängig von der vorbestimmten Zeitperiode besitzt, um ein Aufblitzen oder Flackern der Anzeige auf dem Schirm zu verhindern.

3. Anzeigesystem nach Anspruch 2, dadurch gekennzeichnet, daß die Signalerzeugungsvorrichtung (24, 26) einen Zeichen-Generator (24) aufweist, der mit einer Parallel-Seriell-Umwandlungsvorrichtung (26) gekoppelt ist, die geeignet ist, das Videosignal abzugeben, und angeordnet ist, das Blockier-signal zu empfangen.

4. Anzeigesystem nach Anspruch 1, dadurch gekennzeichnet, daß die Verarbeitungsvorrichtung einen Mikroprozessor (10) aufweist.

Revendications

1. Système d'affichage à tube à rayons cathodiques, comprenant: un tube (30) à rayons cathodiques conçu pour afficher des images sur son écran; un moyen à mémoire (14) conçu pour stocker des données à afficher; des moyens de traitement (10) conçus pour accéder audit moyen à mémoire (14); un contrôleur (12) de tube à rayons cathodiques conçu pour accéder audit moyen à mémoire (14) afin de régénérer des images affichées sur ledit écran; et un moyen de multiplexage (16) connecté de façon à recevoir des signaux d'adresse dudit moyen de traitement (10) et dudit contrôleur (12) du tube à rayons cathodiques et ayant une sortie couplée audit moyen à mémoire (14), ledit moyen de multiplexage (16), en réponse à un signal de commutation, appliquant des signaux d'adresse provenant dudit moyen de traitement (10) à ladite sortie, et lesdits moyens (24, 26) de génération de signaux réagissant à un signal d'inhibition en inhibant la production dudit signal vidéo pendant une période de temps prédéterminée, caractérisé par un moyen de commande (32) couplé audit moyen de traitement (10), audit moyen de multiplexage (16) et auxdits moyens (24, 26) de génération de signal vidéo; par un premier moyen à bus de données (38) connecté audit moyen à mémoire (14) et à un moyen (22) de maintien qui sont connectés auxdits moyens (24, 26) de génération de signaux; et par un second moyen à bus (36) connecté audit moyen (10) de traitement et à un moyen (34) de déclenchement connecté audit premier moyen à bus (38) et qui, en réponse à un signal de déclenchement produit par ledit moyen de commande (32), connecte ledit premier moyen à bus (38) audit second moyen à bus (36); de sorte que, en réponse à un signal de demande appliqué à partir dudit moyen de traitement (10) audit moyen de commande (32), ledit moyen de commande (32) ait pour effet d'appliquer ledit signal de commutation audit moyen de multiplexage (16) pour appliquer ledit signal de déclenchement audit moyen (34) de déclenchement et appliquer ledit signal d'inhibition auxdits moyens (24, 26) de génération de signaux.

2. Système d'affichage selon la revendication 1, caractérisé en ce que ledit tube (30) à rayons cathodiques possède un temps de persistance suffisamment long, qui dépend de ladite période de temps prédéterminée, pour empêcher le clignotement ou le scintillement de l'affichage sur ledit écran.

3. Système d'affichage selon la revendication 2, caractérisé en ce que lesdits moyens (24, 26) de génération de signaux comprennent un générateur (24) de caractères couplé à un moyen (26) de conversion parallèlesérie pour produire ledit signal vidéo et agencé pour recevoir ledit signal d'inhibition.

4. Système d'affichage selon la revendication 1, caractérisé en ce que ledit moyen de traitement comprend un micro-processeur (10).

FIG. 1

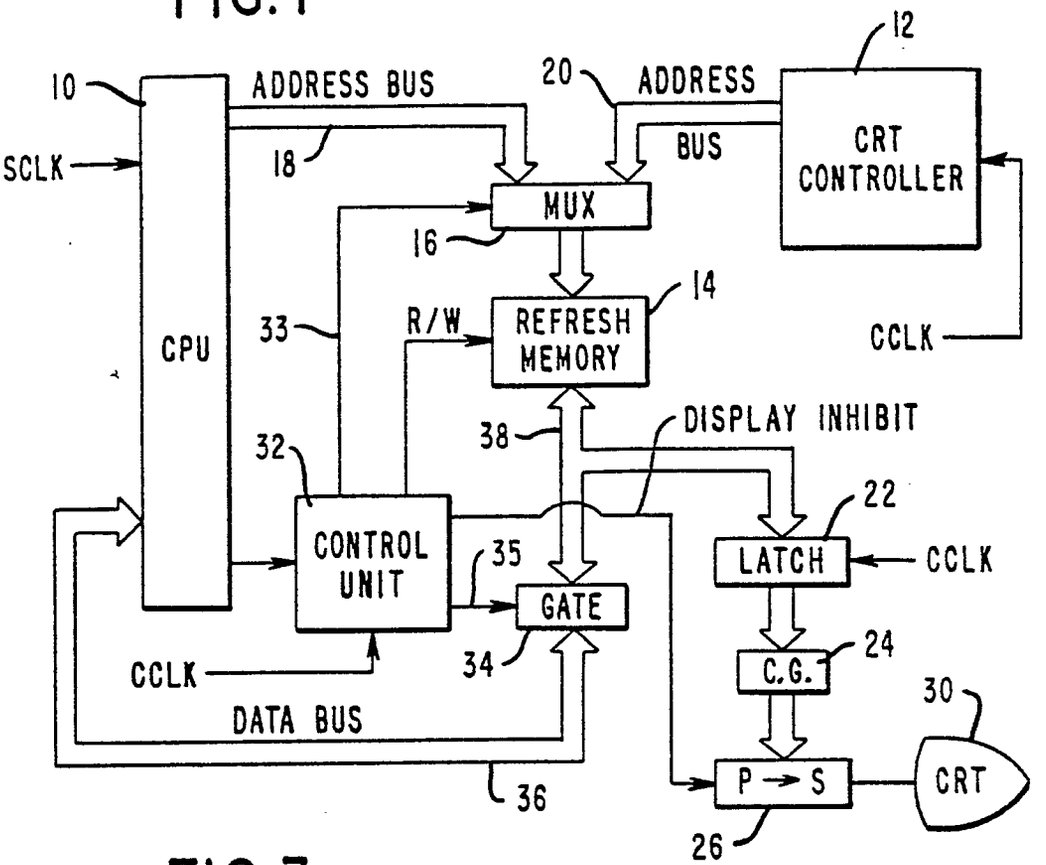

10
ADDRESS BUS
20
ADDRESS
BUS
12
CRT CONTROLLER
SCLK
18
MUX
16
CPU
33
R/W
REFRESH MEMORY
14
CCLK
DISPLAY INHIBIT
38
32
22
CONTROL UNIT
35
LATCH
CCLK
GATE
C.G.
24
CCLK
34
30
DATA BUS
P → S
CRT
36
26

FIG. 3

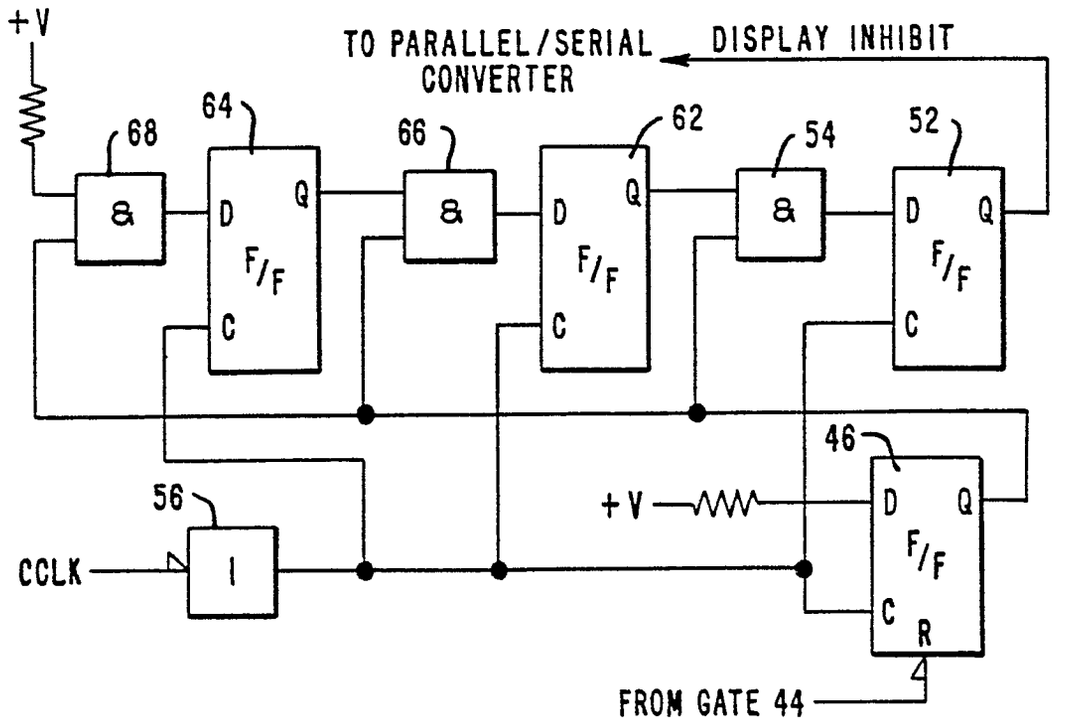

+V
TO PARALLEL/SERIAL CONVERTER
DISPLAY INHIBIT
64
68
66
62
54
52
&
D
Q
F/F
C
46
56
+V
CCLK
1
R
FROM GATE 44

FIG. 2

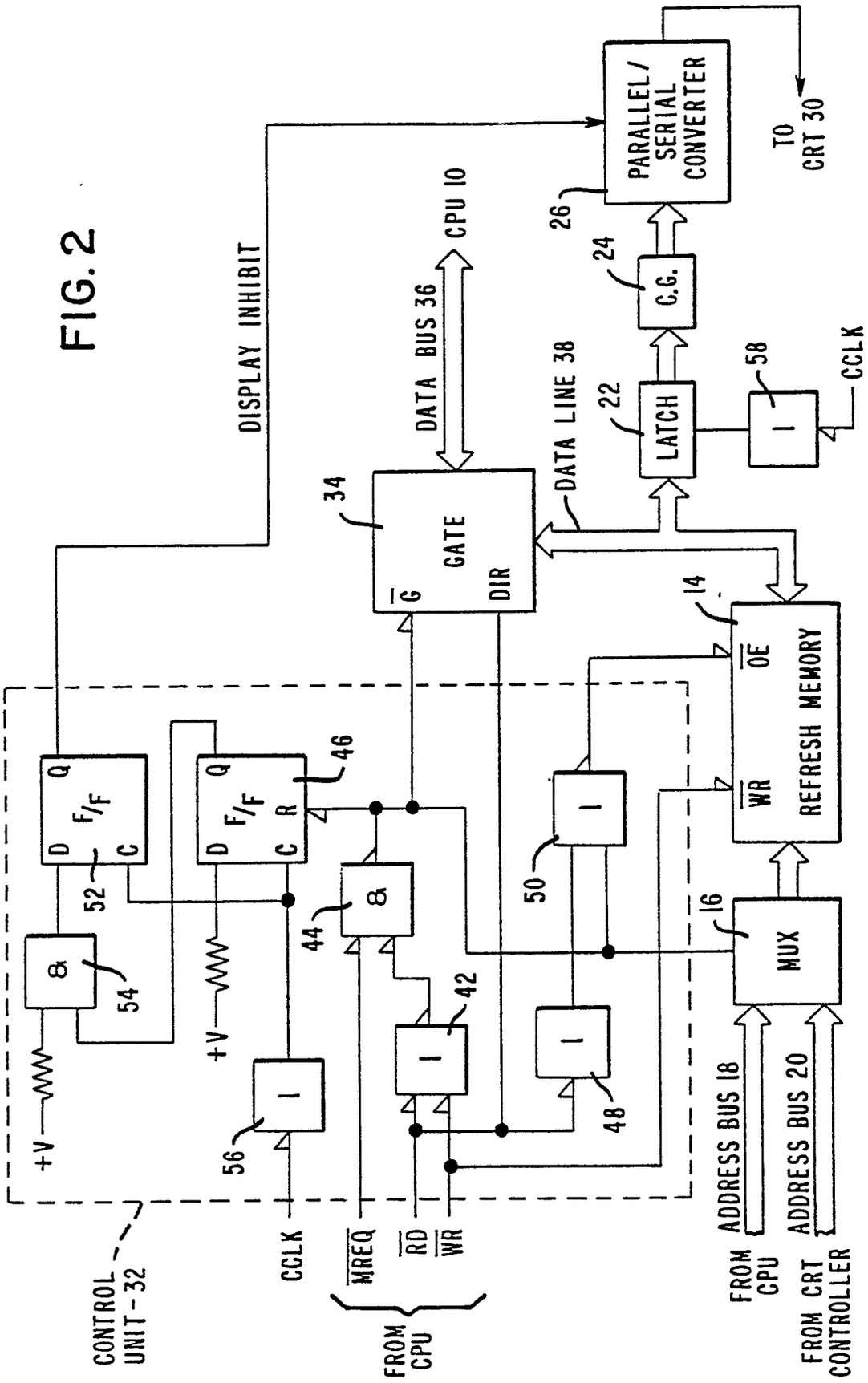
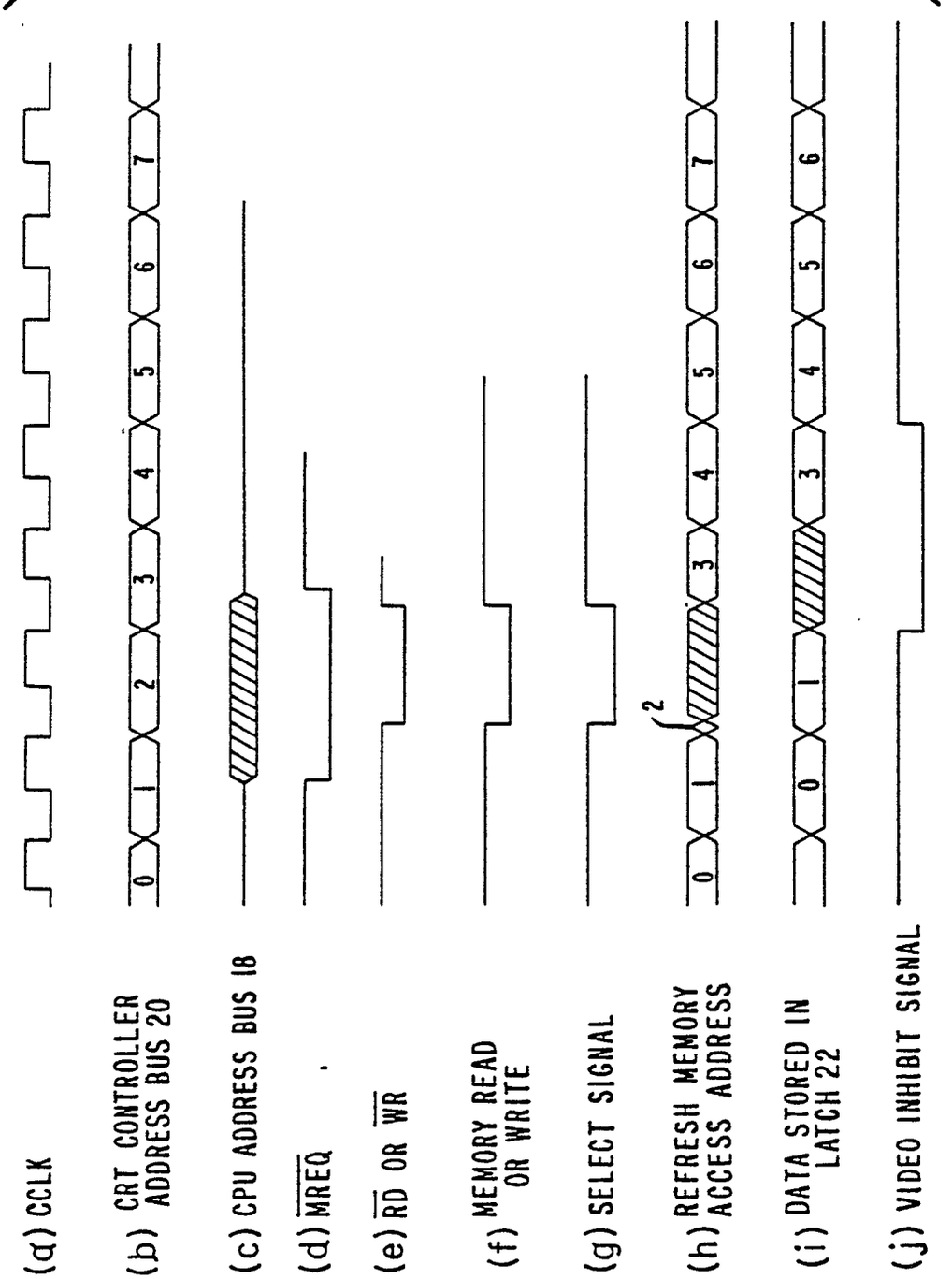

DISPLAY INHIBIT
DATA BUS 36
CPU IO
PARALLEL/ SERIAL CONVERTER
TO CRT 30
26
24
C.G.
DATA LINE 38
22
LATCH
58
CCLK
34
GATE
DIR
G
14
OE
WR
REFRESH MEMORY
46
D
Q
F/F
C
R
52
54
50
44
42
48
16
MUX
+V
56
CONTROL UNIT-32
CCLK
MREQ
RD
WR
FROM CPU
ADDRESS BUS 18
ADDRESS BUS 20
FROM CPU
FROM CRT CONTROLLER

FIG.4


(a) CCLK
(b) CRT CONTROLLER ADDRESS BUS 20
(c) CPU ADDRESS BUS 18
(d) $\overline{MREQ}$
(e) $\overline{RD}$ OR $\overline{WR}$
(f) MEMORY READ OR WRITE
(g) SELECT SIGNAL
(h) REFRESH MEMORY ACCESS ADDRESS
(i) DATA STORED IN LATCH 22
(j) VIDEO INHIBIT SIGNAL
0
1
2
3
4
5
6
7