

EUROPEAN PATENT APPLICATION

Application number: 86300847.0

Int. Cl.³: **H 04 N 5/91**
H 04 N 5/92, H 04 N 7/04

Date of filing: 07.02.86

Priority: 07.02.85 JP 22210/85
 07.02.85 JP 22211/85
 07.02.85 JP 22212/85
 15.03.85 JP 52646/85

Date of publication of application:
13.08.86 Bulletin 86/33

Date of deferred publication of search report: 09.12.87

Designated Contracting States:
DE FR GB

Applicant: Matsushita Electric Industrial Co., Ltd.
1006, Oaza Kadoma
Kadoma-shi Osaka-fu, 571(JP)

Inventor: Yoneyama, Masayuki
Syoei-ryo 30-23, Miyukihigashimachi
Neyagawa-shi Osaka-fu 572(JP)

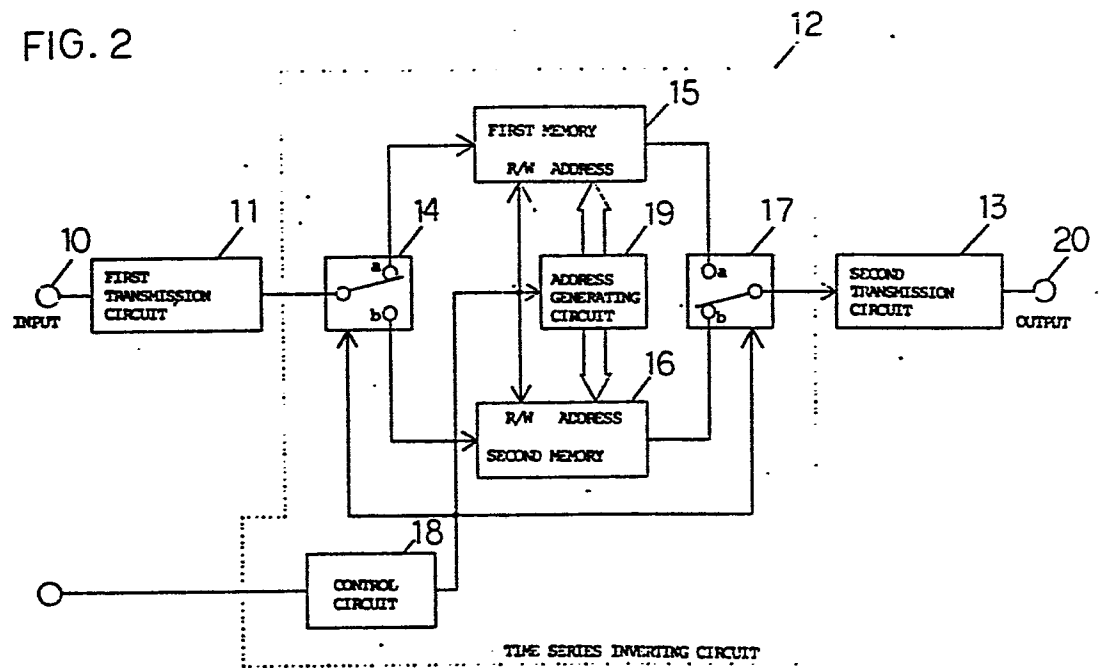
Inventor: Kobayashi, Masaaki
1-224, Nishitadahigashitouge
Kawanishi-shi Hyogo-ken, 661-01(JP)

Representative: Crawford, Andrew Birkby et al,
A.A. THORNTON & CO. Northumberland House 303-306
High Holborn
London WC1V 7LE(GB)

Signal processing apparatus.

A signal processing circuit for processing an input signal by first and second transmission circuits (11,13) in positive and inverse time series respectively. The first and second transmission circuits have a same transfer function. The apparatus includes first and second memories (15,16) and first and second switches (14,17). The first and second memories are selectively connected via the first switch (14) to the first transmission circuit (11) output and via the second switch (17) to the second transmission circuit (13) input. Each memory repeats write and read operations alternately in such a manner that an output signal of the first transmission circuit (11) is written for a predetermined period and the written signal is read for the subsequent predetermined period in a time series inverse to that for writing and sent to the second transmission circuit (13). While one of the first and second memories (15,16) is conducting write operation, the other is conducting read operation. The first and second switches and first and second memories are controlled by a control signal generated by a control circuit (18), which signal reverses its state with intervals of the predetermined period.

FIG. 2





DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X	EP-A-0 128 707 (KOBAYASHI) * Figures 3-8; page 9, lines 5-15; page 14, line 11 - page 16, line 16; page 17, line 22 - page 19, line 2 *	1	H 04 N 5/91 H 04 N 5/92 H 04 N 7/04
A	---	2,3	
A	L.R. RABINER et al.: "Theory and application of digital signal processing", 1975, pages 205-224, Prentice-Hall, Inc., Englewood Cliffs, US * Figure 4.3; page 207, line 6 - page 208, line 3; page 219, line 14 - page 220, line 10; page 223, line 1 - page 224, line 17 *	1,7	
A	---	1-5	TECHNICAL FIELDS SEARCHED (Int. Cl. 4) H 04 N
A	EP-A-0 132 140 (NISHIMOTO) * Figures 1,5-10; abstract; page 5, lines 9-28; page 7, line 21 - page 9, line 29; page 11, line 17 - page 14, line 19 *	1-3,5	
A	---		
A	US-A-4 405 942 (R.B. BLOCK) * Abstract; figures 7,8; column 3, lines 39-46; column 7, line 55 - column 10, line 36 *		

The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 18-09-1987	Examiner BOSCH F.M.D.
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			