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(54) Glitch energy reduction in digital gray scale CRT diplay.

(57) A circuit addition is described for a digital, gray scale CRT display circuit to substantially reduce glitch distortion during CRT beam intensity changes. A high pass filter and DC restoration circuit couples the control grid of the CRT to the video amplifier such that the cathode and control grid substantially track each other during a glitch. This results in no substantial change in beam intensity as would otherwise be perceived during a glitch. This is accomplished without signal conditioning prior to the output of the video amplifier circuit by means of either delaying the higher order bits of the binary value corresponding to the desired intensity level or sampling and holding the analog output of the D/A converter prior to application of that signal to the video amplifier.

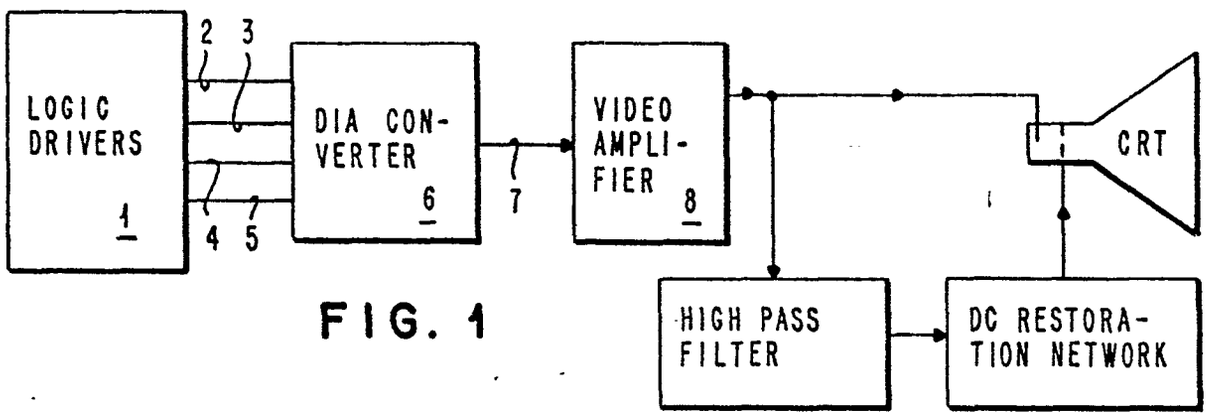

FIG. 1

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GLITCH ENERGY REDUCTION IN DIGITAL GRAY SCALE CRT DISPLAY

Technical Field

This invention relates to display circuitry in general and more particularly to a technique for reducing distortion in gray scale cathode ray tube (CRT) display devices during transitions of CRT beam intensities.

Background Art

The popularity of digitally controlled CRT display systems capable of gray scale presentation is increasing for graphical and text display applications in the office system environment. A block diagram of a digitally driven gray scale CRT display system is shown in Fig. 1. A digital representation of sixteen different beam intensity levels can be accomplished by the binary state of the signal levels on lines 2-5 from an array of logic drivers 1 to a digital to an analog (D/A) converter 6. Depending on the levels of the signals on lines 2-5, the D/A converter 6 produces one of sixteen different output voltages which is then applied to a video amplifier 8 along line 7. The output of the video amplifier 7 is applied to the cathode of a CRT 9 to control the beam intensity thereof, as is well known to those of skill in the art.

A problem occurs with conventional TTL logic components in providing the logic levels on lines 2-5 from the logic drivers 1 to the D/A converter 6. As one example, it requires more time for a TTL circuit to transition from an up level to a down level than it does for the same circuit to transition from a down level to an up level. With this fact in mind, consider the result of changing the beam intensity from that associated with a binary seven (0111) to a binary eight (1000). The zero bit in the binary seven transitions to a one before the one bits in the seven transition to zeroes. Thus, momentarily, the D/A converter 6 is presented with the binary value of fifteen (1111) until the one bits in the binary seven transition to the zero bits in the binary fifteen. With a high speed and accurate D/A converter as would be found in high speed, high performance CRT display systems, the momentary presentation of the binary value of fifteen would result in a momentary increase of beam intensity to the maximum in this system before it resumed operation at a beam intensity level associated with the binary value of eight, which is only one step difference in intensity from that associated with the binary value of seven. This explanation, of course, has assumed a sixteen level intensity resolution associated with a four bit binary value to define the intensity level. The problem would be similar when using other configurations involving greater or lesser resolution; that is, the beam intensity would momentarily be about twice the intended intensity when transitioning from a binary value in which the highest order bit is zero and all lower order bits are one to a value in which the highest order bit is one and all lower order bits are zero. Additionally, it will be understood that the problem also occurs when the intensity is being lowered one step from (in the example of a system with sixteen level resolution) an intensity level corresponding to the binary value of eight to an intensity level corresponding to the binary value of seven.

One solution to this problem has been to introduce a delay in the higher order bits of the binary value from the logic drivers. This results in less of a glitch during the transitions described above but also lowers the response time of the display device when large intensity transitions are required. For even slower applications, the glitch problem has been overcome by analog sample and hold circuitry at the output of the D/A converter to delay the signal from the D/A converter into the video amplifier until that signal has had time to stabilize to a value corresponding to the desired state.

It would, therefore, be greatly advantageous to substantially eliminate the above-described glitch problem in fast gray scale video amplifiers in a very inexpensive manner without any of the speed compromises described above relative to prior art solutions to this problem.

Disclosure of the Invention

Accordingly, a circuit comprising a high pass filter and DC restoration network is driven by the video amplifier output signal and applied to the control grid of the CRT. No signal conditioning is employed prior to the output of the video amplifier circuit. That is, the higher order bits of the binary value corresponding to the desired intensity level are not delayed and no sample and hold circuitry is employed between the D/A converter and the video amplifier. The fast changing glitch energy at the output of the video amplifier passes through the high pass filter and, when coupled to the control grid of the CRT through the DC bias restoration network, provides a circuit configuration in which the cathode and control grid of the CRT are employed as a difference amplifier. The CRT beam intensity is a function of the difference between the control grid and cathode voltages. Thus, as the cathode and control grid substantially track each other during a glitch, there is not the substantial change in beam intensity as would be perceived during a glitch without this circuitry between the cathode and control grid circuits.

The foregoing and other objects, features, extensions and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings.

Brief Description of Drawings

Fig. 1 is a block diagram of the system configuration of this invention including both the well known components of a digital gray scale CRT display system and, additionally, the high pass filter and DC restoration network of this invention to substantially minimize glitch energy in the CRT beam.

Figs. 2a and 2b is a waveforms illustrative of the origin of glitch energy in an uncompensated digital gray scale CRT display system.

Fig. 3 illustrates a D/A converter configuration which may be used in the configuration of a CRT display system employing this invention.

Fig. 4 illustrates a video amplifier circuit which may be used in the configuration of a CRT display system employing this invention.

Fig. 5 is a schematic circuit of the high pass filter and DC restoration network of this invention which provides for a minimization of glitch energy during CRT beam intensity transitions.

Figs. 6a6c are waveforms illustrative of the glitch energy rejection accomplished by the CRT beam intensity control

system of this invention using the difference of cathode and control grid voltages to control beam intensity.

Fig. 7 is a waveform illustrative of the effect of the additional circuitry of this invention on waveforms having zero glitch energy.

Best Mode for Carrying Out the Invention

Referring again to Fig. 1, which shows a block diagram of the system configuration of a gray scale CRT display system employing this invention, logic drivers 1 apply a parallel, multiple bit digital signal along lines 2-5 to the D/A converter 6. This multiple bit digital signal is converted to an analog voltage level by the D/A converter 6, as is well-known in the art, which is applied to the video amplifier 8 along line 7. No conditioning or compensation to reduce glitch energy is employed up to this point. That is, the highest order bits of the binary signal are not delayed with respect to the lower order bits, nor is any sample and hold circuitry employed between the output of the D/A converter 6 and the input of the video amplifier 8.

In prior art gray scale CRT display systems, the output of the video amplifier has been applied directly to the cathode of the CRT for beam intensity control while the control grid has been biased independently of the video amplifier drive to the cathode. However, it has been discovered that by deriving the portion of the video amplifier output waveform which includes the glitch energy and using this signal to modulate the control grid voltage during the duration of the glitch, the glitch can effectively be cancelled because the control grid and cathode of the CRT are used as a difference amplifier. Thus, this result is obtained because the CRT beam intensity is a function of the difference between grid and cathode voltages. As will be discussed in more detail below, a high pass filter is employed to derive only the fast changing glitch portion of the video amplifier output waveform for this control grid modulation, without passing the lower frequency portion of the video amplifier output waveform which is all that is present during smooth beam intensity transitions which do not include glitches.

In Fig. 2, the cause of beam intensity glitches in such CRT display systems is graphically illustrated. It will be noted in Fig. 2a that waveform 15, representative of the highest order, or most significant bit of the signal from the logic drivers 1 applied to the D/A converter 6, is at a valid, high level at time t_0. This is significantly earlier in time than t_1, at which latter time the least significant bits represented by waveforms 16 and 17 fall to valid, low levels. Referring to the video amplifier output waveforms shown in Fig. 2b, by t1 the waveform has responded to the earlier transition of only waveform 15 (Fig. 2a). By t2 the waveform has video amplifier has responded to the analog value associated with the digital value reached by t1 in Fig 2a.

For logic drivers 1, readily available, fast TTL logic may be employed. D/A converters of the current switching type are commercially available for use as the D/A converter 6. A typical configuration of such a D/A converter is shown in Fig. 3. The current switch portion of the D/A converter comprises current switching elements 20a-20n and current sources 21a-21n connected to lines driven by the least significant bit to the most significant bit, respectively, of the binary value applied from the logic drivers to the D/A converter. The current sources 21a-21n are connected in series between a summing network 22 and the switching elements 20a-20n. The output of the D/A converter is taken from the summing network 22 for application to the input of a video amplifier.

In Fig. 4, a typical configuration of a video amplifier is shown for a high resolution, high pel density display with fast transition characteristics. The amplifier in Fig. 4 is of a cascode configuration wherein the base of transistor 33 is driven by the output of a D/A converter through an impedance matching and speed-up circuit which comprises resistors 30 and 31 and capacitor 32. Base drive of transistor 33 causes current to flow through resistor 34 proportional to the voltage at the base of transistor 33. With appropriate base bias to the cascode transistor 35, current flow through transistor 33 and resistor 34 also flows through the collector and emitter of transistor 35, the shunt peaking inductor 36 and the load resistor 37. The output of the differential amplifier is taken at the collector terminal of the cascode transistor 35. The cascode transistor 35 is utilized to minimize the Miller effect associated with increased effective input capacitance due to high voltage gain. (Even though the overall amplifier voltage gain is high, that of the first stage -realized by transistor 33, emitter resistor 34 and the equivalent impedance of the collector 33 -is very low. The lower effective input capacitance allows for faster transitions.)

Resistor 34 and capacitor 38 form a zero to cancel out a pole at the output formed by resistor 37 and the combination of the output capacitance of transistor 35, the cathode capacitance of the CRT, as well as circuit board stray capacitance at the collector of transistor 35.

The high pass filter and DC restoration network of this invention is shown in Fig. 5. The output of the video amplifier 8, connected to the cathode of the CRT 9 is coupled through the high pass filter capacitor 41 to the control grid of the CRT 9. Potentiometer 42 controls the DC bias voltage (V_{ref}) of the control grid. This bias voltage is filtered by capacitor 43. Thus, capacitor 41 couples the glitch energy from the video amplifier 8 to the control grid of the CRT 9. Diode 44 allows the control grid to follow the glitch waveform downward but resets on the upswing of this waveform. This arrangement prevents the DC level of the control grid from shifting depending on the number of glitches encountered by the system.

Diode 44 and resistor 45 form the DC restoration network. Resistor 45 provides a discharge path for capacitor 41 when diode 44 is turned off.

Referring now to Figs. 6a-6c, the waveform in Fig. 6a is the uncorrected waveform presented by the video amplifier to the cathode of the CRT 9 by the circuit configuration shown in Fig. 1. The waveform in Fig. 6b is the signal applied to the control grid of the CRT 9 which is derived from the high pass filter and DC restoration circuit shown in detail in Fig. 5. The waveform in Fig. 6c is the resulting difference in the waveforms of Figs. 6a and 6b. It is, therefore, clear in Fig. 6c that the glitch shown in the uncorrected waveform of Fig. 6a is substantially reduced in the resulting, perceived waveform represented by Fig. 6c.

Fig. 7 shows the effect of the addition of the high pass filter and DC restoration network circuitry of Fig. 5 on waveforms having no glitch energy. The waveform shown by the dashed line in Fig. 7 is the video amplifier output while the waveform shown by the solid line in Fig. 7 represents the net beam intensity change as a result of coupling the video amplifier output waveform to the control grid through the high pass filter and DC restoration circuit.

In summary, a circuit addition has been described for a digital, gray scale CRT display circuit to substantially reduce glitch distortion during CRT beam intensity changes. A high pass filter and DC restoration circuit couples the control grid of the CRT to the video amplifier such that the cathode and control grid substantially track each other during a glitch. This results in no substantial change in beam intensity as would otherwise be perceived during a glitch. This is accomplished without signal conditioning prior to the output of the video amplifier circuit by means of either delaying the higher order bits of the binary value corresponding to the desired intensity level or sampling and holding the analog output of the D/A converter prior to application of that signal to the video amplifier.

While the invention has been shown and described with reference to particular embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

Claims

1.In a digital gray scale CRT display system including a video amplifier having an output connected to a cathode of a CRT, the improvement comprising:

means for deriving a glitch portion of the waveform of said video amplifier output; and

means for coupling said glitch portion of said video amplifier output waveform to a control grid of said CRT.

2. The CRT display system of Claim 1, wherein said means for deriving further comprises a high pass filter.

3. The CRT display system of Claim 2, wherein said means for coupling further comprises a DC restoration circuit.

4. The CRT display system of Claim 3, wherein said high pass filter further comprises a capacitor.

5. The CRT display system of Claim 4, wherein said DC restoration circuit further comprises a potentiometer for providing said control grid of said CRT a reference DC bias voltage.

6. The CRT display system of Claim 5, wherein said DC restoration circuit further comprises a resistor for connecting said DC bias voltage to said control grid of said CRT.

7. The CRT display system of Claim 6, wherein said DC restoration circuit further comprises a diode connected across said resistor for allowing said control grid to follow said glitch portion of said video amplifier output waveform in a first direction but resetting when said portion of said waveform reverses direction.

8. A CRT display system comprising:

a plurality of logic drivers for providing a set of digital signals associated with a desired beam intensity of said CRT;

a digital to analog converter which receives said set of digital signals and provides a voltage associated with said set of signals;

a video amplifier which receives said voltage and provides a beam intensity controlling voltage to a cathode of said CRT; and

means coupling a glitch energy portion of said beam intensity controlling voltage to a control grid of said CRT, whereby glitch energy in said beam intensity controlling voltage has a substantially reduced effect on said CRT beam.

9. The CRT display system of Claim 8, wherein said means for coupling further comprises a high pass filter.

10. The CRT display system of Claim 9, wherein said means for coupling further comprises a DC restoration circuit.

11. The CRT display system of Claim 10, wherein said high pass filter further comprises a capacitor.

12. The CRT display system of Claim 11, wherein said DC restoration circuit further comprises a potentiometer for providing said control grid of said CRT a reference DC bias voltage.

13. The CRT display system of Claim 12, wherein said DC restoration circuit further comprises a resistor for connecting said DC bias voltage to said control grid of said CRT.

14. The CRT display system of Claim 13, wherein said DC restoration circuit further comprises a diode connected across said resistor for allowing said control grid to follow said glitch energy portion of said beam intensity controlling voltage in a first direction and resetting when said portion of said controlling voltage reverses direction.

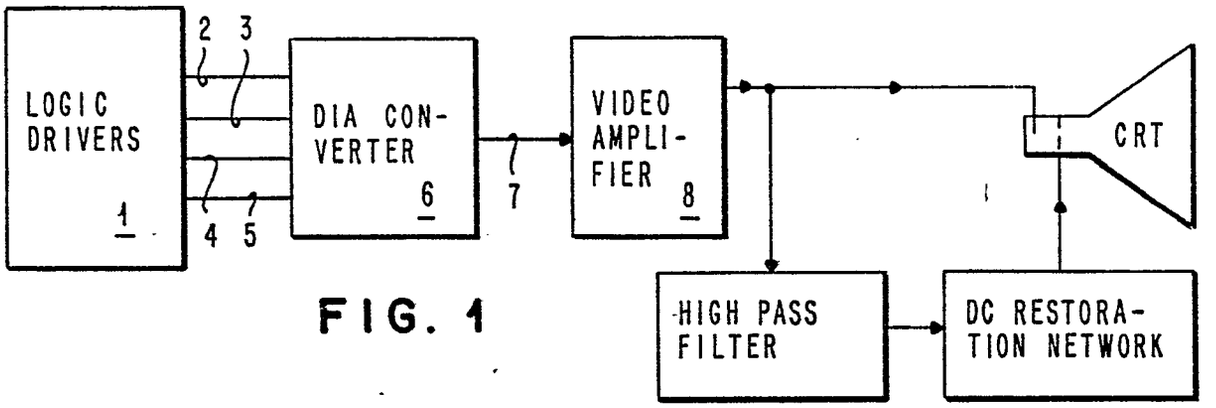

FIG. 1

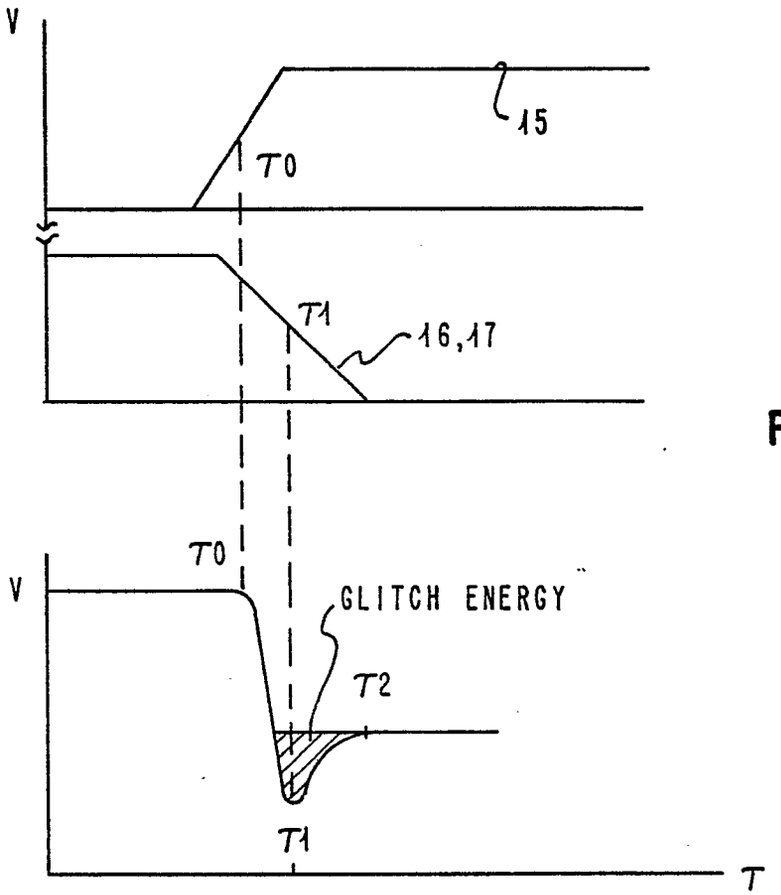

FIG. 2

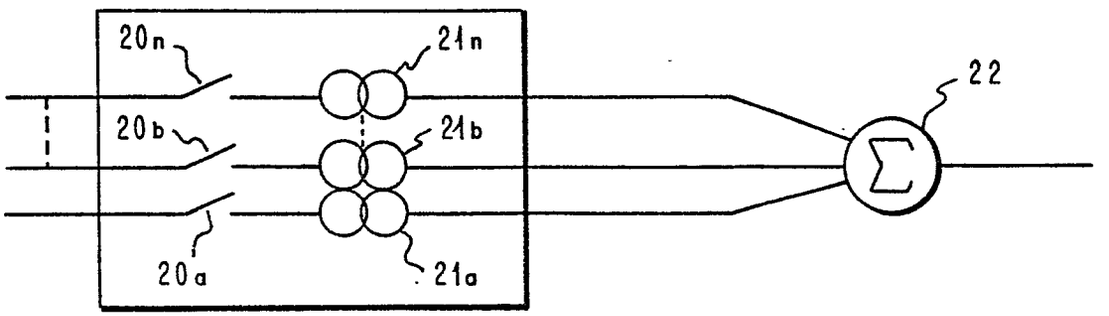

FIG. 3

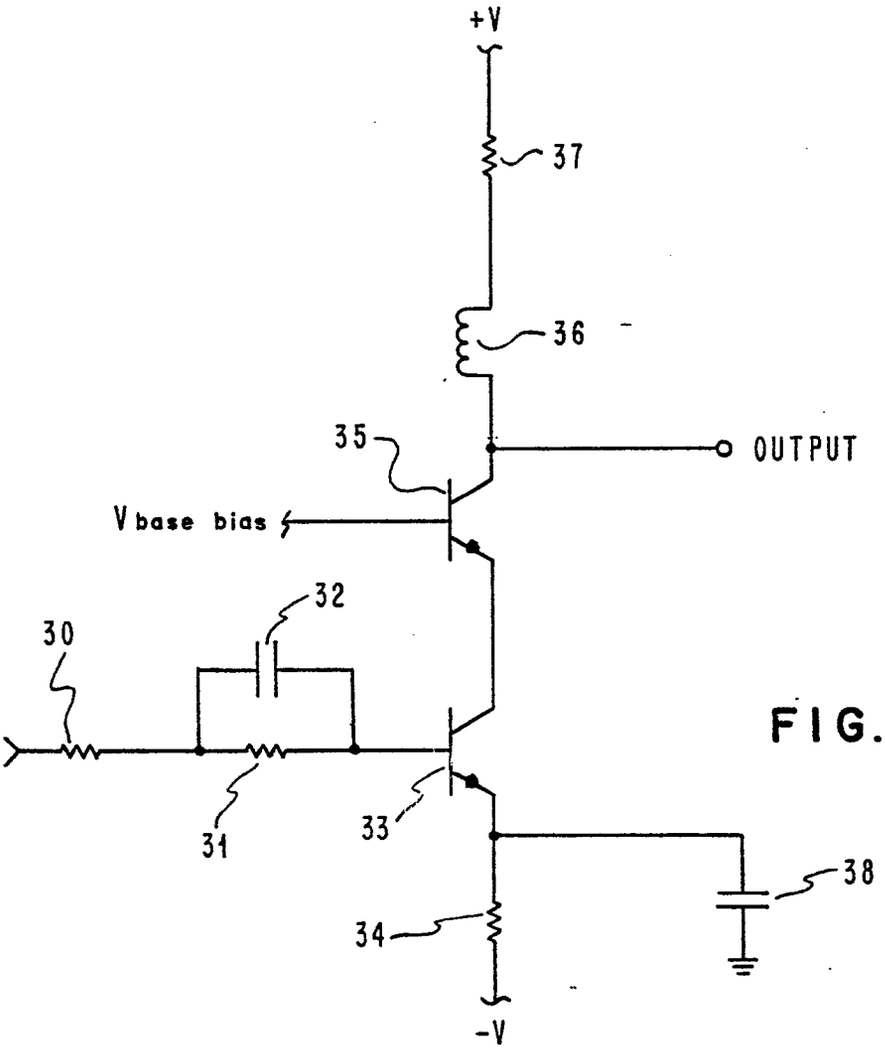
+V
37
36
35
OUTPUT
V base bias
32
30
31
33
38
34
-V

FIG. 4

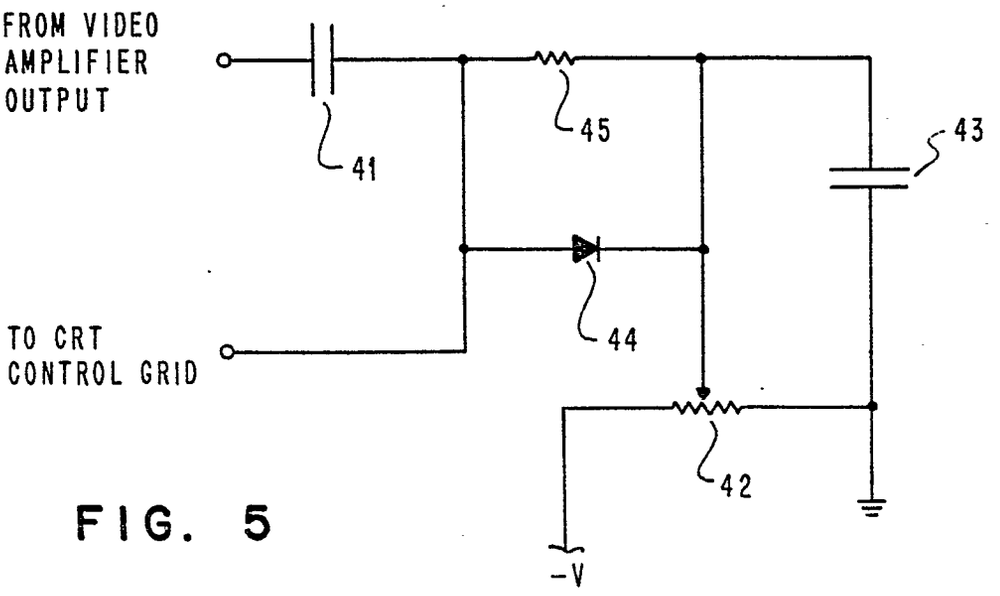
FROM VIDEO
AMPLIFIER
OUTPUT
41
45
43
44
TO CRT
CONTROL GRID
42
-V

FIG. 5

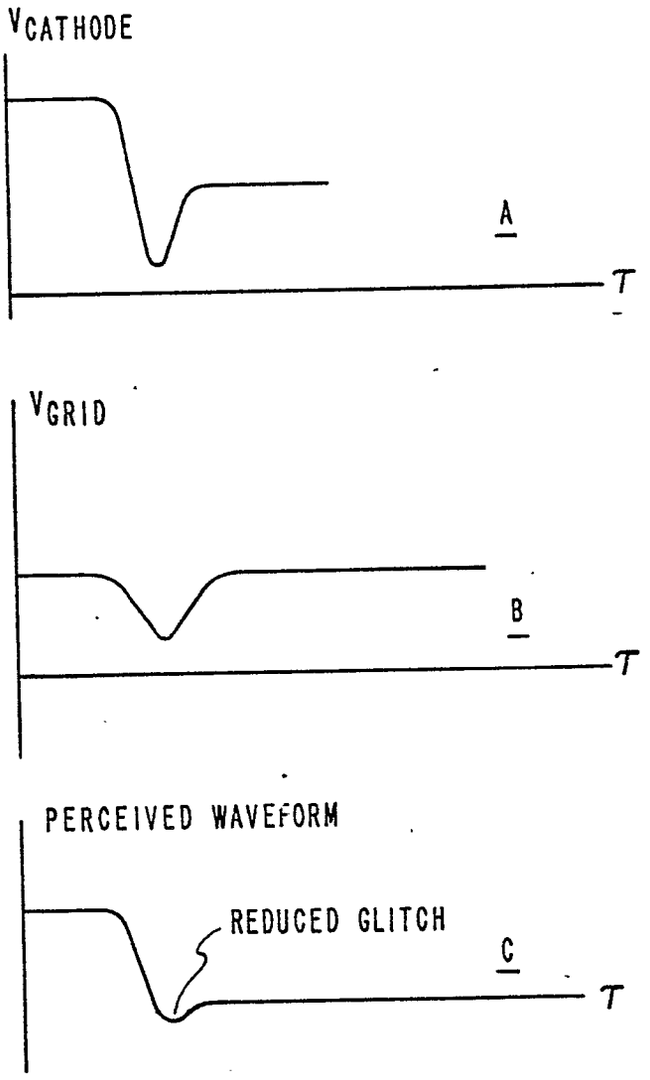
VCATHODE
A
T
VGRID
B
T
PERCEIVED WAVEFORM
REDUCED GLITCH
C
T

FIG. 6

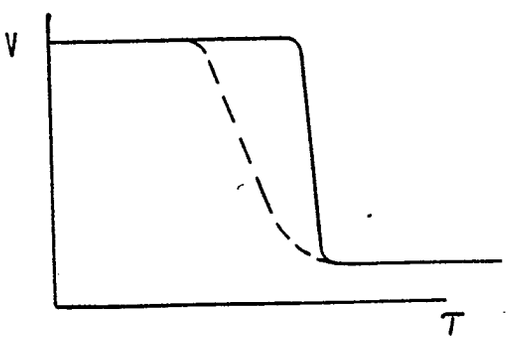
V
T

FIG. 7